AMD Xilinx - XC2VP4-5FGG256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	752
Number of Logic Elements/Cells	6768
Total RAM Bits	516096
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp4-5fgg256i

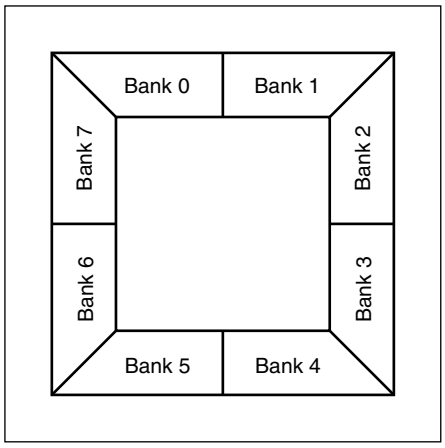

Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

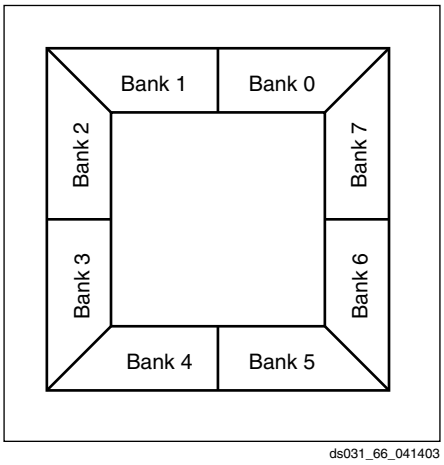

Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

CLB/Slice Configurations

Table 19 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 20 shows the available resources in all CLBs.

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kb Block SelectRAM+ Resources

Introduction

Virtex-II Pro devices incorporate large amounts of 18 Kb block SelectRAM+ resources. These complement the distributed SelectRAM+ resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II Pro block SelectRAM+ resource is an 18 Kb true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM+ behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

Virtex-II Pro block SelectRAM+ supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 21.

Table 21: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM+ has access to the 18 Kb memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kb memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked exter-

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

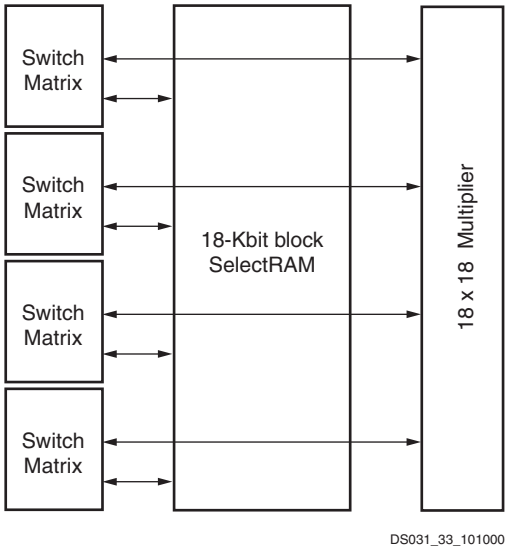

Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

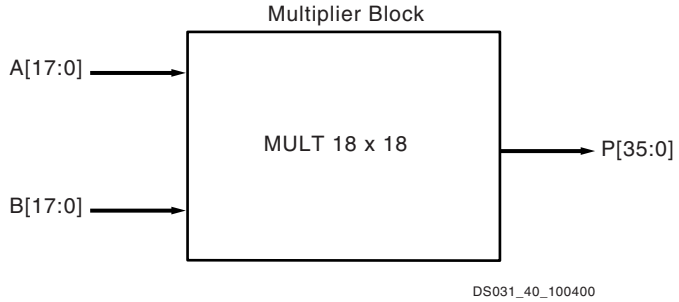

Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

SelectIO-Ultra DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, max	V, min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	24	–24
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.2	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI66_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCIX	–0.2	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)
GTLP	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.2	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL_I	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	8(2)	–8(2)
HSTL_II	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	16(2)	–16(2)
HSTL_III	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	24(2)	–8(2)
HSTL_IV	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	48(2)	–8(2)
SSTL2_I	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	6.7	–6.7
SSTL18_II	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		440	600	780	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

Table 36: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.59	0.68	0.75	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.59	0.68	0.75	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.59	0.68	0.75	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.49	0.57	0.62	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.27	0.31	0.35	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.27	0.31	0.35	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.17	0.20	0.22	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.17	0.20	0.22	ns
LVDS, 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.33	0.37	0.41	ns
LVDS, 2.5V, with Differential Termination (DT)	LVDS_25_DT	$T_{ILVDS\_25\_DT}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DT	LVDSEXT_25_DT	$T_{ILVDSEXT\_25\_DT}$	0.33	0.37	0.41	ns
ULVDS, 2.5V, with DT	ULVDS_25_DT	$T_{IULVDS\_25\_DT}$	0.31	0.36	0.40	ns
LDT, 2.5V, with DT	LDT_25_DT	$T_{ILDT\_25\_DT}$	0.31	0.36	0.40	ns

Multiplier Switching Characteristics

Table 45: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T_{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T_{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T_{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T_{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T_{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T_{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T_{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T_{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T_{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T_{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T_{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T_{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T_{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T_{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T_{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T_{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T_{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T_{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T_{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T_{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T_{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T_{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T_{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T_{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T_{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T_{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T_{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T_{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T_{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T_{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T_{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T_{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T_{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T_{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T_{MULT_P0}	1.13	1.27	1.43	ns, max

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 8, with Master Serial clock timing shown in Figure 9. Programming parameters for both Slave and Master modes are given in Table 50.

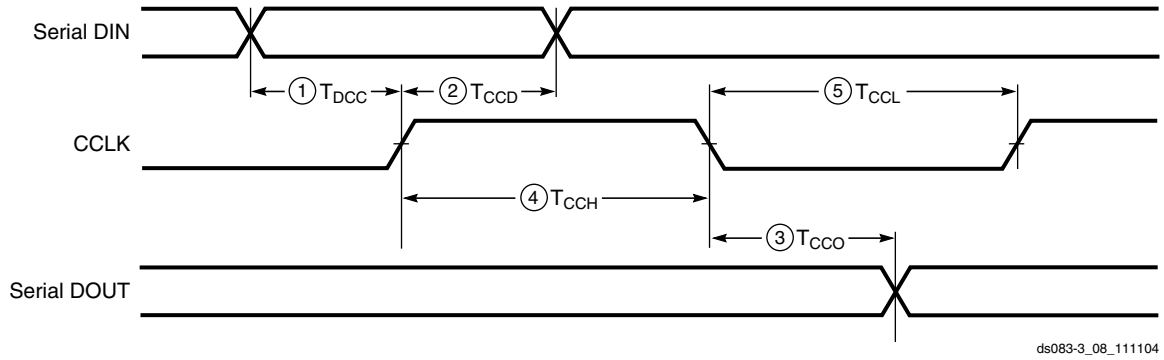

Figure 8: **Slave Serial Mode Timing Sequence**

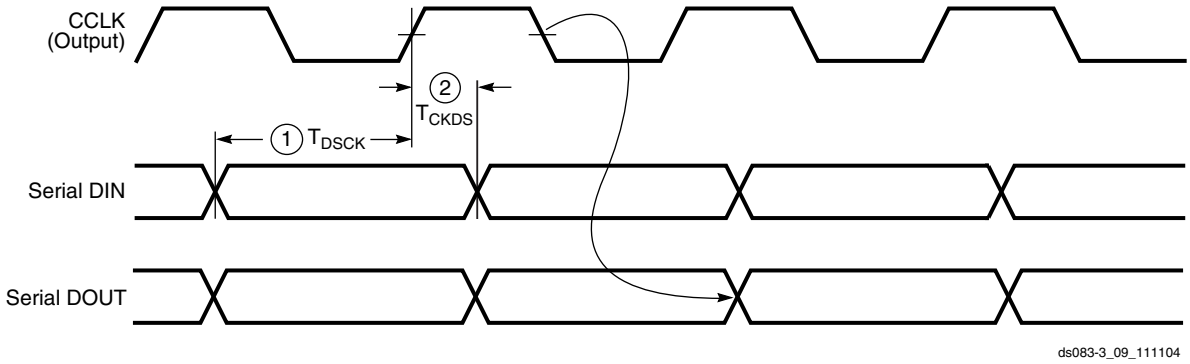

Figure 9: **Master Serial Mode Timing Sequence**

Table 50: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 8)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 9)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 56: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2	1.80/–0.44	1.85/–0.41	1.96/–0.43	ns
		XC2VP4	1.82/–0.53	1.83/–0.31	1.90/–0.29	ns
		XC2VP7	1.80/–0.34	1.81/–0.24	1.88/–0.19	ns
		XC2VP20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VPX20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VP30	1.75/–0.22	1.92/–0.26	1.99/–0.23	ns
		XC2VP40	2.25/–0.54	2.40/–0.56	2.49/–0.54	ns
		XC2VP50	2.93/–1.02	2.98/–0.93	3.00/–0.83	ns
		XC2VP70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VPX70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VP100	N/A	5.58/–2.35	5.60/–2.35	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L37N_1	G13				
1	IO_L37P_1	H13				
1	IO_L27N_1/VREF_1	J13	NC	NC		
1	IO_L27P_1	K13	NC	NC		
1	IO_L26N_1	D8	NC	NC		
1	IO_L26P_1	E8	NC	NC		
1	IO_L25N_1	F12	NC	NC		
1	IO_L25P_1	G12	NC	NC		
1	IO_L21N_1	G11	NC	NC		
1	IO_L21P_1	H11	NC	NC		
1	IO_L20N_1	C7	NC	NC		
1	IO_L20P_1	D7	NC	NC		
1	IO_L19N_1	E11	NC	NC		
1	IO_L19P_1	F11	NC	NC		
1	IO_L09N_1/VREF_1	J12				
1	IO_L09P_1	K12				
1	IO_L08N_1	D6				
1	IO_L08P_1	D5				
1	IO_L07N_1	E9				
1	IO_L07P_1	F9				
1	IO_L06N_1	J11				
1	IO_L06P_1	K11				
1	IO_L05_1/No_Pair	J10				
1	IO_L03N_1/VREF_1	G10				
1	IO_L03P_1	H10				
1	IO_L02N_1	G9				
1	IO_L02P_1	H9				
1	IO_L01N_1/VRP_1	E7				
1	IO_L01P_1/VRN_1	E6				
2	IO_L01N_2/VRP_2	D2				
2	IO_L01P_2/VRN_2	D1				
2	IO_L02N_2	F8				
2	IO_L02P_2	F7				
2	IO_L03N_2	E4				
2	IO_L03P_2	E3				
2	IO_L04N_2/VREF_2	E2				
2	IO_L04P_2	E1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L86N_7	U25				
7	IO_L85P_7	T32				
7	IO_L85N_7	T31				
7	IO_L60P_7	T30				
7	IO_L60N_7	T29				
7	IO_L59P_7	T28				
7	IO_L59N_7	T27				
7	IO_L58P_7	T33				
7	IO_L58N_7/VREF_7	R33				
7	IO_L57P_7	R32				
7	IO_L57N_7	R31				
7	IO_L56P_7	T26				
7	IO_L56N_7	T25				
7	IO_L55P_7	R34				
7	IO_L55N_7	P34				
7	IO_L54P_7	R29				
7	IO_L54N_7	R28				
7	IO_L53P_7	U24				
7	IO_L53N_7	T24				
7	IO_L52P_7	P32				
7	IO_L52N_7/VREF_7	P31				
7	IO_L51P_7	P30				
7	IO_L51N_7	P29				
7	IO_L50P_7	R26				
7	IO_L50N_7	R25				
7	IO_L49P_7	P33				
7	IO_L49N_7	N33				
7	IO_L48P_7	N32				
7	IO_L48N_7	N31				
7	IO_L47P_7	P28				
7	IO_L47N_7	P27				
7	IO_L46P_7	N34				
7	IO_L46N_7/VREF_7	M34				
7	IO_L45P_7	N30				
7	IO_L45N_7	N29				
7	IO_L44P_7	P26				
7	IO_L44N_7	P25				
7	IO_L43P_7	M32				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L75N_1/GCLK3P	C17		
1	IO_L75P_1/GCLK2S	B17		
1	IO_L74N_1/GCLK1P	L17		
1	IO_L74P_1/GCLK0S	K17		
1	IO_L73N_1	E17		
1	IO_L73P_1	D17		
1	IO_L69N_1/VREF_1	G17		
1	IO_L69P_1	F17		
1	IO_L68N_1	J17		
1	IO_L68P_1	H17		
1	IO_L67N_1	C16		
1	IO_L67P_1	B16		
1	IO_L66N_1/VREF_1	G16	NC	
1	IO_L66P_1	F16	NC	
1	IO_L57N_1/VREF_1	B15		
1	IO_L57P_1	A15		
1	IO_L56N_1	L16		
1	IO_L56P_1	K16		
1	IO_L55N_1	D16		
1	IO_L55P_1	C15		
1	IO_L54N_1	F15		
1	IO_L54P_1	E15		
1	IO_L53_1/No_Pair	H16		
1	IO_L50_1/No_Pair	G15		
1	IO_L49N_1	B14		
1	IO_L49P_1	A14		
1	IO_L48N_1	D14		
1	IO_L48P_1	C14		
1	IO_L47N_1	L15		
1	IO_L47P_1	K15		
1	IO_L46N_1	F14		
1	IO_L46P_1	E14		
1	IO_L45N_1/VREF_1	H14		
1	IO_L45P_1	G14		
1	IO_L44N_1	L14		
1	IO_L44P_1	K14		
1	IO_L43N_1	C13		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AF30		
N/A	GND	AB30		
N/A	GND	W30		
N/A	GND	T30		
N/A	GND	N30		
N/A	GND	J30		
N/A	GND	E30		
N/A	GND	A30		
N/A	GND	AP26		
N/A	GND	AK26		
N/A	GND	AB26		
N/A	GND	W26		
N/A	GND	T26		
N/A	GND	N26		
N/A	GND	E26		
N/A	GND	A26		
N/A	GND	AE25		
N/A	GND	K25		
N/A	GND	AP22		
N/A	GND	AK22		
N/A	GND	AF22		
N/A	GND	J22		
N/A	GND	E22		
N/A	GND	A22		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	R21		
N/A	GND	AA20		
N/A	GND	Y20		
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	R20		
N/A	GND	P20		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L03N_4/D2	AN10		
4	IO_L03P_4/D3	AM10		
4	IO_L05_4/No_Pair	AK10		
4	IO_L06N_4/VRP_4	AR10		
4	IO_L06P_4/VRN_4	AP10		
4	IO_L07N_4	AU10		
4	IO_L07P_4/VREF_4	AT10		
4	IO_L08N_4	AJ12		
4	IO_L08P_4	AJ13		
4	IO_L09N_4	AL10		
4	IO_L09P_4/VREF_4	AL11		
4	IO_L19N_4	AN11		
4	IO_L19P_4	AM11		
4	IO_L20N_4	AH13		
4	IO_L20P_4	AH14		
4	IO_L21N_4	AR11		
4	IO_L21P_4	AP11		
4	IO_L25N_4	AU11		
4	IO_L25P_4	AT11		
4	IO_L26N_4	AL14		
4	IO_L26P_4	AK14		
4	IO_L27N_4	AM12		
4	IO_L27P_4/VREF_4	AL12		
4	IO_L28N_4	AT12	NC	
4	IO_L28P_4	AR12	NC	
4	IO_L29N_4	AJ14	NC	
4	IO_L29P_4	AJ15	NC	
4	IO_L30N_4	AM13	NC	
4	IO_L30P_4	AL13	NC	
4	IO_L34N_4	AP12	NC	
4	IO_L34P_4	AN13	NC	
4	IO_L35N_4	AL15	NC	
4	IO_L35P_4	AK15	NC	
4	IO_L36N_4	AT13	NC	
4	IO_L36P_4/VREF_4	AR13	NC	
4	IO_L37N_4	AN14		
4	IO_L37P_4	AM14		
4	IO_L38N_4	AH15		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	AC22		
N/A	GND	AB22		
N/A	GND	AA22		
N/A	GND	Y22		
N/A	GND	W22		
N/A	GND	V22		
N/A	GND	U22		
N/A	GND	T22		
N/A	GND	AD21		
N/A	GND	AC21		
N/A	GND	AB21		
N/A	GND	AA21		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	B38		
N/A	GND	AW37		
N/A	GND	AV37		
N/A	GND	AU37		
N/A	GND	AT37		
N/A	GND	D37		
N/A	GND	C37		
N/A	GND	B37		
N/A	GND	A37		
N/A	GND	AU36		
N/A	GND	AT36		
N/A	GND	D36		
N/A	GND	C36		
N/A	GND	AM35		
N/A	GND	AH35		
N/A	GND	AD35		
N/A	GND	T35		
N/A	GND	M35		
N/A	GND	H35		

FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L01N_0/VRP_0		G34		
0	IO_L01P_0/VRN_0		H34		
0	IO_L02N_0		F34		
0	IO_L02P_0		E34		
0	IO_L03N_0		C34		
0	IO_L03P_0/VREF_0		D34		
0	IO_L05_0/No_Pair		K32		
0	IO_L06N_0		H33		
0	IO_L06P_0		J33		
0	IO_L07N_0		F33		
0	IO_L07P_0		G33		
0	IO_L08N_0		E33		
0	IO_L08P_0		D33		
0	IO_L09N_0		H32		
0	IO_L09P_0/VREF_0		J32		
0	IO_L19N_0		E32		
0	IO_L19P_0		F32		
0	IO_L20N_0		C33		
0	IO_L20P_0		C32		
0	IO_L21N_0		K31		
0	IO_L21P_0		L31		
0	IO_L25N_0		H31		
0	IO_L25P_0		J31		
0	IO_L26N_0		G31		
0	IO_L26P_0		F31		
0	IO_L27N_0		D31		
0	IO_L27P_0/VREF_0		E31		
0	IO_L28N_0		L30		
0	IO_L28P_0		M30		
0	IO_L29N_0		J30		
0	IO_L29P_0		K30		
0	IO_L30N_0		G30		
0	IO_L30P_0		H30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD17		BB15		
N/A	GNDA17		AY16		
N/A	TXPPAD17		BB16		
N/A	TXNPAD17		BB17		
N/A	VTTXPAD17		BA17		
N/A	AVCCAUXTX17		BA16		
N/A	AVCCAUXRX18		BA18		
N/A	VTRXPAD18		BA19		
N/A	RXNPAD18		BB18		
N/A	RXPPAD18		BB19		
N/A	GNDA18		AY21		
N/A	TXPPAD18		BB20		
N/A	TXNPAD18		BB21		
N/A	VTTXPAD18		BA21		
N/A	AVCCAUXTX18		BA20		
N/A	AVCCAUXRX19		BA22		
N/A	VTRXPAD19		BA23		
N/A	RXNPAD19		BB22		
N/A	RXPPAD19		BB23		
N/A	GNDA19		AY22		
N/A	TXPPAD19		BB24		
N/A	TXNPAD19		BB25		
N/A	VTTXPAD19		BA25		
N/A	AVCCAUXTX19		BA24		
N/A	AVCCAUXRX20		BA26		
N/A	VTRXPAD20		BA27		
N/A	RXNPAD20		BB26		
N/A	RXPPAD20		BB27		
N/A	GNDA20		AY27		
N/A	TXPPAD20		BB28		
N/A	TXNPAD20		BB29		
N/A	VTTXPAD20		BA29		
N/A	AVCCAUXTX20		BA28		
N/A	AVCCAUXRX21		BA30		
N/A	VTRXPAD21		BA31		
N/A	RXNPAD21		BB30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCAUX		AM11		
N/A	VCCAUX		AN33		
N/A	VCCAUX		AN10		
N/A	VCCAUX		AV39		
N/A	VCCAUX		AV4		
N/A	VCCAUX		AW38		
N/A	VCCAUX		AW22		
N/A	VCCAUX		AW21		
N/A	VCCAUX		AW5		
N/A	VCCAUX		AA42		
N/A	VCCAUX		AA41		
N/A	VCCAUX		AA2		
N/A	VCCAUX		AA1		
N/A	VCCAUX		Y42		
N/A	VCCAUX		Y1		
N/A	VCCAUX		L32		
N/A	VCCAUX		L11		
N/A	VCCAUX		K33		
N/A	VCCAUX		K10		
N/A	VCCAUX		E39		
N/A	VCCAUX		E4		
N/A	VCCAUX		D38		
N/A	VCCAUX		D22		
N/A	VCCAUX		D21		
N/A	VCCAUX		D5		
N/A	GND		AB38		
N/A	GND		AB35		
N/A	GND		AB32		
N/A	GND		AB26		
N/A	GND		AB25		
N/A	GND		AB24		
N/A	GND		AB23		
N/A	GND		AB22		
N/A	GND		AB21		
N/A	GND		AB20		
N/A	GND		AB19		