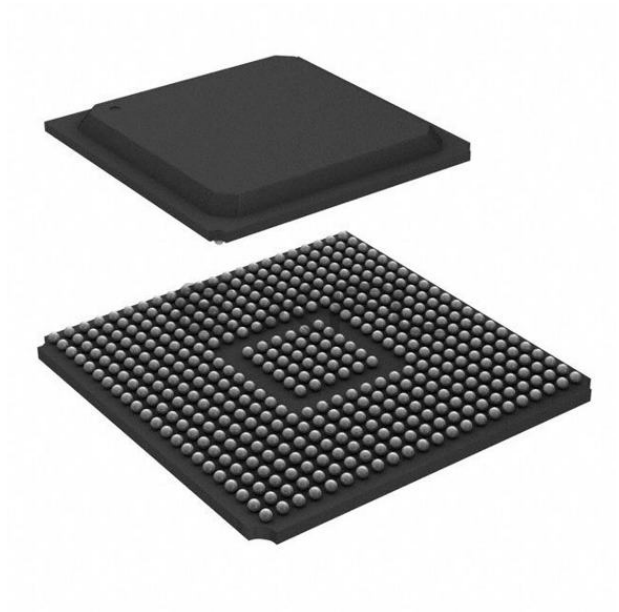

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	752
Number of Logic Elements/Cells	6768
Total RAM Bits	516096
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp4-5fgg456c

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

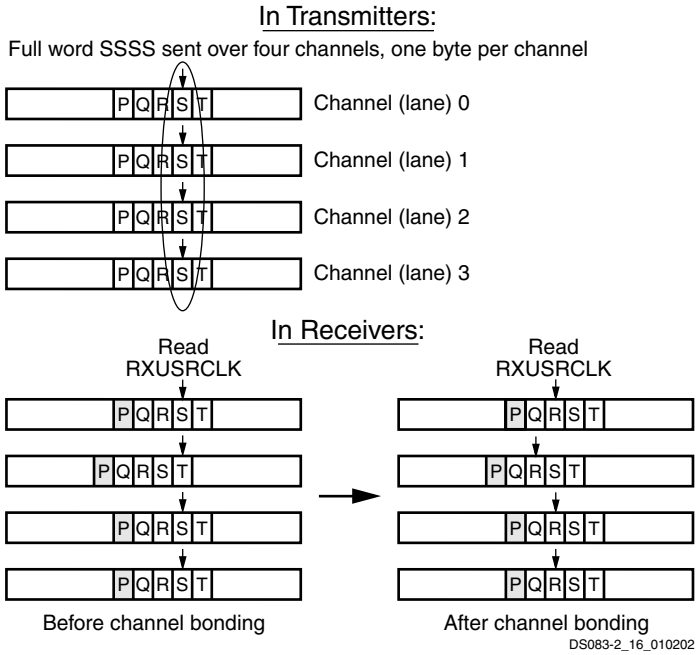

Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

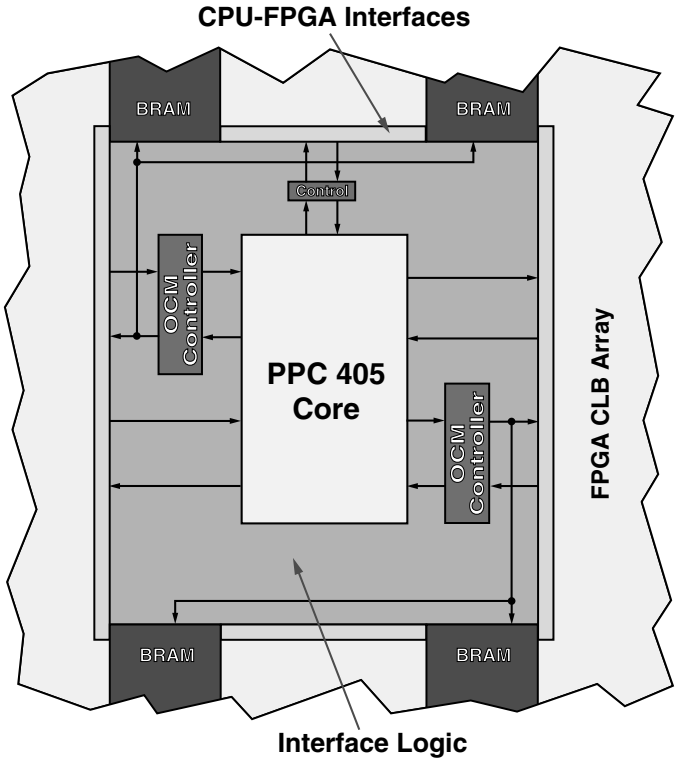

Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

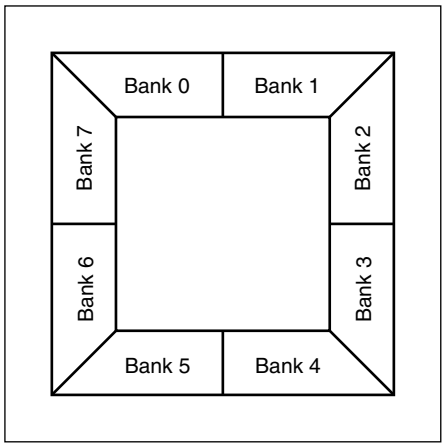

Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

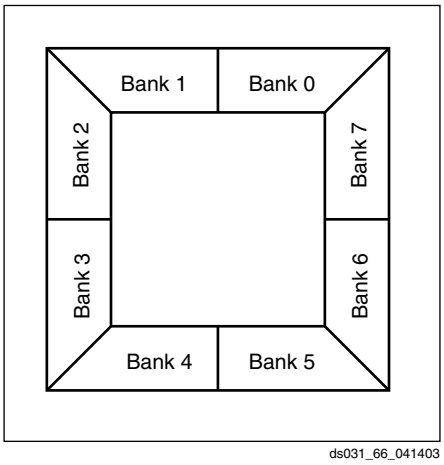

Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Virtex-II Pro X			Virtex-II Pro			Units
		Min	Typ	Max	Min	Typ	Max	
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	1.25			1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			2.0			V
I_{REF}	V_{REF} current per pin			10			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10			10	µA
C_{IN}	Input capacitance (sample-tested)			10			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)			150			150	µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample-tested)			150			150	µA
I_{BATT} (1)	Battery supply current	Note (2)			Note (2)			nA
$I_{CCAUXTX}$	Operating AVCCAUXTX supply current		115			60	105	mA
$I_{CCAUXRX}$	Operating AVCCAUXRX supply current		85			35	75	mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC-coupled		55			30		mA
	Operating I_{TTX} supply current when transmitter is DC-coupled	N/A	N/A	N/A		15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC-coupled		15			0		mA
	Operating I_{TRX} supply current when receiver is DC-coupled	N/A	N/A	N/A		15		
P_{CPU}	Power dissipation of PowerPC™ 405 processor block		0.9			0.9		mW/ MHz
P_{RXTX} (3)	Power dissipation of MGT @ 1.25 Gb/s per channel	N/A	N/A	N/A		230		mW
	Power dissipation of MGT @ 2.5 Gb/s per channel		290			310		mW
	Power dissipation of MGT @ 3.125 Gb/s per channel		310			350		mW
	Power dissipation of MGT @ 4.25 Gb/s per channel		450		N/A	N/A	N/A	mW
	Power dissipation of MGT @ 6.25 Gb/s per channel		525		N/A	N/A	N/A	mW

Notes:

1. Characterized, not tested.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

3. Total dissipation of fully operational PMA and PCS combined. This power is the average power supply dissipation per MGT. The averaging was done by simultaneously turning on all eight transceivers and dividing the total power supply dissipation by eight.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2).

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on V_{CCAUX}, V_{CCO}, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device											Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VPX20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VPX70	XC2VP100	
$I_{CCINTMIN}$	500	500	500	600	600	800	1050	1250	1700	1700	2200	mA
$I_{CCAUXMIN}$	250	250	250	250	250	250	250	250	250	250	250	mA
I_{CCOMIN}	100	100	100	100	100	100	100	100	100	100	100	mA

Notes:
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

Table 36: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.07	0.08	0.09	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.04	0.05	0.05	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.00	0.00	0.00	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.29	0.33	0.36	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.36	0.41	0.45	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.31	0.36	0.40	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.33	0.37	0.41	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.31	0.36	0.40	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.31	0.36	0.40	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{ILVPECL\_25}$	0.69	0.80	0.88	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.14	0.16	0.18	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.15	0.17	0.19	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.12	0.13	0.15	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.59	0.68	0.74	ns
GTL Plus	GTLP	T_{IGTLP}	0.63	0.72	0.79	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.59	0.68	0.75	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.59	0.68	0.75	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.57	0.66	0.72	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.58	0.67	0.74	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.57	0.65	0.72	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.55	0.63	0.69	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.56	0.64	0.70	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.57	0.65	0.71	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.62	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.64	0.73	0.81	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	–0.05	–0.05	–0.06	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.00	0.00	0.00	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.07	0.09	0.09	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.13	0.15	0.17	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.00	0.00	0.00	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.07	0.09	0.09	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.13	0.15	0.17	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.59	0.68	0.75	ns

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Measured as per PCI specification.
3. Measured as per PCI-X specification.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L58P_3	W6				
3	IO_L57N_3/VREF_3	Y3				
3	IO_L57P_3	Y4				
3	IO_L56N_3	W7				
3	IO_L56P_3	W8				
3	IO_L55N_3	Y6				
3	IO_L55P_3	Y7				
3	IO_L54N_3	AA2				
3	IO_L54P_3	AB2				
3	IO_L53N_3	W9				
3	IO_L53P_3	W10				
3	IO_L52N_3	AA3				
3	IO_L52P_3	AA4				
3	IO_L51N_3/VREF_3	AB1				
3	IO_L51P_3	AC1				
3	IO_L50N_3	Y9				
3	IO_L50P_3	Y10				
3	IO_L49N_3	AA5				
3	IO_L49P_3	AA6				
3	IO_L48N_3	AB3				
3	IO_L48P_3	AB4				
3	IO_L47N_3	AA7				
3	IO_L47P_3	AA8				
3	IO_L46N_3	AB5				
3	IO_L46P_3	AB6				
3	IO_L45N_3/VREF_3	AC2				
3	IO_L45P_3	AD2				
3	IO_L44N_3	AA9				
3	IO_L44P_3	AA10				
3	IO_L43N_3	AC3				
3	IO_L43P_3	AC4				
3	IO_L42N_3	AD1				
3	IO_L42P_3	AE1				
3	IO_L41N_3	AB7				
3	IO_L41P_3	AB8				
3	IO_L40N_3	AC6				
3	IO_L40P_3	AC7				
3	IO_L39N_3/VREF_3	AD3				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	V19				
N/A	GND	V20				
N/A	GND	V21				
N/A	GND	W1				
N/A	GND	W14				
N/A	GND	W15				
N/A	GND	W16				
N/A	GND	W17				
N/A	GND	W18				
N/A	GND	W19				
N/A	GND	W20				
N/A	GND	W21				
N/A	GND	W34				
N/A	GND	Y8				
N/A	GND	Y14				
N/A	GND	Y15				
N/A	GND	Y16				
N/A	GND	Y17				
N/A	GND	Y18				
N/A	GND	Y19				
N/A	GND	Y20				
N/A	GND	Y21				
N/A	GND	Y27				
N/A	GND	AA14				
N/A	GND	AA15				
N/A	GND	AA16				
N/A	GND	AA17				
N/A	GND	AA18				
N/A	GND	AA19				
N/A	GND	AA20				
N/A	GND	AA21				
N/A	GND	AC5				
N/A	GND	AC8				
N/A	GND	AC27				
N/A	GND	AC30				
N/A	GND	AE3				
N/A	GND	AE32				
N/A	GND	H23				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L21P_2	E6		
2	IO_L22N_2/VREF_2	F7		
2	IO_L22P_2	F8		
2	IO_L23N_2	M10		
2	IO_L23P_2	L10		
2	IO_L24N_2	G5		
2	IO_L24P_2	F5		
2	IO_L25N_2	F3		
2	IO_L25P_2	F4		
2	IO_L26N_2	M8		
2	IO_L26P_2	M9		
2	IO_L27N_2	F1		
2	IO_L27P_2	F2		
2	IO_L28N_2/VREF_2	G6		
2	IO_L28P_2	G7		
2	IO_L29N_2	M7		
2	IO_L29P_2	N8		
2	IO_L30N_2	G3		
2	IO_L30P_2	H4		
2	IO_L31N_2	G1		
2	IO_L31P_2	G2		
2	IO_L32N_2	N10		
2	IO_L32P_2	N11		
2	IO_L33N_2	H5		
2	IO_L33P_2	H6		
2	IO_L34N_2/VREF_2	H2		
2	IO_L34P_2	H3		
2	IO_L35N_2	N6		
2	IO_L35P_2	N7		
2	IO_L36N_2	K4		
2	IO_L36P_2	J4		
2	IO_L37N_2	J2		
2	IO_L37P_2	J3		
2	IO_L38N_2	P10		
2	IO_L38P_2	P11		
2	IO_L39N_2	K5		
2	IO_L39P_2	K6		
2	IO_L40N_2/VREF_2	L3		

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 12, XC2VP50 and XC2VP70 Virtex-II Pro devices are available in the FF1517 flip-chip fine-pitch BGA package. Following this table are the FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L01N_0/VRP_0	D31		
0	IO_L01P_0/VRN_0	E31		
0	IO_L02N_0	K30		
0	IO_L02P_0	J30		
0	IO_L03N_0	G30		
0	IO_L03P_0/VREF_0	H30		
0	IO_L05_0/No_Pair	K28		
0	IO_L06N_0	E30		
0	IO_L06P_0	F30		
0	IO_L07N_0	C30		
0	IO_L07P_0	D30		
0	IO_L08N_0	J29		
0	IO_L08P_0	K29		
0	IO_L09N_0	G29		
0	IO_L09P_0/VREF_0	H29		
0	IO_L19N_0	E29		
0	IO_L19P_0	F29		
0	IO_L20N_0	L28		
0	IO_L20P_0	L27		
0	IO_L21N_0	C29		
0	IO_L21P_0	D29		
0	IO_L25N_0	H28		
0	IO_L25P_0	J28		
0	IO_L26N_0	M27		
0	IO_L26P_0	M26		
0	IO_L27N_0	D28		
0	IO_L27P_0/VREF_0	E28		
0	IO_L28N_0	H27	NC	
0	IO_L28P_0	J27	NC	
0	IO_L29N_0	J26	NC	
0	IO_L29P_0	K26	NC	
0	IO_L30N_0	F28	NC	
0	IO_L30P_0	G27	NC	
0	IO_L34N_0	D27	NC	

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	AVCCAUXTX6	B23		
N/A	VTTXPAD6	B24		
N/A	TXNPAD6	A24		
N/A	TXPPAD6	A23		
N/A	GNDA6	C24		
N/A	RXPPAD6	A22		
N/A	RXNPAD6	A21		
N/A	VTRXPAD6	B22		
N/A	AVCCAUXRX6	B21		
N/A	AVCCAUXTX7	B18		
N/A	VTTXPAD7	B19		
N/A	TXNPAD7	A19		
N/A	TXPPAD7	A18		
N/A	GNDA7	C16		
N/A	RXPPAD7	A17		
N/A	RXNPAD7	A16		
N/A	VTRXPAD7	B17		
N/A	AVCCAUXRX7	B16		
N/A	AVCCAUXTX8	B14		
N/A	VTTXPAD8	B15		
N/A	TXNPAD8	A15		
N/A	TXPPAD8	A14		
N/A	GNDA8	C13		
N/A	RXPPAD8	A13		
N/A	RXNPAD8	A12		
N/A	VTRXPAD8	B13		
N/A	AVCCAUXRX8	B12		
N/A	AVCCAUXTX9	B10		
N/A	VTTXPAD9	B11		
N/A	TXNPAD9	A11		
N/A	TXPPAD9	A10		
N/A	GNDA9	C9		
N/A	RXPPAD9	A9		
N/A	RXNPAD9	A8		
N/A	VTRXPAD9	B9		
N/A	AVCCAUXRX9	B8		
N/A	AVCCAUXTX11	B6		
N/A	VTTXPAD11	B7		

FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L01N_0/VRP_0		G34		
0	IO_L01P_0/VRN_0		H34		
0	IO_L02N_0		F34		
0	IO_L02P_0		E34		
0	IO_L03N_0		C34		
0	IO_L03P_0/VREF_0		D34		
0	IO_L05_0/No_Pair		K32		
0	IO_L06N_0		H33		
0	IO_L06P_0		J33		
0	IO_L07N_0		F33		
0	IO_L07P_0		G33		
0	IO_L08N_0		E33		
0	IO_L08P_0		D33		
0	IO_L09N_0		H32		
0	IO_L09P_0/VREF_0		J32		
0	IO_L19N_0		E32		
0	IO_L19P_0		F32		
0	IO_L20N_0		C33		
0	IO_L20P_0		C32		
0	IO_L21N_0		K31		
0	IO_L21P_0		L31		
0	IO_L25N_0		H31		
0	IO_L25P_0		J31		
0	IO_L26N_0		G31		
0	IO_L26P_0		F31		
0	IO_L27N_0		D31		
0	IO_L27P_0/VREF_0		E31		
0	IO_L28N_0		L30		
0	IO_L28P_0		M30		
0	IO_L29N_0		J30		
0	IO_L29P_0		K30		
0	IO_L30N_0		G30		
0	IO_L30P_0		H30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L64N_5		AU24		
5	IO_L64P_5		AV24		
5	IO_L60N_5		AR24		
5	IO_L60P_5		AT24		
5	IO_L59N_5		AN24		
5	IO_L59P_5		AP24		
5	IO_L58N_5		AL24		
5	IO_L58P_5		AM24		
5	IO_L57N_5/VREF_5		AY26		
5	IO_L57P_5		AY25		
5	IO_L56N_5		AV25		
5	IO_L56P_5		AV26		
5	IO_L55N_5		AR25		
5	IO_L55P_5		AT25		
5	IO_L54N_5		AM25		
5	IO_L54P_5		AN25		
5	IO_L53_5/No_Pair		AW26		
5	IO_L50_5/No_Pair		AW27		
5	IO_L49N_5		AT26		
5	IO_L49P_5		AU26		
5	IO_L48N_5		AP26		
5	IO_L48P_5		AR26		
5	IO_L47N_5		AN26		
5	IO_L47P_5		AM26		
5	IO_L46N_5		AL26		
5	IO_L46P_5		AL25		
5	IO_L45N_5/VREF_5		AU27		
5	IO_L45P_5		AV27		
5	IO_L44N_5		AT27		
5	IO_L44P_5		AR27		
5	IO_L43N_5		AN27		
5	IO_L43P_5		AP27		
5	IO_L39N_5		AL27		
5	IO_L39P_5		AM27		
5	IO_L38N_5		AY28		
5	IO_L38P_5		AY29		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	VCCO_5	AL30	
5	VCCO_5	AW29	
5	VCCO_5	AR29	
5	VCCO_5	AJ26	
5	VCCO_5	AW25	
5	VCCO_5	AR25	
5	VCCO_5	AJ25	
5	VCCO_5	AH25	
5	VCCO_5	AJ24	
5	VCCO_5	AH24	
5	VCCO_5	AJ23	
5	VCCO_5	AH23	
5	VCCO_5	AJ22	
5	VCCO_5	AH22	
4	VCCO_4	AJ21	
4	VCCO_4	AH21	
4	VCCO_4	AJ20	
4	VCCO_4	AH20	
4	VCCO_4	AJ19	
4	VCCO_4	AH19	
4	VCCO_4	AW18	
4	VCCO_4	AR18	
4	VCCO_4	AJ18	
4	VCCO_4	AH18	
4	VCCO_4	AJ17	
4	VCCO_4	AW14	
4	VCCO_4	AR14	
4	VCCO_4	AL13	
4	VCCO_4	AW10	
3	VCCO_3	AG15	
3	VCCO_3	AF15	
3	VCCO_3	AE15	
3	VCCO_3	AD15	
3	VCCO_3	AC15	
3	VCCO_3	AB15	
3	VCCO_3	AH14	
3	VCCO_3	AG14	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	AG26	
N/A	VCCINT	AF26	
N/A	VCCINT	U26	
N/A	VCCINT	T26	
N/A	VCCINT	R26	
N/A	VCCINT	AG25	
N/A	VCCINT	T25	
N/A	VCCINT	AG24	
N/A	VCCINT	T24	
N/A	VCCINT	AG23	
N/A	VCCINT	T23	
N/A	VCCINT	AG22	
N/A	VCCINT	T22	
N/A	VCCINT	AG21	
N/A	VCCINT	T21	
N/A	VCCINT	AG20	
N/A	VCCINT	T20	
N/A	VCCINT	AG19	
N/A	VCCINT	T19	
N/A	VCCINT	AG18	
N/A	VCCINT	T18	
N/A	VCCINT	AH17	
N/A	VCCINT	AG17	
N/A	VCCINT	AF17	
N/A	VCCINT	U17	
N/A	VCCINT	T17	
N/A	VCCINT	R17	
N/A	VCCINT	AJ16	
N/A	VCCINT	AH16	
N/A	VCCINT	AG16	
N/A	VCCINT	AF16	
N/A	VCCINT	AE16	
N/A	VCCINT	AD16	
N/A	VCCINT	AC16	
N/A	VCCINT	AB16	
N/A	VCCINT	AA16	
N/A	VCCINT	Y16	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
08/14/02	2.0	Added package and pinout information for new devices.
08/27/02	2.1	• Updated SelectIO-Ultra information in Table 4. (Table deleted in v2.3.) • Corrected direction for RXNPAD and TXPPAD in Table 4 (formerly Table 5).
09/27/02	2.2	Corrected Table 2 and Table 3 entries for XC2VP30, FF1152 package, maximum I/Os from 692 to 644.
11/20/02	2.3	Added Number of Differential Pairs data to Table 3. Removed former Table 4.
12/03/02	2.4	Corrections in Table 4: • Reclassified GCLKx (S/P) pins as Input/Output, since these pins can be used as normal I/Os if not used as clocks. • Added cautionary note to PWRDWN_B pin, indicating that this function is not supported.
01/20/03	2.5	Added and removed package/pinout information for existing devices: • In Table 1, added FG676 package information. • In Table 3, added FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • In Table 12, removed FF1517 package option for XC2VP40. • Added FG676 package pinouts (Table 7) for XC2VP20, XC2VP30, and XC2VP40. • Added package diagram (Figure 3) for FG676 package.
05/19/03	2.5.1	• Added section **BREFCLK Pin Definitions**, page 5. • Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	2.5.3	• Added notation of "open-drain" to TDO pin in Table 4. • The final GND pin in each of six pinout tables was inadvertently deleted in v2.5.1. This revision restores the deleted GND pins as follows: - Pin A1, Table 6, page 16 (FG456) - Pin AF26, Table 7, page 30 (FG676) - Pin AN34, Table 10, page 98 (FF1152) - Pin E1, Table 11, page 130 (FF1148) - Pin C38, Table 12, page 162 (FF1517) - Pin E1, Table 14, page 253 (FF1696)
08/25/03	2.5.5	• Table 4: Deleted Note 2, obsolete. There is only one GNDA pin per MGT. • Table 4: Deleted pins ALT_VRP and ALT_VRN. Not used in Virtex-II Pro FPGAs.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 4, signal descriptions column: - For signals TDI, TMS, and TCK, added: Pins are 3.3V-compatible. - For signals M2, M1, M0, added: Tie to 3.3V only with 100Ω series resistor. No toggling during or after configuration. - For signal TDO, added: No internal pull-up. External pull-up to 3.3V OK with resistor greater than 200Ω.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-4 (Module 4 of Virtex-II Pro X data sheet). Added data on available Pb-free packages and updated package diagrams for affected devices.