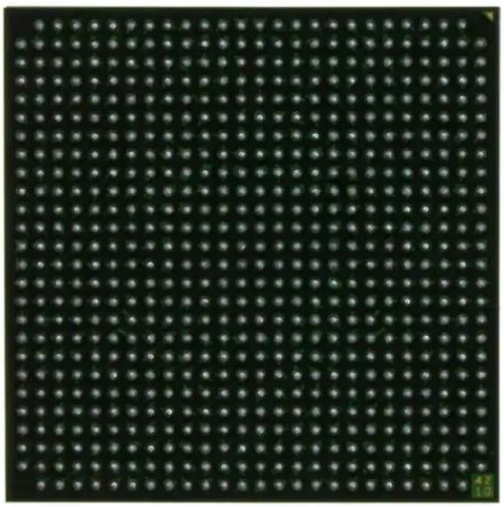

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 752 |
| Number of Logic Elements/Cells | 6768 |
| Total RAM Bits | 516096 |
| Number of I/O | 348 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA, FCBGA |
| Supplier Device Package | 672-FCBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp4-6ffg672c |

The Trace port provides instruction execution trace information to an external trace tool. The PPC405 core is capable of back trace and forward trace. Back trace is the tracing of instructions prior to a debug event while forward trace is the tracing of instructions after a debug event.

The processor JTAG port and the FPGA JTAG port can be accessed independently, or the two can be programmatically linked together and accessed via the dedicated FPGA JTAG pins.

For detailed information on the PPC405 JTAG interface, please refer to the "JTAG Interface" section of the **PowerPC 405 Processor Block Reference Guide**

## CoreConnect™ Bus Architecture

The Processor Block is compatible with the CoreConnect™ bus architecture. Any CoreConnect compliant cores including Xilinx soft IP can integrate with the Processor Block through this high-performance bus architecture implemented on FPGA fabric.

The CoreConnect architecture provides three buses for interconnecting Processor Blocks, Xilinx soft IP, third party IP, and custom logic, as shown in Figure 15:

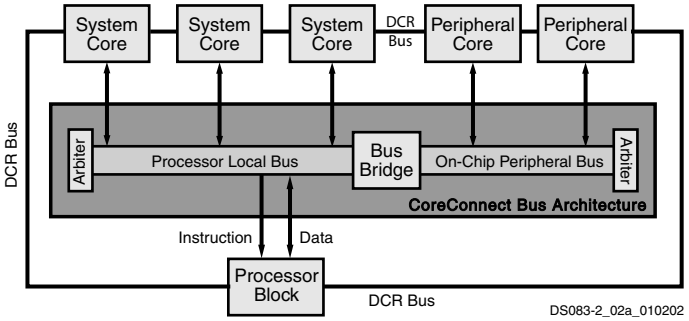


*Figure 15:* **CoreConnect Block Diagram**

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) bus

High-performance peripherals connect to the high-bandwidth, low-latency PLB. Slower peripheral cores connect to the OPB, which reduces traffic on the PLB, resulting in greater overall system performance.

For more information, refer to:
**http://www-3.ibm.com/chips/techlib/techlib.nfs/productfamilies/CoreConnect_Bus_Architecture/**

# Functional Description: Embedded PowerPC 405 Core

This section offers a brief overview of the various functional blocks shown in Figure 16.

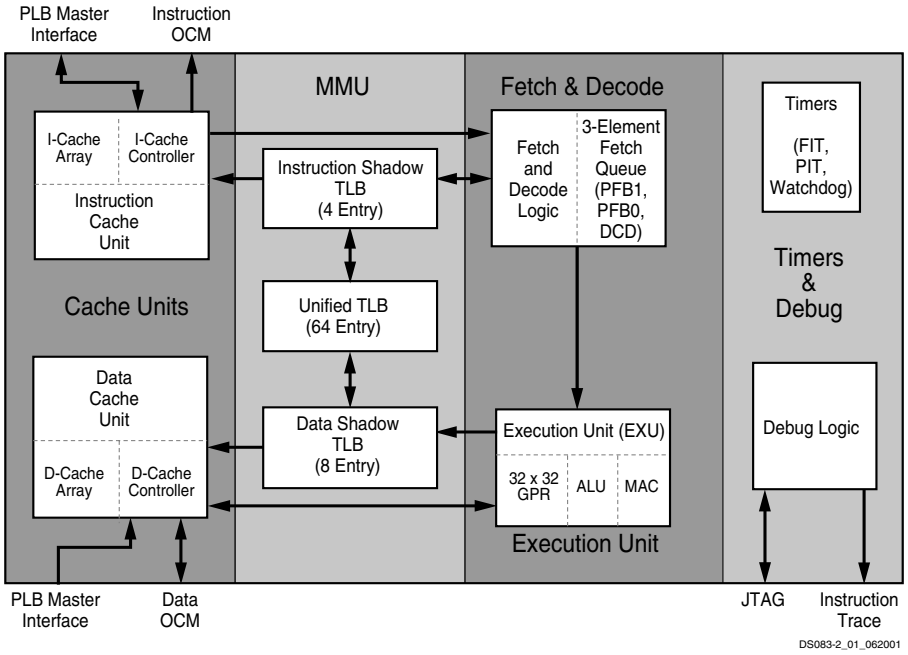


*Figure 16:* **Embedded PPC405 Core Block Diagram**

## Embedded PPC405 Core

The embedded PPC405 core is a 32-bit Harvard architecture processor. Figure 16 illustrates its functional blocks:

- Cache units
- Memory Management unit
- Fetch Decode unit

*Table 11:* **LVCMOS Programmable Currents (Sink and Source)**

| SelectIO-Ultra | Programmable Current (Worst-Case Guaranteed Minimum) | | | | | | |
|---|---|---|---|---|---|---|---|
| LVTTL | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS33 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS25 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS18 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | n/a |
| LVCMOS15 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | n/a |

Figure 23 shows the SSTL2, SSTL18, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

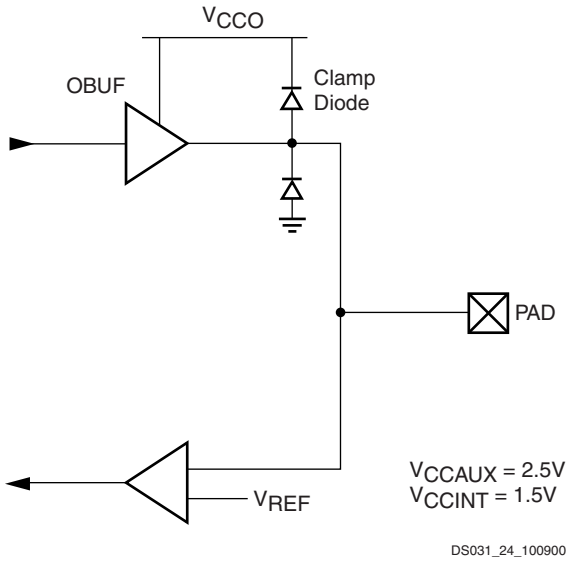


*Figure 23:* **SSTL or HSTL SelectIO-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II Pro uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set High, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set Low, the pull-up resistors are activated on user I/O pins.

All Virtex-II Pro IOBs (except RocketIO transceiver pins) support IEEE 1149.1 and IEEE 1532 compatible Boundary-Scan testing.

### *Input Path*

The Virtex-II Pro IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II Pro device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, $V_{REF}$. The need to supply $V_{REF}$ imposes constraints on which standards can be used in the same bank. See I/O banking description.

### *Output Path*

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied $V_{CCO}$ voltage. The need to supply $V_{CCO}$ imposes constraints on which standards can be used in the same bank. See I/O banking description.

### *I/O Banking*

Some of the I/O standards described above require $V_{CCO}$ and $V_{REF}$ voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 24 and Figure 25. Each bank has multiple $V_{CCO}$ pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

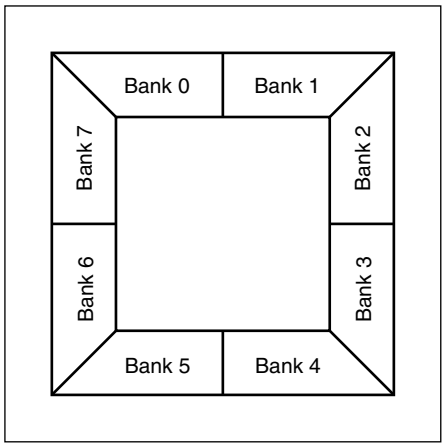


*Figure 24:* **I/O Banks: Wire-Bond Packages (FG) Top View**

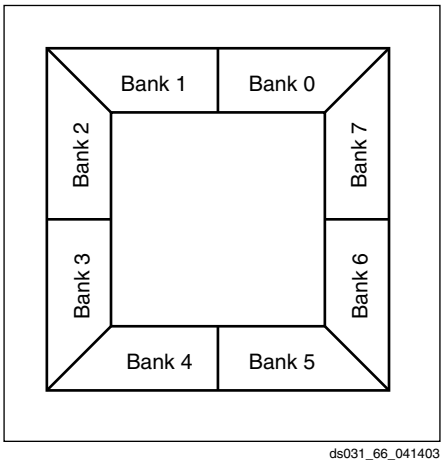


*Figure 25:* **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage ($V_{REF}$), and certain user-I/O pins are automatically configured as $V_{REF}$ inputs. Approximately one in six of the I/O pins in the bank assume this role.

$V_{REF}$ pins within a bank are interconnected internally, thus only one $V_{REF}$ voltage can be used within each bank. However, for correct operation, all $V_{REF}$ pins in the bank must be connected to the external reference voltage source.

The $V_{CCO}$ and the $V_{REF}$ pins for each bank appear in the device pinout tables. Within a given package, the number of $V_{REF}$ and $V_{CCO}$ pins can vary depending on the size of device. In larger devices, more I/O pins convert to $V_{REF}$ pins. Since these are always a superset of the $V_{REF}$ pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All $V_{REF}$ pins for the largest device anticipated must be connected to the $V_{REF}$ voltage and not used for I/O. In smaller devices, some $V_{CCO}$ pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to $V_{CCO}$ to permit migration to a larger device.

### *Rules for Combining I/O Standards in the Same Bank*

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output $V_{CCO}$ requirement can be combined in the same bank.
   *Compatible example:*
   SSTL2_I and LVDS_25 outputs
   *Incompatible example:*
   SSTL2_I (output $V_{CCO}$ = 2.5V) and
   LVCMOS33 (output $V_{CCO}$ = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input $V_{CCO}$ and input $V_{REF}$ requirements can be combined in the same bank.
   *Compatible example:*
   LVCMOS15 and HSTL_IV inputs
   *Incompatible example:*
   LVCMOS15 (input $V_{CCO}$ = 1.5V) and
   LVCMOS18 (input $V_{CCO}$ = 1.8V) inputs
   *Incompatible example:*
   HSTL_I_DCI_18 ($V_{REF}$ = 0.9V) and
   HSTL_IV_DCI_18 ($V_{REF}$ = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input $V_{CCO}$ and output $V_{CCO}$ requirement can be combined in the same bank.
   *Compatible example:*
   LVDS_25 output and HSTL_I input
   *Incompatible example:*
   LVDS_25 output (output $V_{CCO}$ = 2.5V) and
   HSTL_I_DCI_18 input (input $V_{CCO}$ = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      *Incompatible example:*
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      *Incompatible example:*
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

*Table 15:* **SelectIO-Ultra Differential Buffers With On-Chip Termination**

| I/O Standard Description | IOSTANDARD Attribute | |
|---|---|---|
| | External Termination | On-Chip Termination |
| LVDS 2.5V | LVDS_25 | LVDS_25_DCI |
| LVDS Extended 2.5V | LVDSEXT_25 | LVDSEXT_25_DCI |

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

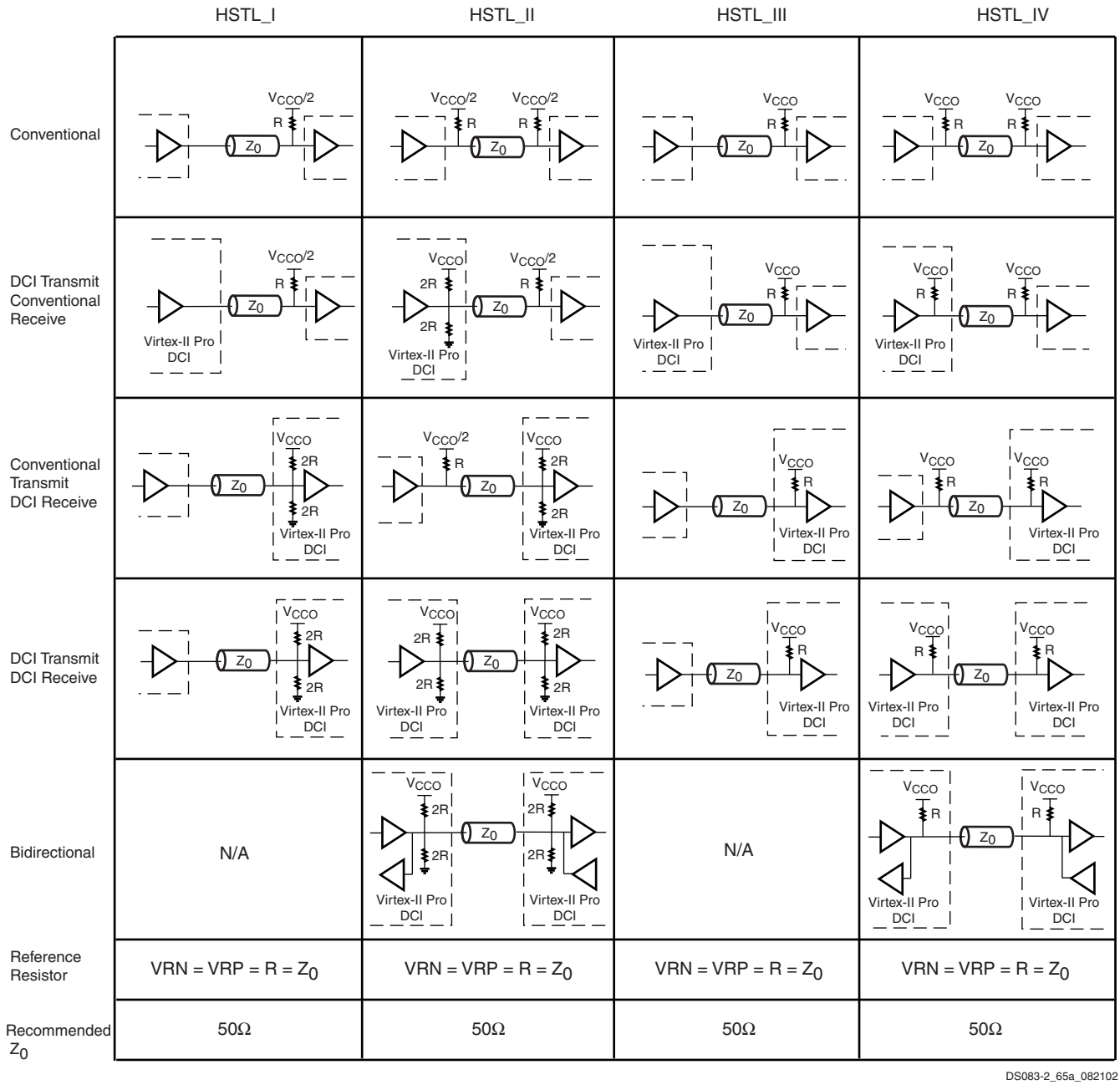


*Figure 28:* **HSTL DCI Usage Examples**

### *3-State Buffers*

#### Introduction

Each Virtex-II Pro CLB contains two 3-state drivers (TBUFs) that can drive on-chip buses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 45. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state buses.

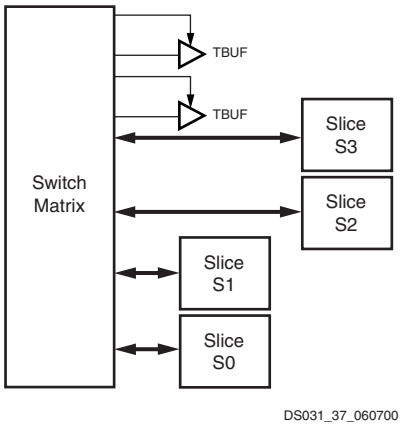


*Figure 45:* **Virtex-II Pro 3-State Buffers**

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

#### Locations / Organization

Four horizontal routing resources per CLB are provided for on-chip 3-state buses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 46. The switch matrices corresponding to SelectRAM+ memory and multiplier or I/O blocks are skipped.

#### Number of 3-State Buffers

Table 18 shows the number of 3-state buffers available in each Virtex-II Pro device. The number of 3-state buffers is twice the number of CLB elements.

*Table 18:* **Virtex-II Pro 3-State Buffers**

| Device | 3-State Buffers per Row | Total Number of 3-State Buffers |
|---|---|---|
| XC2VP2 | 44 | 704 |
| XC2VP4 | 44 | 1,504 |
| XC2VP7 | 68 | 2,464 |
| XC2VP20 | 92 | 4,640 |
| XC2VPX20 | 92 | 4,896 |
| XC2VP30 | 92 | 6,848 |
| XC2VP40 | 116 | 9,696 |
| XC2VP50 | 140 | 11,808 |
| XC2VP70 | 164 | 16,544 |
| XC2VPX70 | 164 | 16,544 |
| XC2VP100 | 188 | 22,048 |

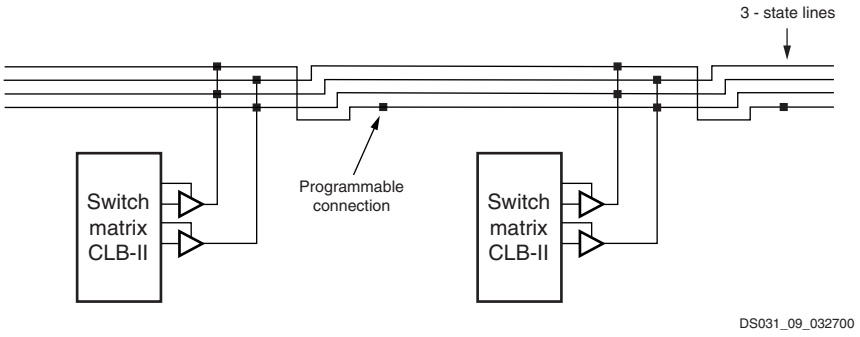


*Figure 46:* **3-State Buffer Connection to Horizontal Lines**

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 27.

*Table 27:* **DCM Status Pins**

| Status Pin | Function |
|---|---|
| 0 | Phase Shift Overflow |
| 1 | CLKIN Stopped |
| 2 | CLKFX Stopped |
| 3 | N/A |
| 4 | N/A |
| 5 | N/A |
| 6 | N/A |
| 7 | N/A |

### Clock De-skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, connect the CLKFB input to CLK0. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

### Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$\mathrm{FREQ}_{\mathrm{CLKFX}} = (M/D) \bullet \mathrm{FREQ}_{\mathrm{CLKIN}}$$

where $M$ and $D$ are two integers. Specifications for $M$ and $D$ are provided under **DCM Timing Parameters** in Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics. By default, $M = 4$ and $D = 1$, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles, with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode. See Table 28 for more details.

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

*Table 28:* **CLKDV Duty Cycle for Non-integer Divides**

| CLKDV_DIVIDE | Duty Cycle |
|---|---|
| 1.5 | 1/3 |
| 2.5 | 2/5 |
| 3.5 | 3/7 |
| 4.5 | 4/9 |
| 5.5 | 5/11 |
| 6.5 | 6/13 |
| 7.5 | 7/15 |

### Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 63 illustrates the effects of fine-phase shifting. For more information on DCM features, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 29 lists fine-phase shifting control pins, when used in variable mode.

*Table 29:* **Fine Phase Shifting Control Pins**

| Control Pin | Direction | Function |
|---|---|---|
| PSINCDEC | In | Increment or decrement |
| PSEN | In | Enable ± phase shift |
| PSCLK | In | Clock for phase shift |
| PSDONE | Out | Active when completed |

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

## Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

### Virtex-II Pro DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description[1] | | Virtex-II Pro X | Virtex-II Pro | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | –0.5 to 1.6 | | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | –0.5 to 3.0 | | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | | –0.5 to 3.75 | | V |
| $V_{BATT}$ | Key memory battery backup supply | | –0.5 to 4.05 | | V |
| $V_{REF}$ | Input reference voltage | | –0.3 to 3.75 | | V |
| $V_{IN}$ | 3.3V I/O input voltage relative to GND (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| $V_{TS}$ | Voltage applied to 3-state 3.3V output (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| AVCCAUXRX | Receive auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 2.0 | –0.5 to 3.0 | V |
| AVCCAUXTX | Transmit auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TRX}$ | Terminal receive supply voltage relative to GND | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TTX}$ | Terminal transmit supply voltage relative to GND | | –0.5 to 1.6 | –0.5 to 3.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | | °C |
| $T_{SOL}$ | Maximum soldering temperature[2] | All regular FG/FF flip-chip packages | +220 | | °C |
| | | Pb-free FGG256 wire-bond package | N/A | +260 | °C |
| | | Pb-free FGG456 and FGG676 wire-bond packages | N/A | +250 | °C |
| $T_J$ | Maximum junction temperature[2] | | +125 | | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

## IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

*Table 36:* **IOB Input Switching Characteristics Standard Adjustments**

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | $T_{ILVTTL}$ | 0.07 | 0.08 | 0.09 | ns |
| LVCMOS (Low-Voltage CMOS ), 3.3V | LVCMOS33 | $T_{ILVCMOS33}$ | 0.04 | 0.05 | 0.05 | ns |
| LVCMOS, 2.5V | LVCMOS25 | $T_{ILVCMOS25}$ | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS, 1.8V | LVCMOS18 | $T_{ILVCMOS18}$ | 0.29 | 0.33 | 0.36 | ns |
| LVCMOS, 1.5V | LVCMOS15 | $T_{ILVCMOS15}$ | 0.36 | 0.41 | 0.45 | ns |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | $T_{ILVDS\_25}$ | 0.31 | 0.36 | 0.40 | ns |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | $T_{ILVDSEXT\_25}$ | 0.33 | 0.37 | 0.41 | ns |
| ULVDS (Ultra LVDS), 2.5V | ULVDS_25 | $T_{IULVDS\_25}$ | 0.31 | 0.36 | 0.40 | ns |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | $T_{IBLVDS\_25}$ | 0.00 | 0.00 | 0.00 | ns |
| LDT (HyperTransport), 2.5V | LDT_25 | $T_{ILDT\_25}$ | 0.31 | 0.36 | 0.40 | ns |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V | LVPECL_25 | $T_{ILVPECL\_25}$ | 0.69 | 0.80 | 0.88 | ns |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 | $T_{IPCI33\_3}$ | 0.14 | 0.16 | 0.18 | ns |
| PCI, 66 MHz, 3.3V | PCI66_3 | $T_{IPCI66\_3}$ | 0.15 | 0.17 | 0.19 | ns |
| PCI-X, 133 MHz, 3.3V | PCIX | $T_{IPCIX}$ | 0.12 | 0.13 | 0.15 | ns |
| GTL (Gunning Transceiver Logic) | GTL | $T_{IGTL}$ | 0.59 | 0.68 | 0.74 | ns |
| GTL Plus | GTLP | $T_{IGTLP}$ | 0.63 | 0.72 | 0.79 | ns |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | $T_{IHSTL\_I}$ | 0.59 | 0.68 | 0.75 | ns |
| HSTL, Class II | HSTL_II | $T_{IHSTL\_II}$ | 0.59 | 0.68 | 0.75 | ns |
| HSTL, Class III | HSTL_III | $T_{IHSTL\_III}$ | 0.57 | 0.66 | 0.72 | ns |
| HSTL, Class IV | HSTL_IV | $T_{IHSTL\_IV}$ | 0.58 | 0.67 | 0.74 | ns |
| HSTL, Class I, 1.8V | HSTL_I_18 | $T_{IHSTL\_I\_18}$ | 0.57 | 0.65 | 0.72 | ns |
| HSTL, Class II, 1.8V | HSTL_II_18 | $T_{IHSTL\_II\_18}$ | 0.55 | 0.63 | 0.69 | ns |
| HSTL, Class III, 1.8V | HSTL_III_18 | $T_{IHSTL\_III\_18}$ | 0.56 | 0.64 | 0.70 | ns |
| HSTL, Class IV, 1.8V | HSTL_IV_18 | $T_{IHSTL\_IV\_18}$ | 0.57 | 0.65 | 0.71 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | $T_{ISSTL18\_I}$ | 0.62 | 0.72 | 0.79 | ns |
| SSTL, Class II, 1.8V | SSTL18_II | $T_{ISSTL18\_II}$ | 0.64 | 0.73 | 0.81 | ns |
| SSTL, Class I, 2.5V | SSTL2_I | $T_{ISSTL2\_I}$ | 0.62 | 0.72 | 0.79 | ns |
| SSTL, Class II, 2.5V | SSTL2_II | $T_{ISSTL2\_II}$ | 0.64 | 0.73 | 0.81 | ns |
| LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33 | $T_{ILVDCI\_33}$ | –0.05 | –0.05 | –0.06 | ns |
| LVDCI, 2.5V | LVDCI_25 | $T_{ILVDCI\_25}$ | 0.00 | 0.00 | 0.00 | ns |
| LVDCI, 1.8V | LVDCI_18 | $T_{ILVDCI\_18}$ | 0.07 | 0.09 | 0.09 | ns |
| LVDCI, 1.5V | LVDCI_15 | $T_{ILVDCI\_15}$ | 0.13 | 0.15 | 0.17 | ns |
| LVDCI, 2.5V, Half-Impedance | LVDCI_DV2_25 | $T_{ILVDCI\_DV2\_25}$ | 0.00 | 0.00 | 0.00 | ns |
| LVDCI, 1.8V, Half-Impedance | LVDCI_DV2_18 | $T_{ILVDCI\_DV2\_18}$ | 0.07 | 0.09 | 0.09 | ns |
| LVDCI, 1.5V, Half-Impedance | LVDCI_DV2_15 | $T_{ILVDCI\_DV2\_15}$ | 0.13 | 0.15 | 0.17 | ns |
| HSLVDCI (High-Speed Low-Voltage DCI), 1.5V | HSLVDCI_15 | $T_{IHSLVDCI\_15}$ | 0.59 | 0.68 | 0.75 | ns |

## I/O Standard Adjustment Measurement Methodology

### *Input Delay Measurements*

Table 39 shows the test setup parameters used for measuring Input standard adjustments (see Table 36, page 25).

*Table 39:* **Input Delay Measurement Methodology**

| Description | IOSTANDARD Attribute | $V_L$ (1,2) | $V_H$ (1,2) | $V_{MEAS}$ (1,4,5) | $V_{REF}$ (1,3,5) |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | 0 | 3.3 | 1.65 | – |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 0 | 3.3 | 1.65 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 | Per PCI Specification | | | – |
| PCI, 66 MHz, 3.3V | PCI66_3 | Per PCI Specification | | | – |
| PCI-X, 133 MHz, 3.3V | PCIX | Per PCI-X Specification | | | – |
| GTL (Gunning Transceiver Logic) | GTL | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.80 |
| GTL Plus | GTLP | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.0 |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL, Class III & IV | HSTL_III, HSTL_IV | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class III & IV, 1.8V | HSTL_III_18, HSTL_IV_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 1.08 |
| SSTL (Stub Terminated Tnscvr Logic), Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.9 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| ULVDS (Ultra LVDS), 2.5V | ULVDS_25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LDT (HyperTransport), 2.5V | LDT_25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V | LVPECL_25 | 1.15 – 0.3 | 1.15 + 0.3 | 1.15 | |

**Notes:**

1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$ and $V_H$.
3. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical. See ***Virtex-II Pro Platform FPGA User Guide*** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 6.

| Date | Version | Revision |
|---|---|---|
| 12/05/03 (cont'd) | 3.0 (cont'd) | • Non-speedsfile parameter values added or updated:<br>• Table 3: $I_{BATT}$.<br>• Table 4: For XC2VP100, $I_{CCINTQ}$, $I_{CCOQ}$, and $I_{CCAUXQ}$.<br>• Table 5: For XC2VP100, $I_{CCINTMIN}$.<br>• Table 17: $T_{CPWL}$ and $T_{CPWH}$.<br>• Table 25: Added explanatory footnote to $T_{RXLAT}$ (MGT receiver latency) max value.<br>• Table 57: Added Footnote (3) regarding use of CLKIN_DIVIDE_BY_2 attribute. |
| 02/19/04 | 3.1 | • Updated time and frequency parameters as per speedsfile **v1.85**.<br>• Table 2, Recommended Operating Conditions: Revised Footnotes (4) and (6).<br>• Table 4, Quiescent Supply Current: Added Footnote (1) and updated Typical parameters.<br>• Table 10, LVPECL DC Specifications: Added parameter values for Maximum Differential Input Voltage (LVPECL).<br>• Table 14, Register-to-Register Performance: Removed reference to a number of designs for which test data is no longer provided.<br>• Table 16, Processor Clocks Absolute AC Characteristics: Added Footnote (1) referring to XAPP755.<br>• Added Table 41, Clock Distribution Switching Characteristics.<br>• Revised section Configuration Timing, page 39 through page 41, and JTAG Test Access Port Switching Characteristics, page 42, with improved timing diagrams, parameter tables, and organization.<br>• Table 50, Master/Slave Serial Mode Timing Characteristics, and Table 51, SelectMAP Mode Write Timing Characteristics: Added parameter $F_{CC\_STARTUP}$.<br>• Table 51, SelectMAP Mode Write Timing Characteristics: Broke out $T_{SMDCC}/T_{SMCCD}$, DATA[0:7] setup/hold time, by device, and added new parameter specifications for XC2VP70 and XC2VP100 devices.<br>• Table 57, Operating Frequency Ranges: Added callouts for existing Footnote (3) to the four CLKIN parameters. Added new Footnote (4) to the four CLKIN parameters. Added new Footnote (5) to CLK2X, CLK2X180. Added new Footnote (6) to CLK2X, CLK2X180; CLK0, CLK180; and CLKIN (using DLL outputs). |
| 03/09/04 | 3.1.1 | • Recompiled for backward compatibility with Acrobat 4 and above. No content changes. |
| 04/22/04 | 3.2 | • Table 2, Recommended Operating Conditions: Corrected VTTX/VTRX lower voltage limit from 1.8V to 1.6V.<br>• Table 5, Power-On Current for Virtex-II Pro Devices: Added Footnote (2) stating that listed $I_{CCOMIN}$ values apply to the entire device (all banks).<br>• Table 40, Output Delay Measurement Methodology: Corrected $V_{MEAS}$ for LVTTL from 1.4V to 1.65V.<br>• Table 57, Operating Frequency Ranges: Corrected CLKOUT_FREQ_1X_LF_MAX and CLKIN_FREQ_DLL_LF_MAX for -7 devices from 210 MHz to 270 MHz.<br>• Table 65, Package Skew: Removed XC2VP40FF1517. |
| 06/30/04 | 4.0 | Merged in DS110-3 (Module 3 of Virtex-II Pro X data sheet). This merge added numerous previously unpublished RocketIO X MGT parameters. Specifications in this revision are from speedsfile **v1.86**. |

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| N/A | GND | R15 | | | |
| N/A | GND | R16 | | | |
| N/A | GND | R17 | | | |
| N/A | GND | T11 | | | |
| N/A | GND | T12 | | | |
| N/A | GND | T13 | | | |
| N/A | GND | T14 | | | |
| N/A | GND | T15 | | | |
| N/A | GND | T16 | | | |
| N/A | GND | U10 | | | |
| N/A | GND | U12 | | | |
| N/A | GND | U13 | | | |
| N/A | GND | U14 | | | |
| N/A | GND | U15 | | | |
| N/A | GND | U17 | | | |
| N/A | GND | Y20 | | | |
| N/A | GND | AA21 | | | |
| N/A | GND | AB22 | | | |
| N/A | GND | AC23 | | | |
| N/A | GND | AD24 | | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| N/A | M0 | | AD24 | | | |
| N/A | M1 | | AC24 | | | |
| N/A | M2 | | AC23 | | | |
| N/A | TCK | | G7 | | | |
| N/A | TDI | | F26 | | | |
| N/A | TDO | | F5 | | | |
| N/A | TMS | | H8 | | | |
| N/A | PWRDWN_B | | AD7 | | | |
| N/A | HSWAP_EN | | H23 | | | |
| N/A | RSVD | | D6 | | | |
| N/A | VBATT | | H7 | | | |
| N/A | DXP | | H24 | | | |
| N/A | DXN | | D25 | | | |
| N/A | AVCCAUXTX4 | | B26 | | | |
| N/A | VTTXPAD4 | | B27 | | | |
| N/A | TXNPAD4 | | A27 | | | |
| N/A | TXPPAD4 | | A26 | | | |
| N/A | GNDA4 | | C25 | | | |
| N/A | RXPPAD4 | | A25 | | | |
| N/A | RXNPAD4 | | A24 | | | |
| N/A | VTRXPAD4 | | B25 | | | |
| N/A | AVCCAUXRX4 | | B24 | | | |
| N/A | AVCCAUXTX6 | | B19 | | | |
| N/A | VTTXPAD6 | | B20 | | | |
| N/A | TXNPAD6 | | A20 | | | |
| N/A | TXPPAD6 | | A19 | | | |
| N/A | GNDA6 | | C19 | | | |
| N/A | RXPPAD6 | | A18 | | | |
| N/A | RXNPAD6 | | A17 | | | |
| N/A | VTRXPAD6 | | B18 | | | |
| N/A | AVCCAUXRX6 | | B17 | | | |
| N/A | AVCCAUXTX7 | | B13 | | | |
| N/A | VTTXPAD7 | | B14 | | | |
| N/A | TXNPAD7 | | A14 | | | |
| N/A | TXPPAD7 | | A13 | | | |
| N/A | GNDA7 | | C12 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| N/A | TXPPAD9 | A8 | | | | |
| N/A | GNDA9 | C8 | | | | |
| N/A | RXPPAD9 | A7 | | | | |
| N/A | RXNPAD9 | A6 | | | | |
| N/A | VTRXPAD9 | B7 | | | | |
| N/A | AVCCAUXRX9 | B6 | | | | |
| N/A | AVCCAUXTX11 | B4 | NC | NC | | |
| N/A | VTTXPAD11 | B5 | NC | NC | | |
| N/A | TXNPAD11 | A5 | NC | NC | | |
| N/A | TXPPAD11 | A4 | NC | NC | | |
| N/A | GNDA11 | C5 | NC | NC | | |
| N/A | RXPPAD11 | A3 | NC | NC | | |
| N/A | RXNPAD11 | A2 | NC | NC | | |
| N/A | VTRXPAD11 | B3 | NC | NC | | |
| N/A | AVCCAUXRX11 | B2 | NC | NC | | |
| N/A | AVCCAUXRX14 | AN2 | NC | NC | | |
| N/A | VTRXPAD14 | AN3 | NC | NC | | |
| N/A | RXNPAD14 | AP2 | NC | NC | | |
| N/A | RXPPAD14 | AP3 | NC | NC | | |
| N/A | GNDA14 | AM5 | NC | NC | | |
| N/A | TXPPAD14 | AP4 | NC | NC | | |
| N/A | TXNPAD14 | AP5 | NC | NC | | |
| N/A | VTTXPAD14 | AN5 | NC | NC | | |
| N/A | AVCCAUXTX14 | AN4 | NC | NC | | |
| N/A | AVCCAUXRX16 | AN6 | | | | |
| N/A | VTRXPAD16 | AN7 | | | | |
| N/A | RXNPAD16 | AP6 | | | | |
| N/A | RXPPAD16 | AP7 | | | | |
| N/A | GNDA16 | AM8 | | | | |
| N/A | TXPPAD16 | AP8 | | | | |
| N/A | TXNPAD16 | AP9 | | | | |
| N/A | VTTXPAD16 | AN9 | | | | |
| N/A | AVCCAUXTX16 | AN8 | | | | |
| N/A | AVCCAUXRX17 | AN10 | NC | NC | NC | |
| N/A | VTRXPAD17 | AN11 | NC | NC | NC | |
| N/A | RXNPAD17 | AP10 | NC | NC | NC | |
| N/A | RXPPAD17 | AP11 | NC | NC | NC | |
| N/A | GNDA17 | AM12 | NC | NC | NC | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 0 | IO_L43N_0 | B22 | | |
| 0 | IO_L43P_0 | C22 | | |
| 0 | IO_L44N_0 | K21 | | |
| 0 | IO_L44P_0 | L21 | | |
| 0 | IO_L45N_0 | G21 | | |
| 0 | IO_L45P_0/VREF_0 | H21 | | |
| 0 | IO_L46N_0 | E21 | | |
| 0 | IO_L46P_0 | F21 | | |
| 0 | IO_L47N_0 | K20 | | |
| 0 | IO_L47P_0 | L20 | | |
| 0 | IO_L48N_0 | C21 | | |
| 0 | IO_L48P_0 | D21 | | |
| 0 | IO_L49N_0 | A21 | | |
| 0 | IO_L49P_0 | B21 | | |
| 0 | IO_L50_0/No_Pair | G20 | | |
| 0 | IO_L53_0/No_Pair | H19 | | |
| 0 | IO_L54N_0 | E20 | | |
| 0 | IO_L54P_0 | F20 | | |
| 0 | IO_L55N_0 | C20 | | |
| 0 | IO_L55P_0 | D19 | | |
| 0 | IO_L56N_0 | K19 | | |
| 0 | IO_L56P_0 | L19 | | |
| 0 | IO_L57N_0 | A20 | | |
| 0 | IO_L57P_0/VREF_0 | B20 | | |
| 0 | IO_L66N_0 | F19 | NC | |
| 0 | IO_L66P_0/VREF_0 | G19 | NC | |
| 0 | IO_L67N_0 | B19 | | |
| 0 | IO_L67P_0 | C19 | | |
| 0 | IO_L68N_0 | H18 | | |
| 0 | IO_L68P_0 | J18 | | |
| 0 | IO_L69N_0 | F18 | | |
| 0 | IO_L69P_0/VREF_0 | G18 | | |
| 0 | IO_L73N_0 | D18 | | |
| 0 | IO_L73P_0 | E18 | | |
| 0 | IO_L74N_0/GCLK7P | K18 | | |
| 0 | IO_L74P_0/GCLK6S | L18 | | |
| 0 | IO_L75N_0/GCLK5P | B18 | | |
| 0 | IO_L75P_0/GCLK4S | C18 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 2 | IO_L59P_2 | U11 | | |
| 2 | IO_L60N_2 | R1 | | |
| 2 | IO_L60P_2 | R2 | | |
| 2 | IO_L85N_2 | T3 | | |
| 2 | IO_L85P_2 | T4 | | |
| 2 | IO_L86N_2 | U8 | | |
| 2 | IO_L86P_2 | U9 | | |
| 2 | IO_L87N_2 | U2 | | |
| 2 | IO_L87P_2 | T2 | | |
| 2 | IO_L88N_2/VREF_2 | U4 | | |
| 2 | IO_L88P_2 | U5 | | |
| 2 | IO_L89N_2 | U6 | | |
| 2 | IO_L89P_2 | U7 | | |
| 2 | IO_L90N_2 | V3 | | |
| 2 | IO_L90P_2 | U3 | | |
| | | | | |
| 3 | IO_L90N_3 | V6 | | |
| 3 | IO_L90P_3 | V7 | | |
| 3 | IO_L89N_3 | V10 | | |
| 3 | IO_L89P_3 | V11 | | |
| 3 | IO_L88N_3 | V4 | | |
| 3 | IO_L88P_3 | V5 | | |
| 3 | IO_L87N_3/VREF_3 | V2 | | |
| 3 | IO_L87P_3 | W2 | | |
| 3 | IO_L86N_3 | V8 | | |
| 3 | IO_L86P_3 | V9 | | |
| 3 | IO_L85N_3 | W6 | | |
| 3 | IO_L85P_3 | W7 | | |
| 3 | IO_L60N_3 | W3 | | |
| 3 | IO_L60P_3 | W4 | | |
| 3 | IO_L59N_3 | W10 | | |
| 3 | IO_L59P_3 | W11 | | |
| 3 | IO_L58N_3 | Y5 | | |
| 3 | IO_L58P_3 | Y6 | | |
| 3 | IO_L57N_3/VREF_3 | Y3 | | |
| 3 | IO_L57P_3 | AA3 | | |
| 3 | IO_L56N_3 | W8 | | |
| 3 | IO_L56P_3 | Y7 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 7 | IO_L43N_7 | R37 | | |
| 7 | IO_L42P_7 | R34 | | |
| 7 | IO_L42N_7 | R35 | | |
| 7 | IO_L41P_7 | U28 | | |
| 7 | IO_L41N_7 | T28 | | |
| 7 | IO_L40P_7 | R32 | | |
| 7 | IO_L40N_7/VREF_7 | R33 | | |
| 7 | IO_L39P_7 | P38 | | |
| 7 | IO_L39N_7 | P39 | | |
| 7 | IO_L38P_7 | T29 | | |
| 7 | IO_L38N_7 | T30 | | |
| 7 | IO_L37P_7 | N37 | | |
| 7 | IO_L37N_7 | P37 | | |
| 7 | IO_L36P_7 | P35 | | |
| 7 | IO_L36N_7 | P36 | | |
| 7 | IO_L35P_7 | T27 | | |
| 7 | IO_L35N_7 | R27 | | |
| 7 | IO_L34P_7 | P33 | | |
| 7 | IO_L34N_7/VREF_7 | P34 | | |
| 7 | IO_L33P_7 | N38 | | |
| 7 | IO_L33N_7 | N39 | | |
| 7 | IO_L32P_7 | R28 | | |
| 7 | IO_L32N_7 | R29 | | |
| 7 | IO_L31P_7 | N35 | | |
| 7 | IO_L31N_7 | M36 | | |
| 7 | IO_L30P_7 | N33 | | |
| 7 | IO_L30N_7 | N34 | | |
| 7 | IO_L29P_7 | R30 | | |
| 7 | IO_L29N_7 | R31 | | |
| 7 | IO_L28P_7 | M37 | | |
| 7 | IO_L28N_7/VREF_7 | M38 | | |
| 7 | IO_L27P_7 | M33 | | |
| 7 | IO_L27N_7 | M34 | | |
| 7 | IO_L26P_7 | P28 | | |
| 7 | IO_L26N_7 | P29 | | |
| 7 | IO_L25P_7 | L38 | | |
| 7 | IO_L25N_7 | L39 | | |
| 7 | IO_L24P_7 | L36 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | TXNPAD11 | A7 | | |
| N/A | TXPPAD11 | A6 | | |
| N/A | GNDA11 | C6 | | |
| N/A | RXPPAD11 | A5 | | |
| N/A | RXNPAD11 | A4 | | |
| N/A | VTRXPAD11 | B5 | | |
| N/A | AVCCAUXRX11 | B4 | | |
| N/A | AVCCAUXRX14 | AV4 | | |
| N/A | VTRXPAD14 | AV5 | | |
| N/A | RXNPAD14 | AW4 | | |
| N/A | RXPPAD14 | AW5 | | |
| N/A | GNDA14 | AU6 | | |
| N/A | TXPPAD14 | AW6 | | |
| N/A | TXNPAD14 | AW7 | | |
| N/A | VTTXPAD14 | AV7 | | |
| N/A | AVCCAUXTX14 | AV6 | | |
| N/A | AVCCAUXRX16 | AV8 | | |
| N/A | VTRXPAD16 | AV9 | | |
| N/A | RXNPAD16 | AW8 | | |
| N/A | RXPPAD16 | AW9 | | |
| N/A | GNDA16 | AU9 | | |
| N/A | TXPPAD16 | AW10 | | |
| N/A | TXNPAD16 | AW11 | | |
| N/A | VTTXPAD16 | AV11 | | |
| N/A | AVCCAUXTX16 | AV10 | | |
| N/A | AVCCAUXRX17 | AV12 | | |
| N/A | VTRXPAD17 | AV13 | | |
| N/A | RXNPAD17 | AW12 | | |
| N/A | RXPPAD17 | AW13 | | |
| N/A | GNDA17 | AU13 | | |
| N/A | TXPPAD17 | AW14 | | |
| N/A | TXNPAD17 | AW15 | | |
| N/A | VTTXPAD17 | AV15 | | |
| N/A | AVCCAUXTX17 | AV14 | | |
| N/A | AVCCAUXRX18 | AV16 | | |
| N/A | VTRXPAD18 | AV17 | | |
| N/A | RXNPAD18 | AW16 | | |
| N/A | RXPPAD18 | AW17 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | GND | | E22 | | |
| N/A | GND | | E21 | | |
| N/A | GND | | E5 | | |
| N/A | GND | | D39 | | |
| N/A | GND | | D32 | | |
| N/A | GND | | D28 | | |
| N/A | GND | | D15 | | |
| N/A | GND | | D11 | | |
| N/A | GND | | D4 | | |
| N/A | GND | | C42 | | |
| N/A | GND | | C41 | | |
| N/A | GND | | C40 | | |
| N/A | GND | | C3 | | |
| N/A | GND | | C2 | | |
| N/A | GND | | C1 | | |
| N/A | GND | | B42 | | |
| N/A | GND | | B1 | | |
| N/A | GND | | N14 | | |
| N/A | GND | | N29 | | |
| N/A | GND | | AK14 | | |
| N/A | GND | | AK29 | | |
| N/A | GND | | P13 | | |
| N/A | GND | | P30 | | |
| N/A | GND | | AJ13 | | |
| N/A | GND | | AJ30 | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 6 | IO_L15P_6 | AP39 | |
| 6 | IO_L15N_6/VREF_6 | AP40 | |
| 6 | IO_L16P_6 | AP36 | |
| 6 | IO_L16N_6 | AP37 | |
| 6 | IO_L17P_6 | AH31 | |
| 6 | IO_L17N_6 | AG31 | |
| 6 | IO_L18P_6 | AN41 | |
| 6 | IO_L18N_6 | AN42 | |
| 6 | IO_L19P_6 | AN40 | |
| 6 | IO_L19N_6 | AM40 | |
| 6 | IO_L20P_6 | AG34 | |
| 6 | IO_L20N_6 | AG35 | |
| 6 | IO_L21P_6 | AN37 | |
| 6 | IO_L21N_6/VREF_6 | AN38 | |
| 6 | IO_L22P_6 | AN36 | |
| 6 | IO_L22N_6 | AM36 | |
| 6 | IO_L23P_6 | AG32 | |
| 6 | IO_L23N_6 | AG33 | |
| 6 | IO_L24P_6 | AM41 | |
| 6 | IO_L24N_6 | AM42 | |
| 6 | IO_L25P_6 | AM38 | |
| 6 | IO_L25N_6 | AM39 | |
| 6 | IO_L26P_6 | AF35 | |
| 6 | IO_L26N_6 | AF36 | |
| 6 | IO_L27P_6 | AM37 | |
| 6 | IO_L27N_6/VREF_6 | AL36 | |
| 6 | IO_L28P_6 | AL41 | |
| 6 | IO_L28N_6 | AK41 | |
| 6 | IO_L29P_6 | AF32 | |
| 6 | IO_L29N_6 | AF33 | |
| 6 | IO_L30P_6 | AL39 | |
| 6 | IO_L30N_6 | AL40 | |
| 6 | IO_L31P_6 | AL37 | |
| 6 | IO_L31N_6 | AL38 | |
| 6 | IO_L32P_6 | AF31 | |
| 6 | IO_L32N_6 | AE31 | |
| 6 | IO_L33P_6 | AK39 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 6 | IO_L33N_6/VREF_6 | AK40 | |
| 6 | IO_L34P_6 | AK36 | |
| 6 | IO_L34N_6 | AK37 | |
| 6 | IO_L35P_6 | AE36 | |
| 6 | IO_L35N_6 | AE37 | |
| 6 | IO_L36P_6 | AJ41 | |
| 6 | IO_L36N_6 | AJ42 | |
| 6 | IO_L37P_6 | AJ40 | |
| 6 | IO_L37N_6 | AH40 | |
| 6 | IO_L38P_6 | AE34 | |
| 6 | IO_L38N_6 | AE35 | |
| 6 | IO_L39P_6 | AJ38 | |
| 6 | IO_L39N_6/VREF_6 | AH37 | |
| 6 | IO_L40P_6 | AJ36 | |
| 6 | IO_L40N_6 | AJ37 | |
| 6 | IO_L41P_6 | AE32 | |
| 6 | IO_L41N_6 | AE33 | |
| 6 | IO_L42P_6 | AH41 | |
| 6 | IO_L42N_6 | AH42 | |
| 6 | IO_L43P_6 | AH38 | |
| 6 | IO_L43N_6 | AH39 | |
| 6 | IO_L44P_6 | AD36 | |
| 6 | IO_L44N_6 | AC35 | |
| 6 | IO_L45P_6 | AH36 | |
| 6 | IO_L45N_6/VREF_6 | AG36 | |
| 6 | IO_L46P_6 | AG41 | |
| 6 | IO_L46N_6 | AG42 | |
| 6 | IO_L47P_6 | AD34 | |
| 6 | IO_L47N_6 | AC33 | |
| 6 | IO_L48P_6 | AG40 | |
| 6 | IO_L48N_6 | AF39 | |
| 6 | IO_L49P_6 | AG38 | |
| 6 | IO_L49N_6 | AG39 | |
| 6 | IO_L50P_6 | AD32 | |
| 6 | IO_L50N_6 | AD33 | |
| 6 | IO_L51P_6 | AG37 | |
| 6 | IO_L51N_6/VREF_6 | AF37 | |