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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	752
Number of Logic Elements/Cells	6768
Total RAM Bits	516096
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp4-6fg456c

Notice of Disclaimer

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Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011

Product Specification

Virtex-II Pro⁽¹⁾ Array Functional Description

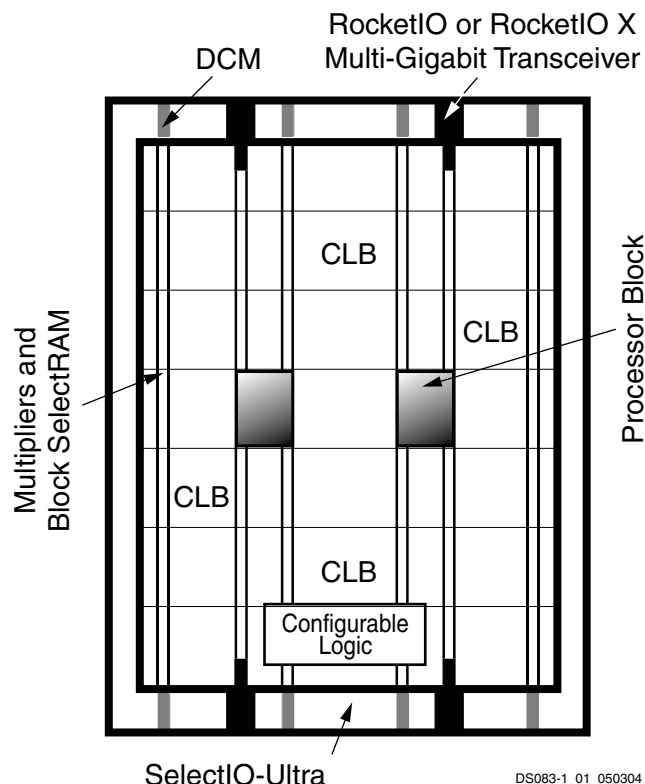


Figure 1: Virtex-II Pro Generic Architecture Overview

This module describes the following Virtex™-II Pro functional components, as shown in **Figure 1**:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in **Module 3** of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see [PowerPC Processor Reference Guide](#) and [PowerPC 405 Processor Block Reference Guide](#).
- For detailed RocketIO transceiver digital/analog design considerations, see [RocketIO Transceiver User Guide](#).
- For detailed RocketIO X transceiver digital/analog design considerations, see [RocketIO X Transceiver User Guide](#).
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see [Virtex-II Pro Platform FPGA User Guide](#).

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

- [Functional Description: RocketIO X Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: RocketIO Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: Processor Block](#)
- [Functional Description: Embedded PowerPC 405 Core](#)
- [Functional Description: FPGA](#)
- [Revision History](#)

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX} , the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 μ m has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Routing

DCM and MGT Locations/Organization

Virtex-II Pro DCMs and serial transceivers (MGTs) are placed on the top and bottom of each block RAM and multiplier column in some combination, as shown in Table 31. The number of DCMs and RocketIO transceivers total twice the number of block RAM columns in the device. Refer to Figure 52, page 47 for an illustration of this in the XC2VP4 device.

Table 31: DCM and MGT Organization

Device	Block RAM Columns	DCMs	MGTs
XC2VP2	4	4	4
XC2VP4	4	4	4
XC2VP7	6	4	8
XC2VP20	8	8	8
XC2VPX20	8	8	8
XC2VP30	8	8	8
XC2VP40	10	8	12
XC2VP50	12	8	16
XC2VP70	14	8	20
XC2VPX70	14	8	20
XC2VP100	16	12	20

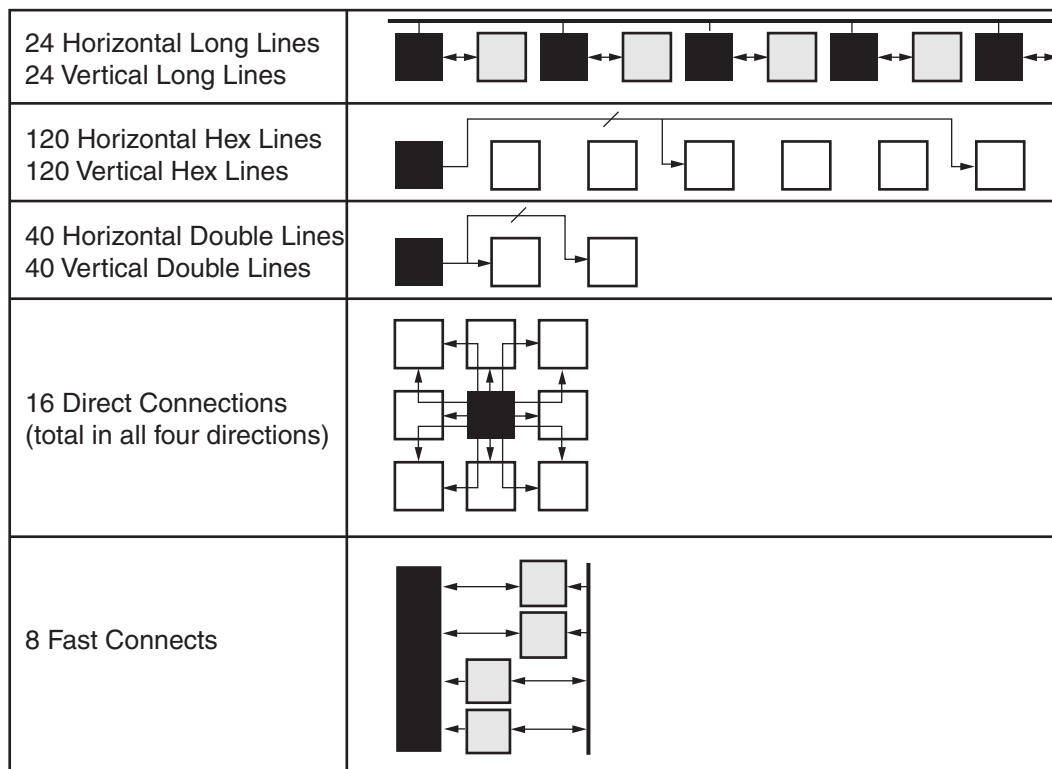
Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II Pro signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in Figure 64, page 54, Virtex-II Pro has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).



DS031_60_110200

Figure 64: Hierarchical Routing Resources

Clock Distribution Switching Characteristics

Table 41: Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Global Clock Buffer I input to O output	T_{GIO}	0.05	0.057	0.064	ns, max
Global Clock Buffer S input Setup/Hold to I1 and I2 inputs	T_{GSI}/T_{GIS}	0.49/–0.10	0.54/–0.12	0.60/–0.13	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see [Figure 34](#) in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 42: CLB Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T _{ILO}	0.28	0.32	0.36	ns, max
5-input function: F/G inputs to F5 output	T _{IF5}	0.59	0.65	0.73	ns, max
5-input function: F/G inputs to X output	T _{IF5X}	0.63	0.70	0.79	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T _{IFXY}	0.29	0.32	0.36	ns, max
FXINA input to FX output via MUXFX	T _{INAFX}	0.29	0.32	0.36	ns, max
FXINB input to FX output via MUXFX	T _{INBFX}	0.29	0.32	0.36	ns, max
SOPIN input to SOPOUT output via ORCY	T _{SOPSOP}	0.11	0.13	0.14	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T _{IFNCTL}	0.23	0.24	0.27	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T _{CKO}	0.37	0.38	0.42	ns, max
Latch Clock CLK to XQ/YQ outputs	T _{CKLO}	0.54	0.57	0.64	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T _{DICK} /T _{CKDI}	0.21/–0.04	0.24/–0.05	0.27/–0.06	ns, min
DY inputs	T _{DYCK} /T _{CKDY}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
DX inputs	T _{DXCK} /T _{CKDX}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
CE input	T _{CECK} /T _{CKCE}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
SR/BY inputs (synchronous)	T _{RCK} /T _{CKR}	0.55/–0.01	0.60/–0.01	0.78/–0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T _{CH}	0.37	0.40	0.45	ns, min
Minimum Pulse Width, Low	T _{CL}	0.37	0.40	0.45	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T _{RPW}	0.37	0.40	0.45	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T _{RQ}	1.09	1.25	1.40	ns, max
Toggle Frequency (for export control)	F _{TOG}	1350	1200	1050	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Date	Version	Revision
08/25/03	2.9	- Updated time and frequency parameters as per speedsfile v1.81. Table 1: Footnote (2) rewritten to specify “one or more banks.” Table 2: Added footnote referring to XAPP659 for 3.3V I/O operation. Table 53 and Table 54: Revised test setup footnote to refer to Figure 6. Previously specified a capacitive load parameter. Table 57: Due to a document compilation error in v2.8, some DCM parameters were erroneously omitted from the full data sheet file (all four modules concatenated), though not from the stand-alone Module 3 file. The omitted parameters have been restored. Table 64 and Table 66: Corrected parameters to expression in picoseconds, as labeled. Previously expressed in nanoseconds, but labeled picoseconds. Figure 6: Added note to figure regarding termination resistors. Table 5: Added $I_{CCINTMIN}$ for XC2VP30 device.
09/10/03	2.10	Figure 7: Changed representation of mode pins M0, M1, and M2 indicating that they must be held to a constant DC level during and after configuration. Table 49: Added footnote indicating that mode pins M0, M1, and M2 must be held to a constant DC level during and after configuration.
10/14/03	2.11	Table 1: Deleted Footnote (2), which had derated the absolute maximum T_J when one or more banks operated at 3.3V. Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. Added new Footnote (2) linking to website for package thermal data. Table 4 and Table 5: Filled in power-on and quiescent current parameters for all devices through XC2VP70. Added Industrial Grade multiplier specification to Footnote (1) in both tables. - In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to XAPP689 regarding handling of simultaneously switching outputs (SSO). - In section I/O Standard Adjustment Measurement Methodology: Table 39 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 40, Output Delay Measurement Methodology. - Replaced Figure 6, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. Table 58: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
11/10/03	2.12	Table 1: Changed 3.3V absolute max V_{IN} and V_{TS} from 3.75V to 4.05V. Added footnote referring to XAPP659. Table 4: Removed MIN column from table.
12/05/03	3.0	- XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, updated and released to Production status as per speedsfile v1.83. Featured changes: - Speedsfile parameter values for -7 speed grade added for devices XC2VP2-XC2VP70. Table 13 and Table 14: Pin-to-pin and register-to_register performance parameter values added. Table 64: New parameter T_{DCD_LOCAL} (and footnote) replaces T_{DCD_CLK0}. - All remaining source-synchronous parameter values added (Table 64 & following).

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)

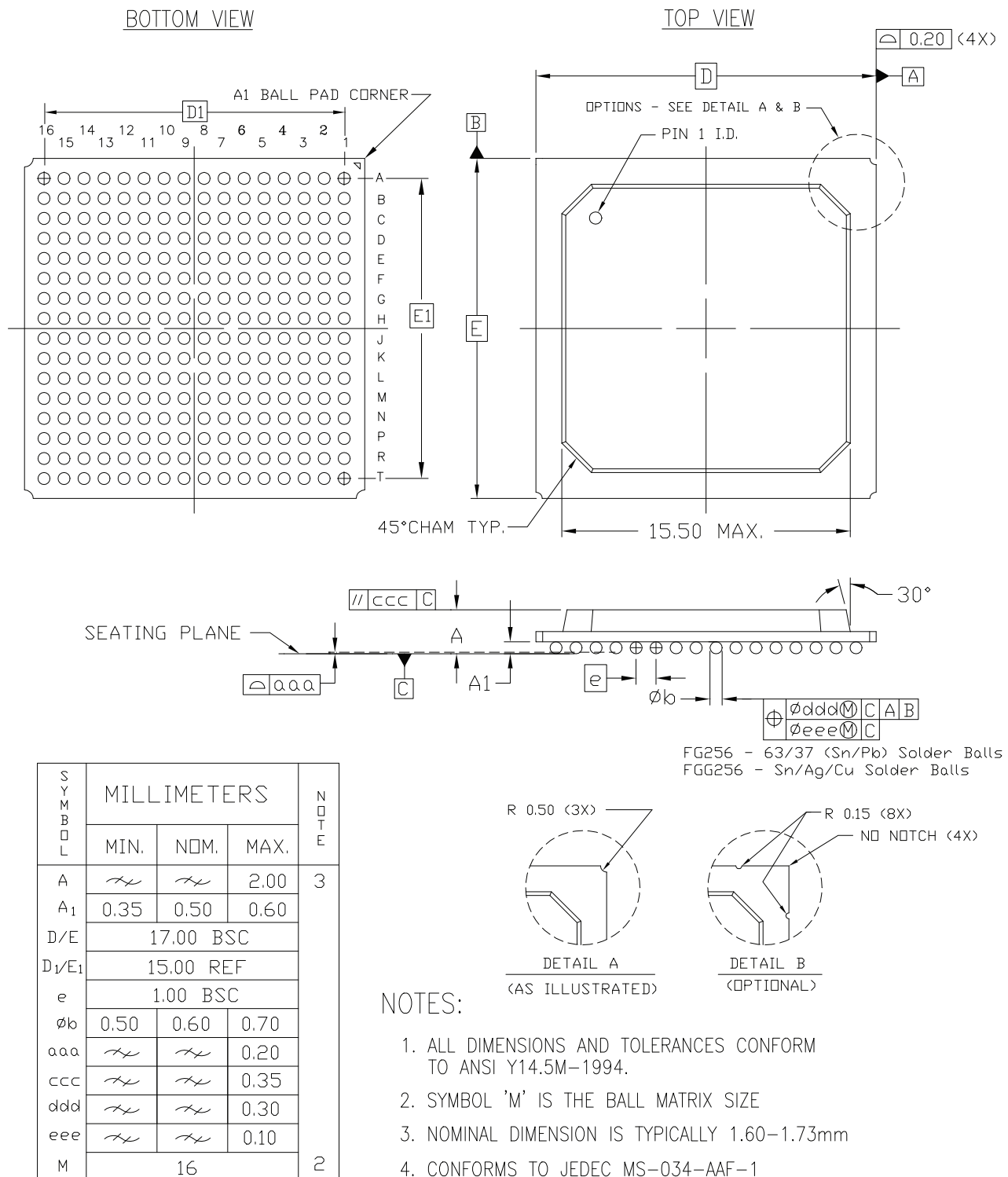


Figure 1: FG256/FGG256 Fine-Pitch BGA Package Specifications

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
5	IO_L74P_5/GCLK4P	AB14			
5	IO_L73N_5	AA14			
5	IO_L73P_5	Y14			
5	IO_L69N_5/VREF_5	W14			
5	IO_L69P_5	W15			
5	IO_L68N_5	AD15			
5	IO_L68P_5	AC15			
5	IO_L67N_5	AB15			
5	IO_L67P_5	AA15			
5	IO_L45N_5/VREF_5	AC16	NC	NC	
5	IO_L45P_5	AB16	NC	NC	
5	IO_L44N_5	Y15	NC	NC	
5	IO_L44P_5	Y16	NC	NC	
5	IO_L43N_5	AC17	NC	NC	
5	IO_L43P_5	AB17	NC	NC	
5	IO_L39N_5	AA16	NC	NC	
5	IO_L39P_5	AA17	NC	NC	
5	IO_L38N_5	W16	NC	NC	
5	IO_L38P_5	Y17	NC	NC	
5	IO_L37N_5	AD18	NC	NC	
5	IO_L37P_5	AC18	NC	NC	
5	IO_L09N_5/VREF_5	AA18			
5	IO_L09P_5	Y18			
5	IO_L08N_5	AF19			
5	IO_L08P_5	AE19			
5	IO_L07N_5/VREF_5	AD19			
5	IO_L07P_5	AC19			
5	IO_L06N_5/VRP_5	AB18			
5	IO_L06P_5/VRN_5	AB19			
5	IO_L05_5/No_Pair	Y19			
5	IO_L03N_5/D4	AA19			
5	IO_L03P_5/D5	AA20			
5	IO_L02N_5/D6	AC20			
5	IO_L02P_5/D7	AB20			
5	IO_L01N_5/RDWR_B	AD21			
5	IO_L01P_5/CS_B	AC21			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L74N_1/GCLK1P	D17				
1	IO_L74P_1/GCLK0S	E17				
1	IO_L73N_1	F17				
1	IO_L73P_1	G17				
1	IO_L69N_1/VREF_1	K17				
1	IO_L69P_1	L17				
1	IO_L68N_1	D16				
1	IO_L68P_1	E16				
1	IO_L67N_1	F16				
1	IO_L67P_1	G16				
1	IO_L57N_1/VREF_1	H16				
1	IO_L57P_1	J16				
1	IO_L56N_1	D15				
1	IO_L56P_1	D14				
1	IO_L55N_1	F15				
1	IO_L55P_1	G15				
1	IO_L54N_1	K16				
1	IO_L54P_1	L16				
1	IO_L53_1/No_Pair	C13				
1	IO_L50_1/No_Pair	C14				
1	IO_L49N_1	E14				
1	IO_L49P_1	F14				
1	IO_L48N_1	J15				
1	IO_L48P_1	K15				
1	IO_L47N_1	C11				
1	IO_L47P_1	D11				
1	IO_L46N_1	D12				
1	IO_L46P_1	D13				
1	IO_L45N_1/VREF_1	G14				
1	IO_L45P_1	H14				
1	IO_L44N_1	D10				
1	IO_L44P_1	E10				
1	IO_L43N_1	E13				
1	IO_L43P_1	F13				
1	IO_L39N_1	J14				
1	IO_L39P_1	K14				
1	IO_L38N_1	C9				
1	IO_L38P_1	D9				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 11](#), XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the [FF1148 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

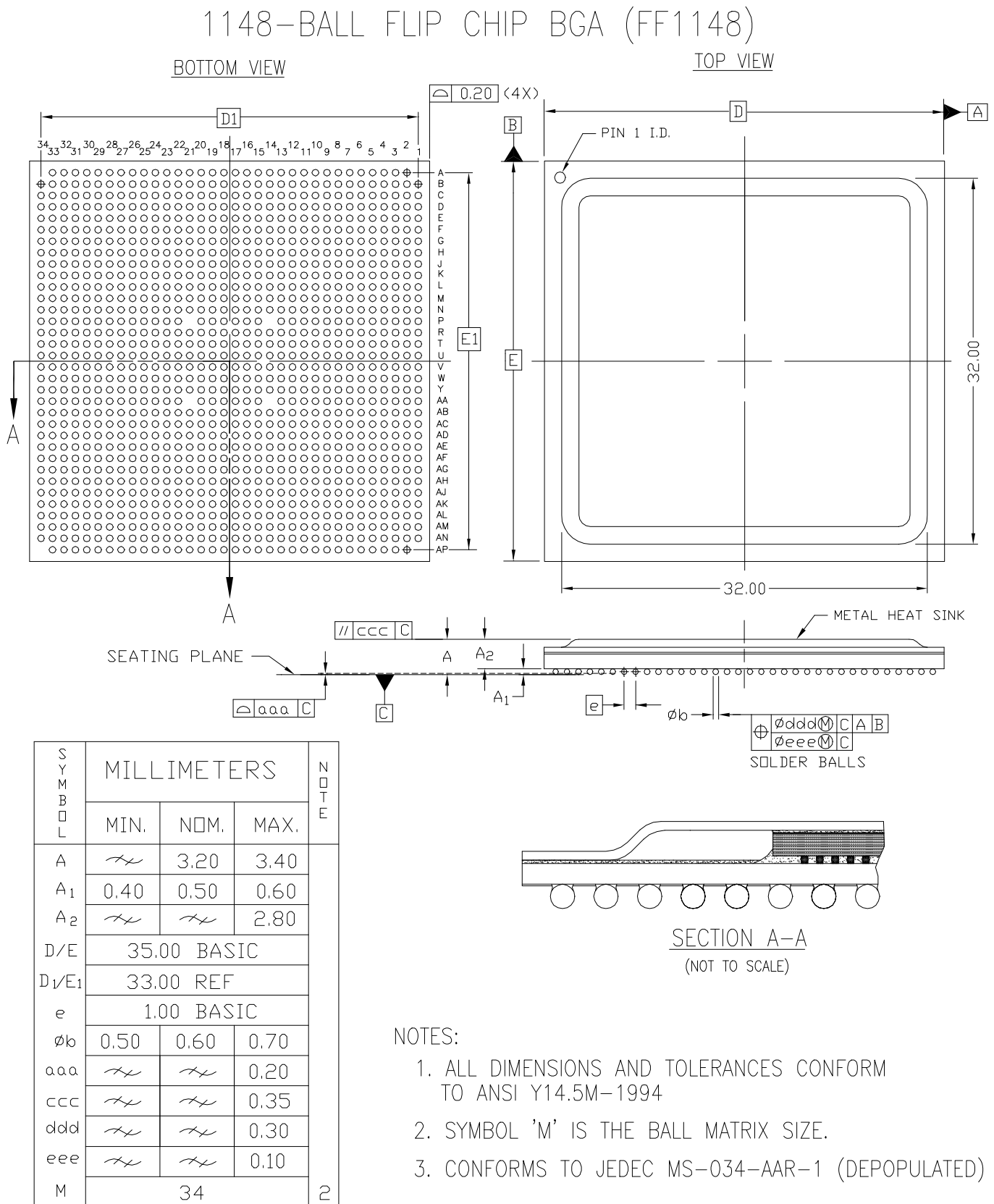


Figure 7: FF1148 Flip-Chip Fine-Pitch BGA Package Specifications

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L49N_2	U5		
2	IO_L49P_2	U6		
2	IO_L50N_2	U13		
2	IO_L50P_2	V13		
2	IO_L51N_2	U4		
2	IO_L51P_2	T4		
2	IO_L52N_2/VREF_2	U1		
2	IO_L52P_2	U2		
2	IO_L53N_2	V9		
2	IO_L53P_2	V10		
2	IO_L54N_2	V7		
2	IO_L54P_2	V8		
2	IO_L55N_2	V5		
2	IO_L55P_2	V6		
2	IO_L56N_2	V11		
2	IO_L56P_2	V12		
2	IO_L57N_2	V3		
2	IO_L57P_2	V4		
2	IO_L58N_2/VREF_2	V1		
2	IO_L58P_2	V2		
2	IO_L59N_2	W10		
2	IO_L59P_2	W11		
2	IO_L60N_2	W7		
2	IO_L60P_2	W8		
2	IO_L85N_2	W5		
2	IO_L85P_2	W6		
2	IO_L86N_2	W12		
2	IO_L86P_2	W13		
2	IO_L87N_2	W3		
2	IO_L87P_2	W4		
2	IO_L88N_2/VREF_2	Y7		
2	IO_L88P_2	Y8		
2	IO_L89N_2	W9		
2	IO_L89P_2	Y9		
2	IO_L90N_2	Y3		
2	IO_L90P_2	Y4		
3	IO_L90N_3	AA7		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L66P_4/VREF_4	AU19		
4	IO_L67N_4	AM19		
4	IO_L67P_4	AL19		
4	IO_L68N_4	AK19		
4	IO_L68P_4	AJ19		
4	IO_L69N_4	AP19		
4	IO_L69P_4/VREF_4	AN19		
4	IO_L73N_4	AT19		
4	IO_L73P_4	AR19		
4	IO_L74N_4/GCLK3S	AH20		
4	IO_L74P_4/GCLK2P	AG20		
4	IO_L75N_4/GCLK1S	AL20		
4	IO_L75P_4/GCLK0P	AK20		
5	IO_L75N_5/GCLK7S	AR20		
5	IO_L75P_5/GCLK6P	AT20		
5	IO_L74N_5/GCLK5S	AH21		
5	IO_L74P_5/GCLK4P	AJ21		
5	IO_L73N_5	AP20		
5	IO_L73P_5	AP21		
5	IO_L69N_5/VREF_5	AU21		
5	IO_L69P_5	AU22		
5	IO_L68N_5	AK21		
5	IO_L68P_5	AL21		
5	IO_L67N_5	AR21		
5	IO_L67P_5	AT21		
5	IO_L66N_5/VREF_5	AN21		
5	IO_L66P_5	AN22		
5	IO_L65N_5	AM20		
5	IO_L65P_5	AM21		
5	IO_L64N_5	AR22		
5	IO_L64P_5	AT22		
5	IO_L60N_5	AP22		
5	IO_L60P_5	AR23		
5	IO_L59N_5	AG21		
5	IO_L59P_5	AG22		
5	IO_L58N_5	AL22		
5	IO_L58P_5	AM22		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L24N_7	L37		
7	IO_L23P_7	P31		
7	IO_L23N_7	P32		
7	IO_L22P_7	L34		
7	IO_L22N_7/VREF_7	L35		
7	IO_L21P_7	L32		
7	IO_L21N_7	L33		
7	IO_L20P_7	N29		
7	IO_L20N_7	M29		
7	IO_L19P_7	K38		
7	IO_L19N_7	K39		
7	IO_L18P_7	J37		
7	IO_L18N_7	K37		
7	IO_L17P_7	N30		
7	IO_L17N_7	P30		
7	IO_L16P_7	K35		
7	IO_L16N_7/VREF_7	K36		
7	IO_L15P_7	K34		
7	IO_L15N_7	K33		
7	IO_L14P_7	N31		
7	IO_L14N_7	M32		
7	IO_L13P_7	J38		
7	IO_L13N_7	J39		
7	IO_L12P_7	J35		
7	IO_L12N_7	H36		
7	IO_L11P_7	M30		
7	IO_L11N_7	L31		
7	IO_L10P_7	J33		
7	IO_L10N_7/VREF_7	J34		
7	IO_L09P_7	H37		
7	IO_L09N_7	H38		
7	IO_L08P_7	K31		
7	IO_L08N_7	K32		
7	IO_L07P_7	H33		
7	IO_L07N_7	H34		
7	IO_L84P_7	G38	NC	
7	IO_L84N_7	G39	NC	
7	IO_L82P_7	G36	NC	

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L44P_2		U10		
2	IO_L45N_2		U3		
2	IO_L45P_2		U4		
2	IO_L46N_2/VREF_2		U1		
2	IO_L46P_2		U2		
2	IO_L47N_2		T12		
2	IO_L47P_2		U12		
2	IO_L48N_2		V10		
2	IO_L48P_2		V11		
2	IO_L49N_2		V7		
2	IO_L49P_2		V8		
2	IO_L50N_2		U11		
2	IO_L50P_2		V12		
2	IO_L51N_2		V4		
2	IO_L51P_2		V5		
2	IO_L52N_2/VREF_2		V1		
2	IO_L52P_2		V2		
2	IO_L53N_2		W9		
2	IO_L53P_2		W10		
2	IO_L54N_2		W7		
2	IO_L54P_2		W8		
2	IO_L55N_2		W5		
2	IO_L55P_2		W6		
2	IO_L56N_2		W11		
2	IO_L56P_2		W12		
2	IO_L57N_2		W3		
2	IO_L57P_2		W4		
2	IO_L58N_2/VREF_2		W1		
2	IO_L58P_2		W2		
2	IO_L59N_2		Y9		
2	IO_L59P_2		Y10		
2	IO_L60N_2		Y6		
2	IO_L60P_2		Y7		
2	IO_L85N_2		Y3		
2	IO_L85P_2		Y4		
2	IO_L86N_2		Y11		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L60P_4		AR19		
4	IO_L64N_4		AV19		
4	IO_L64P_4		AU19		
4	IO_L65N_4		AW19		
4	IO_L65P_4		AY19		
4	IO_L66N_4		AL21		
4	IO_L66P_4/VREF_4		AL20		
4	IO_L67N_4		AN20		
4	IO_L67P_4		AM20		
4	IO_L68N_4		AP20		
4	IO_L68P_4		AR20		
4	IO_L69N_4		AV20		
4	IO_L69P_4/VREF_4		AU20		
4	IO_L73N_4		AY20		
4	IO_L73P_4		AW20		
4	IO_L74N_4/GCLK3S		AN21		
4	IO_L74P_4/GCLK2P		AP21		
4	IO_L75N_4/GCLK1S		AU21		
4	IO_L75P_4/GCLK0P		AT21		
5	IO_L75N_5/GCLK7S	BREFCLKN	AT22		
5	IO_L75P_5/GCLK6P	BREFCLKP	AU22		
5	IO_L74N_5/GCLK5S		AP22		
5	IO_L74P_5/GCLK4P		AN22		
5	IO_L73N_5		AW23		
5	IO_L73P_5		AY23		
5	IO_L69N_5/VREF_5		AU23		
5	IO_L69P_5		AV23		
5	IO_L68N_5		AR23		
5	IO_L68P_5		AP23		
5	IO_L67N_5		AM23		
5	IO_L67P_5		AN23		
5	IO_L66N_5/VREF_5		AL23		
5	IO_L66P_5		AL22		
5	IO_L65N_5		AY24		
5	IO_L65P_5		AW24		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L76N_6		AU42		
6	IO_L77P_6		AT39		
6	IO_L77N_6		AT40		
6	IO_L78P_6		AT41		
6	IO_L78N_6		AT42		
6	IO_L79P_6		AR38		
6	IO_L79N_6		AR39		
6	IO_L80P_6		AR37		
6	IO_L80N_6		AT38		
6	IO_L81P_6		AR40		
6	IO_L81N_6/VREF_6		AR41		
6	IO_L82P_6		AP36		
6	IO_L82N_6		AP37		
6	IO_L83P_6		AP35		
6	IO_L83N_6		AR36		
6	IO_L84P_6		AP38		
6	IO_L84N_6		AP39		
6	IO_L07P_6		AP41		
6	IO_L07N_6		AP42		
6	IO_L08P_6		AN35		
6	IO_L08N_6		AN36		
6	IO_L09P_6		AN37		
6	IO_L09N_6/VREF_6		AN38		
6	IO_L10P_6		AN41		
6	IO_L10N_6		AN42		
6	IO_L11P_6		AM33		
6	IO_L11N_6		AN34		
6	IO_L12P_6		AM36		
6	IO_L12N_6		AM37		
6	IO_L13P_6		AM38		
6	IO_L13N_6		AM39		
6	IO_L14P_6		AM34		
6	IO_L14N_6		AM35		
6	IO_L15P_6		AN40		
6	IO_L15N_6/VREF_6		AM40		
6	IO_L16P_6		AM41		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCAUX		AM11		
N/A	VCCAUX		AN33		
N/A	VCCAUX		AN10		
N/A	VCCAUX		AV39		
N/A	VCCAUX		AV4		
N/A	VCCAUX		AW38		
N/A	VCCAUX		AW22		
N/A	VCCAUX		AW21		
N/A	VCCAUX		AW5		
N/A	VCCAUX		AA42		
N/A	VCCAUX		AA41		
N/A	VCCAUX		AA2		
N/A	VCCAUX		AA1		
N/A	VCCAUX		Y42		
N/A	VCCAUX		Y1		
N/A	VCCAUX		L32		
N/A	VCCAUX		L11		
N/A	VCCAUX		K33		
N/A	VCCAUX		K10		
N/A	VCCAUX		E39		
N/A	VCCAUX		E4		
N/A	VCCAUX		D38		
N/A	VCCAUX		D22		
N/A	VCCAUX		D21		
N/A	VCCAUX		D5		
N/A	GND		AB38		
N/A	GND		AB35		
N/A	GND		AB32		
N/A	GND		AB26		
N/A	GND		AB25		
N/A	GND		AB24		
N/A	GND		AB23		
N/A	GND		AB22		
N/A	GND		AB21		
N/A	GND		AB20		
N/A	GND		AB19		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L56N_3	AC11	
3	IO_L56P_3	AC12	
3	IO_L55N_3	AD3	
3	IO_L55P_3	AE3	
3	IO_L54N_3	AE1	
3	IO_L54P_3	AE2	
3	IO_L53N_3	AC6	
3	IO_L53P_3	AC7	
3	IO_L52N_3	AF2	
3	IO_L52P_3	AF3	
3	IO_L51N_3/VREF_3	AF6	
3	IO_L51P_3	AG6	
3	IO_L50N_3	AD10	
3	IO_L50P_3	AD11	
3	IO_L49N_3	AG4	
3	IO_L49P_3	AG5	
3	IO_L48N_3	AF4	
3	IO_L48P_3	AG3	
3	IO_L47N_3	AC10	
3	IO_L47P_3	AD9	
3	IO_L46N_3	AG1	
3	IO_L46P_3	AG2	
3	IO_L45N_3/VREF_3	AG7	
3	IO_L45P_3	AH7	
3	IO_L44N_3	AC8	
3	IO_L44P_3	AD7	
3	IO_L43N_3	AH4	
3	IO_L43P_3	AH5	
3	IO_L42N_3	AH1	
3	IO_L42P_3	AH2	
3	IO_L41N_3	AE10	
3	IO_L41P_3	AE11	
3	IO_L40N_3	AJ6	
3	IO_L40P_3	AJ7	
3	IO_L39N_3/VREF_3	AH6	
3	IO_L39P_3	AJ5	
3	IO_L38N_3	AE8	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	