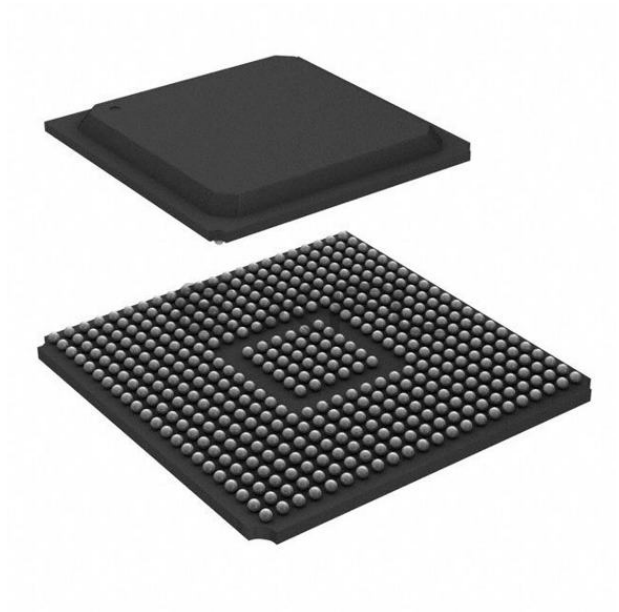
# AMD Xilinx - XC2VP4-6FG456I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 752 |
| Number of Logic Elements/Cells | 6768 |
| Total RAM Bits | 516096 |
| Number of I/O | 248 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp4-6fg456i |

## Virtex-II Pro Ordering Examples

Virtex-II Pro ordering examples are shown in Figure 1 (flip-chip package) and Figure 2 (Pb-free wire-bond package).

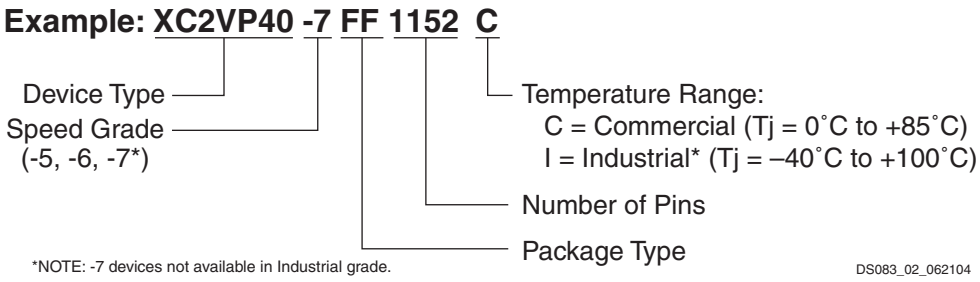



*Figure 1:* **Virtex-II Pro Ordering Example, Flip-Chip Package**

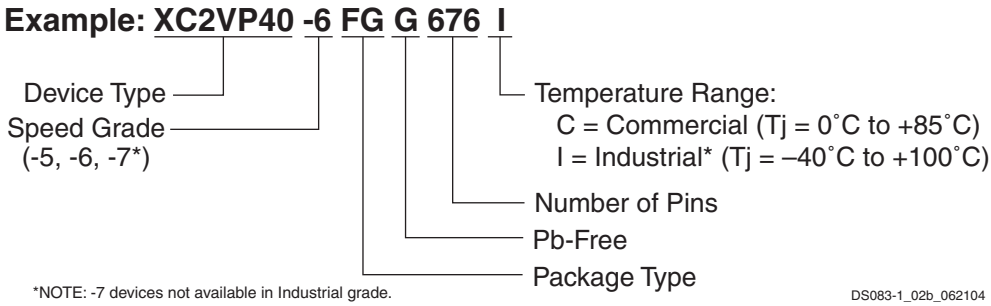



*Figure 2:* **Virtex-II Pro Ordering Example, Pb-Free Wire-Bond Package**

## Virtex-II Pro X Ordering Example

A Virtex-II Pro X ordering example is shown in Figure 3.

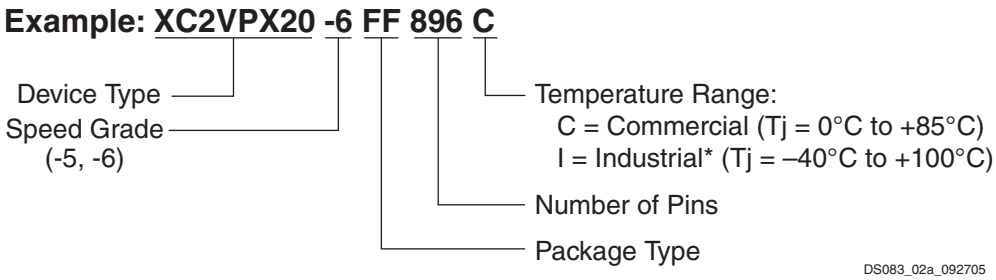



*Figure 3:* **Virtex-II Pro X Ordering Example, Flip-Chip Package**

cation is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Comma detection has been expanded beyond 10-bit symbol detection and alignment to include 8-bit symbol detection and alignment for 16-, 20-, 32-, and 40-bit paths. The ability to detect symbols, and then either align to 1-word, 2-word, or 4-word boundaries is included. The RXSLIDE input allows the user to “slide” or “slip” the alignment by one bit in each 16-, 20-, 32- and 40-bit mode at any time for SONET applications. Comma detection can be bypassed when needed.

### Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 6.

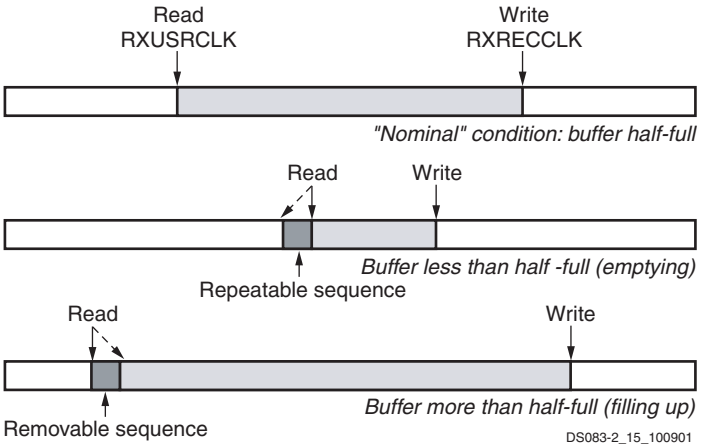



*Figure 6:* **Clock Correction in Receiver**

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 6, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 6, where the solid read pointer decrements to the value represented by the dashed pointer. By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 6, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

### Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 7.

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 7 shows the initial situation in the FPGA’s receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 7, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bond-

## 18-Bit x 18-Bit Multipliers

### *Introduction*

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

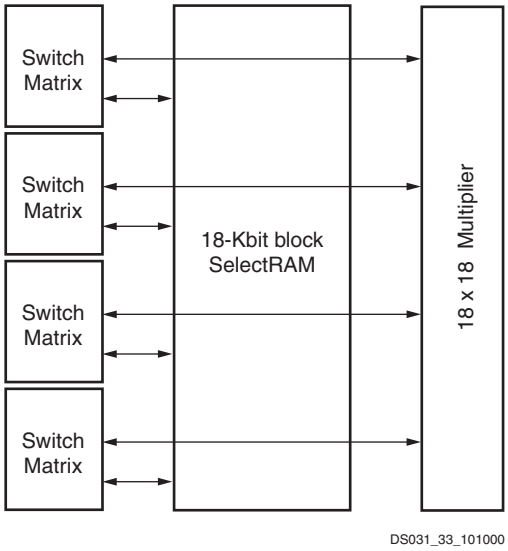



*Figure 53:* **SelectRAM+ and Multiplier Blocks**

### *Association With Block SelectRAM+ Memory*

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

### *Configuration*

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

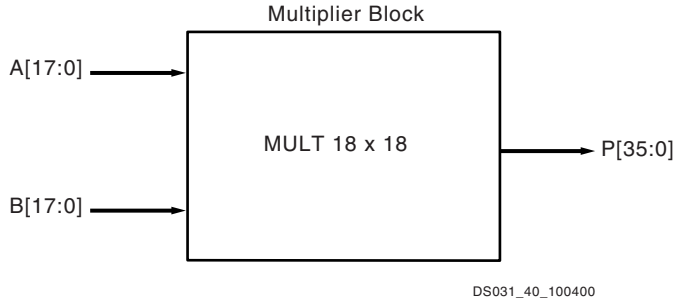



*Figure 54:* **Multiplier Block**

### *Locations / Organization*

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

*Table 26:* **Multiplier Resources**

| Device | Columns | Total Multipliers |
|---|---|---|
| XC2VP2 | 4 | 12 |
| XC2VP4 | 4 | 28 |
| XC2VP7 | 6 | 44 |
| XC2VP20 | 8 | 88 |
| XC2VP30 | 8 | 136 |
| XC2VPX20 | 8 | 88 |
| XC2VP40 | 10 | 192 |
| XC2VP50 | 12 | 232 |
| XC2VP70 | 14 | 328 |
| XC2VPX70 | 14 | 308 |
| XC2VP100 | 16 | 444 |

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

## Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The $V_{CCINT}$ power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 $V_{DC}$ to minimum supply voltages (see Table 2).

$V_{CCAUX}$ and $V_{CCO}$ can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on $V_{CCAUX}$, $V_{CCO}$, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

*Table 5:* **Power-On Current for Virtex-II Pro Devices**

| Symbol | Device | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XC2VP2 | XC2VP4 | XC2VP7 | XC2VP20 | XC2VPX20 | XC2VP30 | XC2VP40 | XC2VP50 | XC2VP70 | XC2VPX70 | XC2VP100 | |
| $I_{CCINTMIN}$ | 500 | 500 | 500 | 600 | 600 | 800 | 1050 | 1250 | 1700 | 1700 | 2200 | mA |
| $I_{CCAUXMIN}$ | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | mA |
| $I_{CCOMIN}$ | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | mA |

**Notes:**
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. $I_{CCOMIN}$ values listed here apply to the entire device (all banks).

## General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

$V_{CCAUX}$ powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. $V_{CCAUX}$ can share a power plane with $V_{CCO}$, but only if $V_{CCO}$ does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in $V_{CCAUX}$ voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

### *Master/Slave Serial Mode Parameters*

Clock timing for Slave Serial configuration programming is shown in Figure 8, with Master Serial clock timing shown in Figure 9. Programming parameters for both Slave and Master modes are given in Table 50.

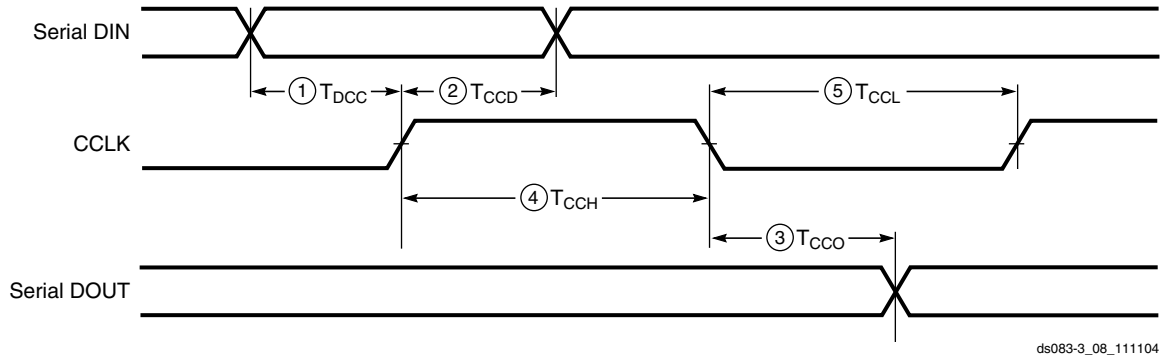



*Figure 8:* **Slave Serial Mode Timing Sequence**

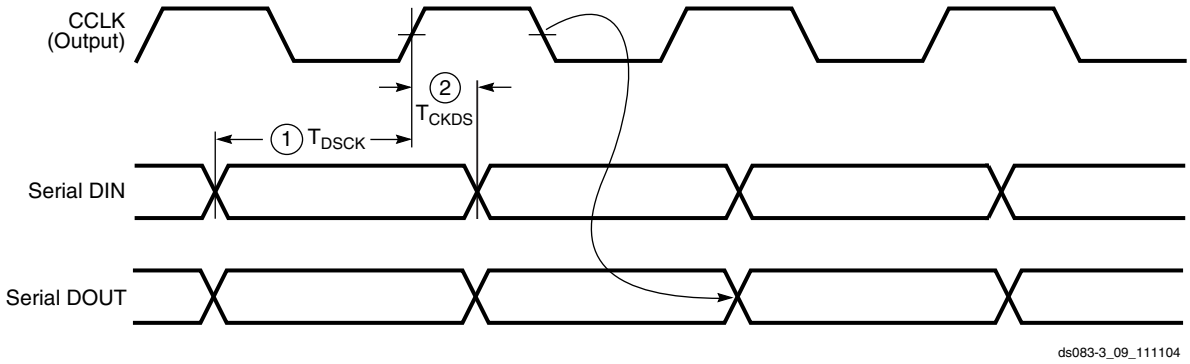


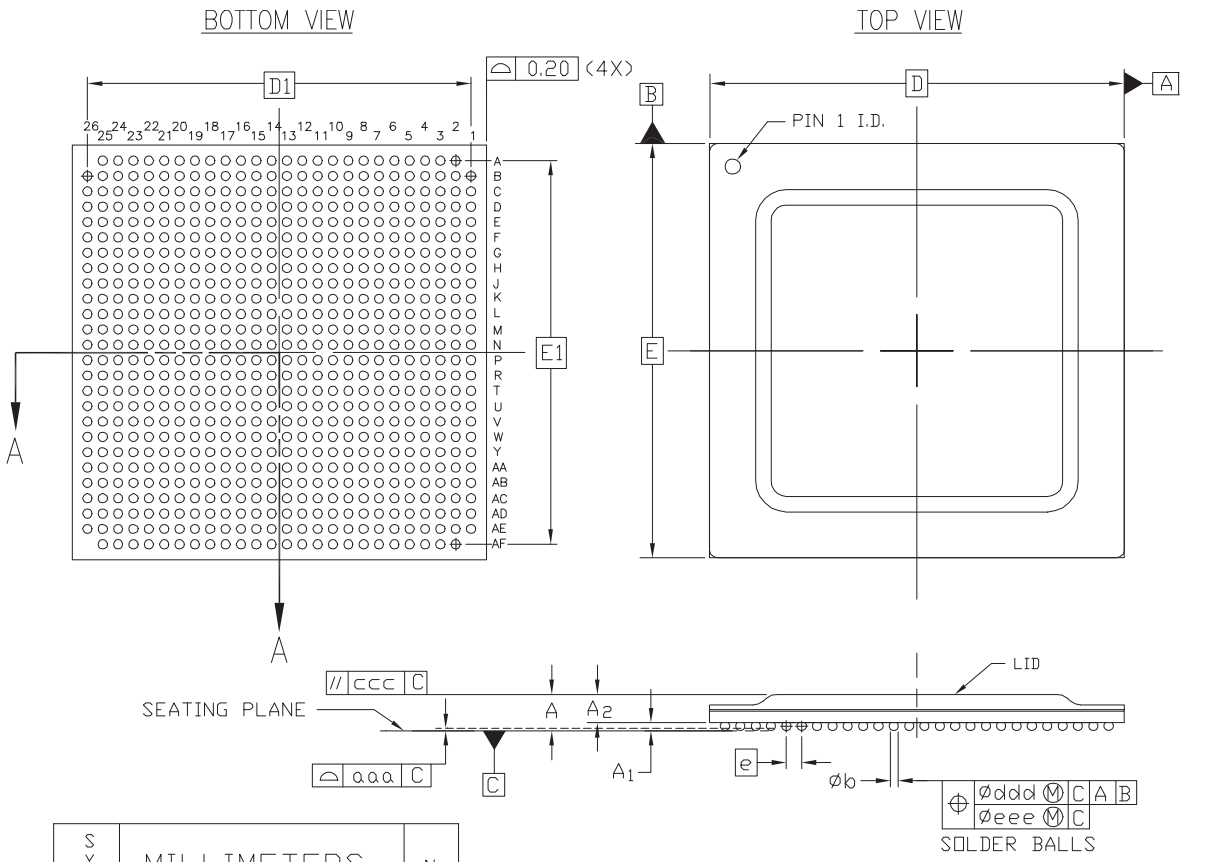

*Figure 9:* **Master Serial Mode Timing Sequence**

*Table 50:* **Master/Slave Serial Mode Timing Characteristics**

| | Description | Figure References | Symbol | Value | Units |
|---|---|---|---|---|---|
| CCLK | DIN setup/hold, slave mode (Figure 8) | 1/2 | $T_{DCC}/T_{CCD}$ | 5.0/0.0 | ns, min |
| | DIN setup/hold, master mode (Figure 9) | 1/2 | $T_{DSCK}/T_{CKDS}$ | 5.0/0.0 | ns, min |
| | DOUT | 3 | $T_{CCO}$ | 12.0 | ns, max |
| | High time | 4 | $T_{CCH}$ | 5.0 | ns, min |
| | Low time | 5 | $T_{CCL}$ | 5.0 | ns, min |
| | Maximum start-up frequency | | $F_{CC\_STARTUP}$ | 50 | MHz, max |
| | Maximum frequency | | $F_{CC\_SERIAL}$ | 66(1) | MHz, max |
| | Frequency tolerance, master mode with respect to nominal | | | +45%<br>–30% | |

**Notes:**
1. If no provision is made in the design to adjust the frequency of CCLK, $F_{CC\_SERIAL}$ should not exceed $F_{CC\_STARTUP}$.

## FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | | 2.45 | 2.65 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.15 | |
| D/E | 27.00 BASIC | | | |
| $D_1/E_1$ | 25.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| ccc | | | 0.35 | |
| ddd | | | 0.30 | |
| eee | | | 0.10 | |
| M | 26 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

*Figure 4:* **FF672 Flip-Chip Fine-Pitch BGA Package Specifications**

## FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 9, XC2VP7, XC2VP20, and XC2VP30 Virtex-II Pro devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 3 | IO_L39P_3 | | AE2 | NC | | |
| 3 | IO_L38N_3 | | AA7 | NC | | |
| 3 | IO_L38P_3 | | AA8 | NC | | |
| 3 | IO_L37N_3 | | AD3 | NC | | |
| 3 | IO_L37P_3 | | AD4 | NC | | |
| 3 | IO_L36N_3 | | AF1 | NC | | |
| 3 | IO_L36P_3 | | AF2 | NC | | |
| 3 | IO_L35N_3 | | AC5 | NC | | |
| 3 | IO_L35P_3 | | AC6 | NC | | |
| 3 | IO_L34N_3 | | AF3 | NC | | |
| 3 | IO_L34P_3 | | AF4 | NC | | |
| 3 | IO_L33N_3/VREF_3 | | AE3 | NC | | |
| 3 | IO_L33P_3 | | AE4 | NC | | |
| 3 | IO_L32N_3 | | AB7 | NC | | |
| 3 | IO_L32P_3 | | AB8 | NC | | |
| 3 | IO_L31N_3 | | AE5 | NC | | |
| 3 | IO_L31P_3 | | AF6 | NC | | |
| 3 | IO_L06N_3 | | AG1 | | | |
| 3 | IO_L06P_3 | | AG2 | | | |
| 3 | IO_L05N_3 | | AD5 | | | |
| 3 | IO_L05P_3 | | AD6 | | | |
| 3 | IO_L04N_3 | | AG3 | | | |
| 3 | IO_L04P_3 | | AH4 | | | |
| 3 | IO_L03N_3/VREF_3 | | AH1 | | | |
| 3 | IO_L03P_3 | | AH2 | | | |
| 3 | IO_L02N_3 | | AG5 | | | |
| 3 | IO_L02P_3 | | AH5 | | | |
| 3 | IO_L01N_3/VRP_3 | | AJ3 | | | |
| 3 | IO_L01P_3/VRN_3 | | AK3 | | | |
| | | | | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | | AG6 | | | |
| 4 | IO_L01P_4/INIT_B | | AF7 | | | |
| 4 | IO_L02N_4/D0/DIN(1) | | AC9 | | | |
| 4 | IO_L02P_4/D1 | | AD9 | | | |
| 4 | IO_L03N_4/D2 | | AG7 | | | |
| 4 | IO_L03P_4/D3 | | AH7 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 4 | VCCO_4 | | AA11 | | | |
| 4 | VCCO_4 | | AA10 | | | |
| 5 | VCCO_5 | | AB21 | | | |
| 5 | VCCO_5 | | AB20 | | | |
| 5 | VCCO_5 | | AB19 | | | |
| 5 | VCCO_5 | | AB18 | | | |
| 5 | VCCO_5 | | AA21 | | | |
| 5 | VCCO_5 | | AA20 | | | |
| 5 | VCCO_5 | | AA19 | | | |
| 5 | VCCO_5 | | AA18 | | | |
| 5 | VCCO_5 | | AA17 | | | |
| 5 | VCCO_5 | | AA16 | | | |
| 6 | VCCO_6 | | AB22 | | | |
| 6 | VCCO_6 | | AA22 | | | |
| 6 | VCCO_6 | | Y22 | | | |
| 6 | VCCO_6 | | Y21 | | | |
| 6 | VCCO_6 | | W22 | | | |
| 6 | VCCO_6 | | W21 | | | |
| 6 | VCCO_6 | | V22 | | | |
| 6 | VCCO_6 | | V21 | | | |
| 6 | VCCO_6 | | U21 | | | |
| 6 | VCCO_6 | | T21 | | | |
| 7 | VCCO_7 | | R21 | | | |
| 7 | VCCO_7 | | P21 | | | |
| 7 | VCCO_7 | | N22 | | | |
| 7 | VCCO_7 | | N21 | | | |
| 7 | VCCO_7 | | M22 | | | |
| 7 | VCCO_7 | | M21 | | | |
| 7 | VCCO_7 | | L22 | | | |
| 7 | VCCO_7 | | L21 | | | |
| 7 | VCCO_7 | | K22 | | | |
| 7 | VCCO_7 | | J22 | | | |
| | | | | | | |
| N/A | CCLK | | AC7 | | | |
| N/A | PROG_B | | G24 | | | |
| N/A | DONE | | AC8 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| N/A | GND | | AG19 | | | |
| N/A | GND | | AG12 | | | |
| N/A | GND | | AG9 | | | |
| N/A | GND | | AG4 | | | |
| N/A | GND | | AF26 | | | |
| N/A | GND | | AF5 | | | |
| N/A | GND | | AE25 | | | |
| N/A | GND | | AE18 | | | |
| N/A | GND | | AE13 | | | |
| N/A | GND | | AE6 | | | |
| N/A | GND | | AC30 | | | |
| N/A | GND | | AC1 | | | |
| N/A | GND | | Y28 | | | |
| N/A | GND | | Y25 | | | |
| N/A | GND | | Y20 | | | |
| N/A | GND | | Y11 | | | |
| N/A | GND | | Y6 | | | |
| N/A | GND | | Y3 | | | |
| N/A | GND | | W19 | | | |
| N/A | GND | | W18 | | | |
| N/A | GND | | W17 | | | |
| N/A | GND | | W16 | | | |
| N/A | GND | | W15 | | | |
| N/A | GND | | W14 | | | |
| N/A | GND | | W13 | | | |
| N/A | GND | | W12 | | | |
| N/A | GND | | V19 | | | |
| N/A | GND | | V18 | | | |
| N/A | GND | | V17 | | | |
| N/A | GND | | V16 | | | |
| N/A | GND | | V15 | | | |
| N/A | GND | | V14 | | | |
| N/A | GND | | V13 | | | |
| N/A | GND | | V12 | | | |
| N/A | GND | | U25 | | | |
| N/A | GND | | U19 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 6 | IO_L01P_6/VRN_6 | AJ30 | | | | |
| 6 | IO_L01N_6/VRP_6 | AJ31 | | | | |
| 6 | IO_L02P_6 | AJ27 | | | | |
| 6 | IO_L02N_6 | AJ28 | | | | |
| 6 | IO_L03P_6 | AK31 | | | | |
| 6 | IO_L03N_6/VREF_6 | AK32 | | | | |
| 6 | IO_L04P_6 | AH29 | | | | |
| 6 | IO_L04N_6 | AH30 | | | | |
| 6 | IO_L05P_6 | AH27 | | | | |
| 6 | IO_L05N_6 | AG28 | | | | |
| 6 | IO_L06P_6 | AL33 | | | | |
| 6 | IO_L06N_6 | AL34 | | | | |
| 6 | IO_L15P_6 | AG29 | NC | | | |
| 6 | IO_L15N_6/VREF_6 | AG30 | NC | | | |
| 6 | IO_L16P_6 | AK33 | NC | | | |
| 6 | IO_L16N_6 | AK34 | NC | | | |
| 6 | IO_L17P_6 | AF27 | NC | | | |
| 6 | IO_L17N_6 | AF28 | NC | | | |
| 6 | IO_L18P_6 | AJ33 | NC | | | |
| 6 | IO_L18N_6 | AJ34 | NC | | | |
| 6 | IO_L19P_6 | AH31 | NC | | | |
| 6 | IO_L19N_6 | AH32 | NC | | | |
| 6 | IO_L20P_6 | AD25 | NC | | | |
| 6 | IO_L20N_6 | AD26 | NC | | | |
| 6 | IO_L21P_6 | AG31 | NC | | | |
| 6 | IO_L21N_6/VREF_6 | AG32 | NC | | | |
| 6 | IO_L22P_6 | AF29 | NC | | | |
| 6 | IO_L22N_6 | AF30 | NC | | | |
| 6 | IO_L23P_6 | AE27 | NC | | | |
| 6 | IO_L23N_6 | AE28 | NC | | | |
| 6 | IO_L24P_6 | AH33 | NC | | | |
| 6 | IO_L24N_6 | AH34 | NC | | | |
| 6 | IO_L31P_6 | AF31 | | | | |
| 6 | IO_L31N_6 | AF32 | | | | |
| 6 | IO_L32P_6 | AC25 | | | | |
| 6 | IO_L32N_6 | AC26 | | | | |
| 6 | IO_L33P_6 | AG33 | | | | |
| 6 | IO_L33N_6/VREF_6 | AG34 | | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 6 | IO_L34P_6 | AE30 | | | | |
| 6 | IO_L34N_6 | AE31 | | | | |
| 6 | IO_L35P_6 | AD27 | | | | |
| 6 | IO_L35N_6 | AD28 | | | | |
| 6 | IO_L36P_6 | AF33 | | | | |
| 6 | IO_L36N_6 | AE33 | | | | |
| 6 | IO_L37P_6 | AD29 | | | | |
| 6 | IO_L37N_6 | AD30 | | | | |
| 6 | IO_L38P_6 | AB25 | | | | |
| 6 | IO_L38N_6 | AB26 | | | | |
| 6 | IO_L39P_6 | AD31 | | | | |
| 6 | IO_L39N_6/VREF_6 | AD32 | | | | |
| 6 | IO_L40P_6 | AC28 | | | | |
| 6 | IO_L40N_6 | AC29 | | | | |
| 6 | IO_L41P_6 | AB27 | | | | |
| 6 | IO_L41N_6 | AB28 | | | | |
| 6 | IO_L42P_6 | AE34 | | | | |
| 6 | IO_L42N_6 | AD34 | | | | |
| 6 | IO_L43P_6 | AC31 | | | | |
| 6 | IO_L43N_6 | AC32 | | | | |
| 6 | IO_L44P_6 | AA25 | | | | |
| 6 | IO_L44N_6 | AA26 | | | | |
| 6 | IO_L45P_6 | AD33 | | | | |
| 6 | IO_L45N_6/VREF_6 | AC33 | | | | |
| 6 | IO_L46P_6 | AB29 | | | | |
| 6 | IO_L46N_6 | AB30 | | | | |
| 6 | IO_L47P_6 | AA27 | | | | |
| 6 | IO_L47N_6 | AA28 | | | | |
| 6 | IO_L48P_6 | AB31 | | | | |
| 6 | IO_L48N_6 | AB32 | | | | |
| 6 | IO_L49P_6 | AA29 | | | | |
| 6 | IO_L49N_6 | AA30 | | | | |
| 6 | IO_L50P_6 | Y25 | | | | |
| 6 | IO_L50N_6 | Y26 | | | | |
| 6 | IO_L51P_6 | AC34 | | | | |
| 6 | IO_L51N_6/VREF_6 | AB34 | | | | |
| 6 | IO_L52P_6 | AA31 | | | | |
| 6 | IO_L52N_6 | AA32 | | | | |

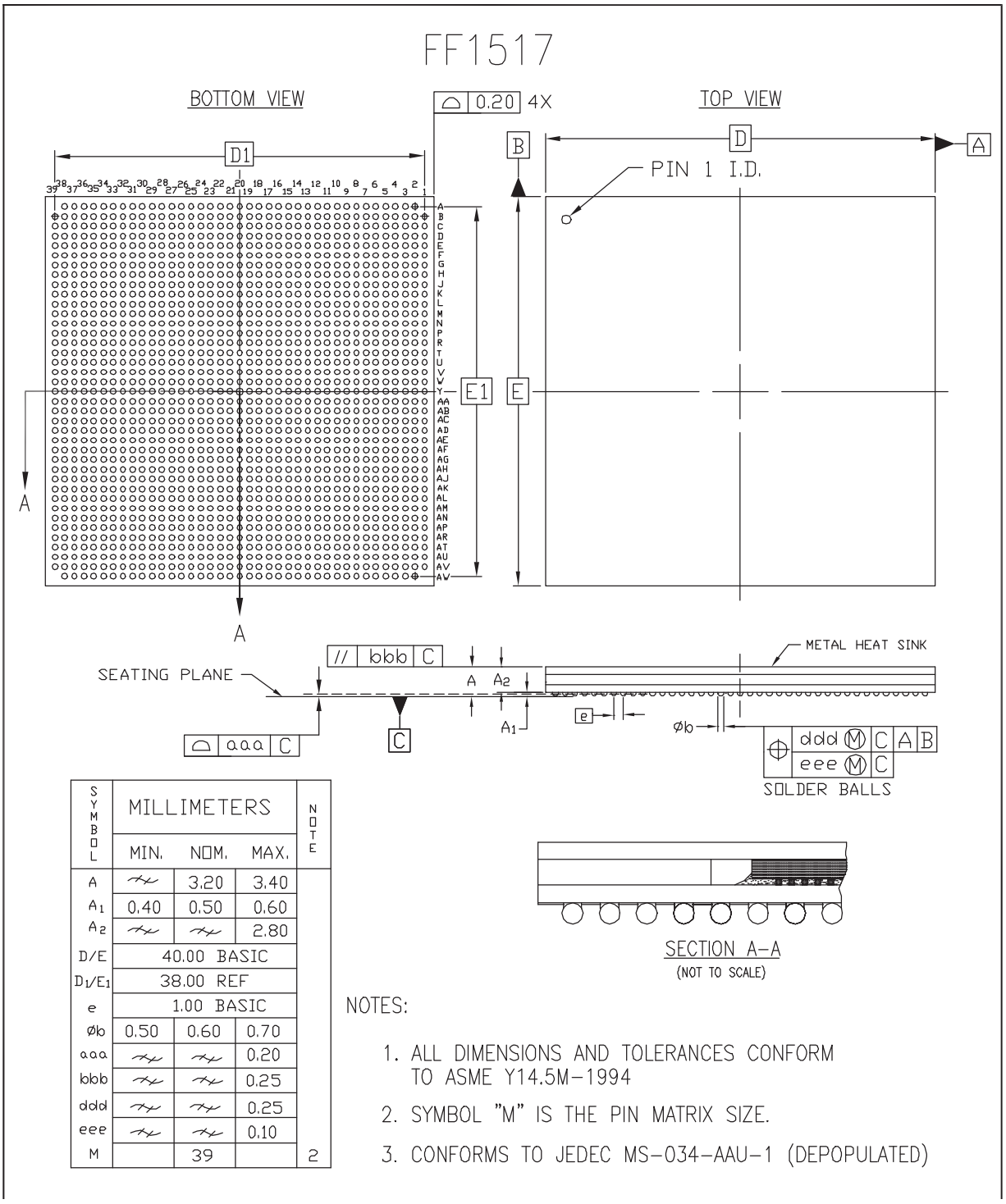
*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 2 | IO_L02P_2 | D9 | | |
| 2 | IO_L03N_2 | B7 | | |
| 2 | IO_L03P_2 | A7 | | |
| 2 | IO_L04N_2/VREF_2 | B6 | | |
| 2 | IO_L04P_2 | A6 | | |
| 2 | IO_L05N_2 | E8 | | |
| 2 | IO_L05P_2 | D8 | | |
| 2 | IO_L06N_2 | B4 | | |
| 2 | IO_L06P_2 | A4 | | |
| 2 | IO_L07N_2 | B3 | | |
| 2 | IO_L07P_2 | A3 | | |
| 2 | IO_L08N_2 | H7 | | |
| 2 | IO_L08P_2 | H8 | | |
| 2 | IO_L09N_2 | C6 | | |
| 2 | IO_L09P_2 | C7 | | |
| 2 | IO_L10N_2/VREF_2 | C5 | | |
| 2 | IO_L10P_2 | B5 | | |
| 2 | IO_L11N_2 | K8 | | |
| 2 | IO_L11P_2 | J8 | | |
| 2 | IO_L12N_2 | C1 | | |
| 2 | IO_L12P_2 | C2 | | |
| 2 | IO_L13N_2 | E7 | | |
| 2 | IO_L13P_2 | D7 | | |
| 2 | IO_L14N_2 | J6 | | |
| 2 | IO_L14P_2 | J7 | | |
| 2 | IO_L15N_2 | D5 | | |
| 2 | IO_L15P_2 | D6 | | |
| 2 | IO_L16N_2/VREF_2 | E4 | | |
| 2 | IO_L16P_2 | D4 | | |
| 2 | IO_L17N_2 | L9 | | |
| 2 | IO_L17P_2 | K9 | | |
| 2 | IO_L18N_2 | E3 | | |
| 2 | IO_L18P_2 | D3 | | |
| 2 | IO_L19N_2 | D1 | | |
| 2 | IO_L19P_2 | D2 | | |
| 2 | IO_L20N_2 | K7 | | |
| 2 | IO_L20P_2 | L7 | | |
| 2 | IO_L21N_2 | F6 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 3 | IO_L28P_3 | AH3 | | |
| 3 | IO_L27N_3/VREF_3 | AJ7 | | |
| 3 | IO_L27P_3 | AJ8 | | |
| 3 | IO_L26N_3 | AF8 | | |
| 3 | IO_L26P_3 | AF9 | | |
| 3 | IO_L25N_3 | AJ5 | | |
| 3 | IO_L25P_3 | AJ6 | | |
| 3 | IO_L24N_3 | AJ3 | | |
| 3 | IO_L24P_3 | AJ4 | | |
| 3 | IO_L23N_3 | AF10 | | |
| 3 | IO_L23P_3 | AG10 | | |
| 3 | IO_L22N_3 | AJ1 | | |
| 3 | IO_L22P_3 | AJ2 | | |
| 3 | IO_L21N_3/VREF_3 | AK6 | | |
| 3 | IO_L21P_3 | AK7 | | |
| 3 | IO_L20N_3 | AF11 | | |
| 3 | IO_L20P_3 | AF12 | | |
| 3 | IO_L19N_3 | AK4 | | |
| 3 | IO_L19P_3 | AK5 | | |
| 3 | IO_L18N_3 | AK1 | | |
| 3 | IO_L18P_3 | AK2 | | |
| 3 | IO_L17N_3 | AG9 | | |
| 3 | IO_L17P_3 | AH8 | | |
| 3 | IO_L16N_3 | AL6 | | |
| 3 | IO_L16P_3 | AL7 | | |
| 3 | IO_L15N_3/VREF_3 | AK3 | | |
| 3 | IO_L15P_3 | AL3 | | |
| 3 | IO_L14N_3 | AG11 | | |
| 3 | IO_L14P_3 | AH11 | | |
| 3 | IO_L13N_3 | AL1 | | |
| 3 | IO_L13P_3 | AL2 | | |
| 3 | IO_L12N_3 | AM6 | | |
| 3 | IO_L12P_3 | AM7 | | |
| 3 | IO_L11N_3 | AH10 | | |
| 3 | IO_L11P_3 | AJ9 | | |
| 3 | IO_L10N_3 | AL5 | | |
| 3 | IO_L10P_3 | AM4 | | |
| 3 | IO_L09N_3/VREF_3 | AM2 | | |

## FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | | 3.20 | 3.40 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.80 | |
| D/E | 40.00 BASIC | | | |
| $D_1/E_1$ | 38.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.25 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | | 39 | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAU-1 (DEPOPULATED)

*Figure 8:* **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | IO_L35N_3 | | AH11 | | |
| 3 | IO_L35P_3 | | AH12 | | |
| 3 | IO_L34N_3 | | AH5 | | |
| 3 | IO_L34P_3 | | AH6 | | |
| 3 | IO_L33N_3/VREF_3 | | AH9 | | |
| 3 | IO_L33P_3 | | AH10 | | |
| 3 | IO_L32N_3 | | AJ11 | | |
| 3 | IO_L32P_3 | | AJ12 | | |
| 3 | IO_L31N_3 | | AJ1 | | |
| 3 | IO_L31P_3 | | AJ2 | | |
| 3 | IO_L30N_3 | | AJ5 | | |
| 3 | IO_L30P_3 | | AJ6 | | |
| 3 | IO_L29N_3 | | AJ9 | | |
| 3 | IO_L29P_3 | | AJ10 | | |
| 3 | IO_L28N_3 | | AJ7 | | |
| 3 | IO_L28P_3 | | AJ8 | | |
| 3 | IO_L27N_3/VREF_3 | | AK1 | | |
| 3 | IO_L27P_3 | | AK2 | | |
| 3 | IO_L26N_3 | | AK11 | | |
| 3 | IO_L26P_3 | | AK12 | | |
| 3 | IO_L25N_3 | | AK3 | | |
| 3 | IO_L25P_3 | | AK4 | | |
| 3 | IO_L24N_3 | | AK5 | | |
| 3 | IO_L24P_3 | | AK6 | | |
| 3 | IO_L23N_3 | | AK9 | | |
| 3 | IO_L23P_3 | | AK10 | | |
| 3 | IO_L22N_3 | | AK7 | | |
| 3 | IO_L22P_3 | | AK8 | | |
| 3 | IO_L21N_3/VREF_3 | | AL2 | | |
| 3 | IO_L21P_3 | | AL3 | | |
| 3 | IO_L20N_3 | | AL11 | | |
| 3 | IO_L20P_3 | | AL12 | | |
| 3 | IO_L19N_3 | | AL4 | | |
| 3 | IO_L19P_3 | | AL5 | | |
| 3 | IO_L18N_3 | | AL7 | | |
| 3 | IO_L18P_3 | | AL8 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | TXPPAD7 | | A20 | | |
| N/A | GNDA7 | | C21 | | |
| N/A | RXPPAD7 | | A19 | | |
| N/A | RXNPAD7 | | A18 | | |
| N/A | VTRXPAD7 | | B19 | | |
| N/A | AVCCAUXRX7 | | B18 | | |
| N/A | AVCCAUXTX8 | | B16 | | |
| N/A | VTTXPAD8 | | B17 | | |
| N/A | TXNPAD8 | | A17 | | |
| N/A | TXPPAD8 | | A16 | | |
| N/A | GNDA8 | | C16 | | |
| N/A | RXPPAD8 | | A15 | | |
| N/A | RXNPAD8 | | A14 | | |
| N/A | VTRXPAD8 | | B15 | | |
| N/A | AVCCAUXRX8 | | B14 | | |
| N/A | AVCCAUXTX9 | | B12 | | |
| N/A | VTTXPAD9 | | B13 | | |
| N/A | TXNPAD9 | | A13 | | |
| N/A | TXPPAD9 | | A12 | | |
| N/A | GNDA9 | | C12 | | |
| N/A | RXPPAD9 | | A11 | | |
| N/A | RXNPAD9 | | A10 | | |
| N/A | VTRXPAD9 | | B11 | | |
| N/A | AVCCAUXRX9 | | B10 | | |
| N/A | AVCCAUXTX10 | | B8 | | |
| N/A | VTTXPAD10 | | B9 | | |
| N/A | TXNPAD10 | | A9 | | |
| N/A | TXPPAD10 | | A8 | | |
| N/A | GNDA10 | | C8 | | |
| N/A | RXPPAD10 | | A7 | | |
| N/A | RXNPAD10 | | A6 | | |
| N/A | VTRXPAD10 | | B7 | | |
| N/A | AVCCAUXRX10 | | B6 | | |
| N/A | AVCCAUXTX11 | | B4 | | |
| N/A | VTTXPAD11 | | B5 | | |
| N/A | TXNPAD11 | | A5 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | VCCINT | | U26 | | |
| N/A | VCCINT | | U17 | | |
| N/A | VCCINT | | U16 | | |
| N/A | VCCINT | | T27 | | |
| N/A | VCCINT | | T26 | | |
| N/A | VCCINT | | T25 | | |
| N/A | VCCINT | | T24 | | |
| N/A | VCCINT | | T23 | | |
| N/A | VCCINT | | T22 | | |
| N/A | VCCINT | | T21 | | |
| N/A | VCCINT | | T20 | | |
| N/A | VCCINT | | T19 | | |
| N/A | VCCINT | | T18 | | |
| N/A | VCCINT | | T17 | | |
| N/A | VCCINT | | T16 | | |
| N/A | VCCINT | | R28 | | |
| N/A | VCCINT | | R27 | | |
| N/A | VCCINT | | R26 | | |
| N/A | VCCINT | | R17 | | |
| N/A | VCCINT | | R16 | | |
| N/A | VCCINT | | R15 | | |
| N/A | VCCINT | | P29 | | |
| N/A | VCCINT | | P28 | | |
| N/A | VCCINT | | P27 | | |
| N/A | VCCINT | | P16 | | |
| N/A | VCCINT | | P15 | | |
| N/A | VCCINT | | P14 | | |
| N/A | VCCINT | | N30 | | |
| N/A | VCCINT | | N13 | | |
| N/A | VCCAUX | | AB42 | | |
| N/A | VCCAUX | | AB41 | | |
| N/A | VCCAUX | | AB2 | | |
| N/A | VCCAUX | | AB1 | | |
| N/A | VCCAUX | | AC42 | | |
| N/A | VCCAUX | | AC1 | | |
| N/A | VCCAUX | | AM32 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 1 | IO_L21P_1 | H13 | |
| 1 | IO_L20N_1 | L12 | |
| 1 | IO_L20P_1 | K12 | |
| 1 | IO_L19N_1 | B11 | |
| 1 | IO_L19P_1 | A11 | |
| 1 | IO_L09N_1/VREF_1 | E11 | |
| 1 | IO_L09P_1 | D11 | |
| 1 | IO_L08N_1 | J11 | |
| 1 | IO_L08P_1 | H11 | |
| 1 | IO_L07N_1 | G11 | |
| 1 | IO_L07P_1 | F11 | |
| 1 | IO_L06N_1 | B10 | |
| 1 | IO_L06P_1 | A10 | |
| 1 | IO_L05_1/No_Pair | G10 | |
| 1 | IO_L03N_1/VREF_1 | C10 | |
| 1 | IO_L03P_1 | C11 | |
| 1 | IO_L02N_1 | L11 | |
| 1 | IO_L02P_1 | K11 | |
| 1 | IO_L01N_1/VRP_1 | F10 | |
| 1 | IO_L01P_1/VRN_1 | E10 | |
| | | | |
| 2 | IO_L01N_2/VRP_2 | B8 | |
| 2 | IO_L01P_2/VRN_2 | A8 | |
| 2 | IO_L02N_2 | C9 | |
| 2 | IO_L02P_2 | B9 | |
| 2 | IO_L03N_2 | B7 | |
| 2 | IO_L03P_2 | A7 | |
| 2 | IO_L04N_2/VREF_2 | B6 | |
| 2 | IO_L04P_2 | A6 | |
| 2 | IO_L05N_2 | D8 | |
| 2 | IO_L05P_2 | D9 | |
| 2 | IO_L06N_2 | B4 | |
| 2 | IO_L06P_2 | A4 | |
| 2 | IO_L73N_2 | C7 | |
| 2 | IO_L73P_2 | C8 | |
| 2 | IO_L74N_2 | G9 | |
| 2 | IO_L74P_2 | F9 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 3 | IO_L38P_3 | AE9 | |
| 3 | IO_L37N_3 | AH3 | |
| 3 | IO_L37P_3 | AJ3 | |
| 3 | IO_L36N_3 | AJ1 | |
| 3 | IO_L36P_3 | AJ2 | |
| 3 | IO_L35N_3 | AE6 | |
| 3 | IO_L35P_3 | AE7 | |
| 3 | IO_L34N_3 | AK6 | |
| 3 | IO_L34P_3 | AK7 | |
| 3 | IO_L33N_3/VREF_3 | AK3 | |
| 3 | IO_L33P_3 | AK4 | |
| 3 | IO_L32N_3 | AE12 | |
| 3 | IO_L32P_3 | AF12 | |
| 3 | IO_L31N_3 | AL5 | |
| 3 | IO_L31P_3 | AL6 | |
| 3 | IO_L30N_3 | AL3 | |
| 3 | IO_L30P_3 | AL4 | |
| 3 | IO_L29N_3 | AF10 | |
| 3 | IO_L29P_3 | AF11 | |
| 3 | IO_L28N_3 | AK2 | |
| 3 | IO_L28P_3 | AL2 | |
| 3 | IO_L27N_3/VREF_3 | AL7 | |
| 3 | IO_L27P_3 | AM6 | |
| 3 | IO_L26N_3 | AF7 | |
| 3 | IO_L26P_3 | AF8 | |
| 3 | IO_L25N_3 | AM4 | |
| 3 | IO_L25P_3 | AM5 | |
| 3 | IO_L24N_3 | AM1 | |
| 3 | IO_L24P_3 | AM2 | |
| 3 | IO_L23N_3 | AG10 | |
| 3 | IO_L23P_3 | AG11 | |
| 3 | IO_L22N_3 | AM7 | |
| 3 | IO_L22P_3 | AN7 | |
| 3 | IO_L21N_3/VREF_3 | AN5 | |
| 3 | IO_L21P_3 | AN6 | |
| 3 | IO_L20N_3 | AG8 | |
| 3 | IO_L20P_3 | AG9 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| N/A | GND | AF1 | |
| N/A | GND | AC1 | |
| N/A | GND | Y1 | |
| N/A | GND | U1 | |
| N/A | GND | N1 | |
| N/A | GND | J1 | |
| N/A | GND | E1 | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.