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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	804
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ff1148c

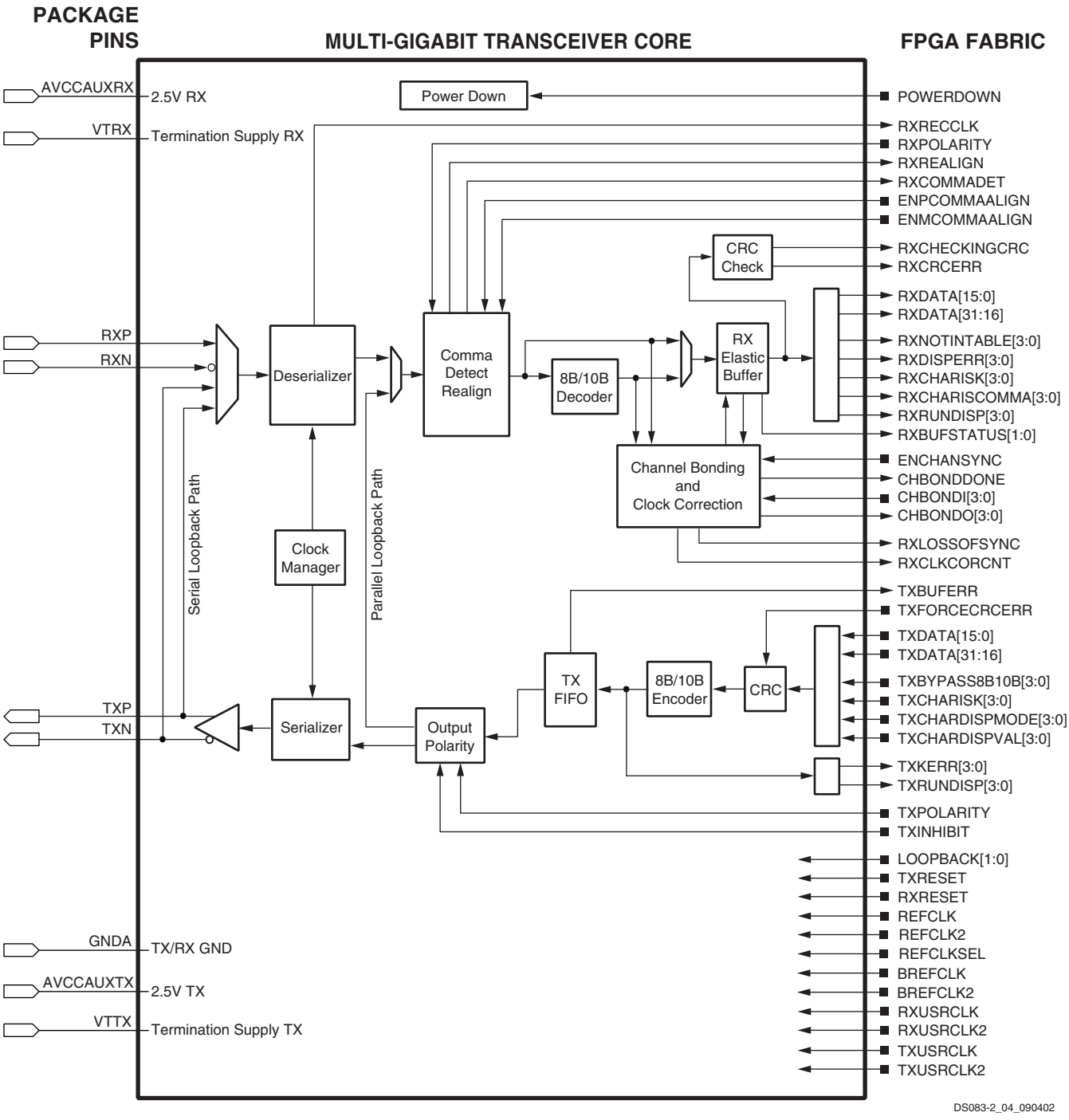

Figure 10: **RocketIO Transceiver Block Diagram**

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Table 11: **LVCMOS Programmable Currents (Sink and Source)**

SelectIO-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 23 shows the SSTL2, SSTL18, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

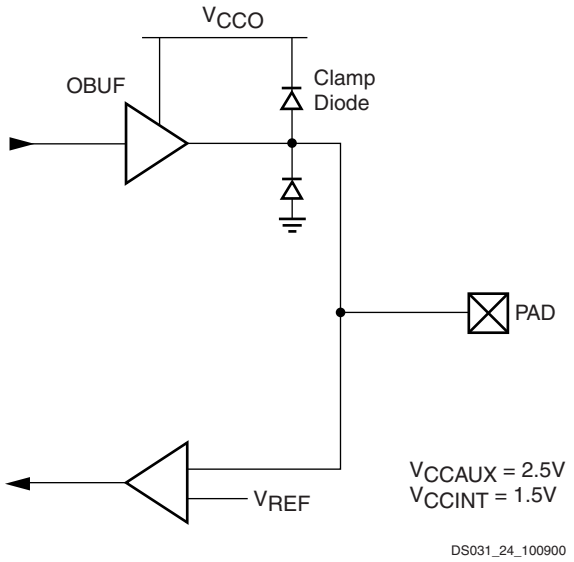

Figure 23: **SSTL or HSTL SelectIO-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II Pro uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set High, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set Low, the pull-up resistors are activated on user I/O pins.

All Virtex-II Pro IOBs (except RocketIO transceiver pins) support IEEE 1149.1 and IEEE 1532 compatible Boundary-Scan testing.

Input Path

The Virtex-II Pro IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II Pro device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 24 and Figure 25. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as DCI.

Readback

In this mode, configuration data from the Virtex-II Pro FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM+, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II Pro Platform FPGA User Guide.*

Bitstream Encryption

Virtex-II Pro devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II Pro devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the ***Virtex-II Pro Platform FPGA User Guide***. Your local FAE can also provide specific information on this feature.

Partial Reconfiguration

Partial reconfiguration of Virtex-II Pro devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

For more information on Partial Reconfiguration in Virtex-II Pro devices, please refer to Xilinx Application Note **XAPP290**, *Two Flows for Partial Reconfiguration*.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	• Revised Reset and Power sections. • Updated Table 8, which lists compatible input standards. [Table deleted in v2.6.] • Added Figure 28, Figure 29, and Figure 30, which provide examples illustrating the use of I/O standards.
09/27/02	2.2	• In section RocketIO Overview, corrected max number of MGTs from 16 to 24. • In section Input/Output Blocks (IOBs), added references to XAPP653 regarding implementation of 3.3V I/O standards.
11/20/02	2.3	• Table 8: Added rows for LVTTL, LVCMOS33, and PCI-X. • Table 8: Added LVTTL and LVCMOS33 to compatible 3.3V cells. [Table deleted in v2.6.] • Table 33: Correct bitstream lengths.
12/03/02	2.4	• Added mention of LVTTL and PCI with respect to SelectIO-Ultra configurations. See section Input/Output Individual Options and Figure 22.
01/20/03	2.5	• Added qualification to features vs. Virtex-II (open-drain output pin TDO does not have internal pull-up resistor) • Table 7: Added HSTL18 (I, II, III, & IV) and HSTL18_DCI (I,II, III & IV) to 1.8V VCCO row. [Table deleted in v2.6.] • Table 8: Numerous revisions. [Table deleted in v2.6.]

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–7		–6		–5		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Output Clock Jitter

Table 59: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			–7	–6	–5	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note (1)	Note (1)	Note (1)	ps

Notes:
1. Use the **Jitter Calculator** on the Xilinx website (http://www.xilinx.com/applications/web_ds_v2/jitter_calc.htm) for CLKFX and CLKFX180 output jitter.

Output Clock Phase Alignment

Table 60: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			–7	–6	–5	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK* outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L23N_6	Y6	NC		
6	IO_L24P_6	AA4	NC		
6	IO_L24N_6	AA3	NC		
6	IO_L31P_6	AA2			
6	IO_L31N_6	AA1			
6	IO_L33P_6	Y5			
6	IO_L33N_6/VREF_6	W5			
6	IO_L35P_6	Y4			
6	IO_L35N_6	Y3			
6	IO_L36P_6	Y2			
6	IO_L36N_6	Y1			
6	IO_L37P_6	W7			
6	IO_L37N_6	W6			
6	IO_L39P_6	W2			
6	IO_L39N_6/VREF_6	W1			
6	IO_L41P_6	V8			
6	IO_L41N_6	V7			
6	IO_L42P_6	V6			
6	IO_L42N_6	V5			
6	IO_L43P_6	V4			
6	IO_L43N_6	V3			
6	IO_L45P_6	V2			
6	IO_L45N_6/VREF_6	V1			
6	IO_L47P_6	U8			
6	IO_L47N_6	T8			
6	IO_L48P_6	U5			
6	IO_L48N_6	U4			
6	IO_L49P_6	U3			
6	IO_L49N_6	T3			
6	IO_L51P_6	U2			
6	IO_L51N_6/VREF_6	U1			
6	IO_L53P_6	T7			
6	IO_L53N_6	R7			
6	IO_L54P_6	T6			
6	IO_L54N_6	T5			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L27P_4/VREF_4	AL10	NC	NC		
4	IO_L37N_4	AE13				
4	IO_L37P_4	AF13				
4	IO_L38N_4	AG13				
4	IO_L38P_4	AH13				
4	IO_L39N_4	AJ11				
4	IO_L39P_4	AK11				
4	IO_L43N_4	AE14				
4	IO_L43P_4	AF14				
4	IO_L44N_4	AJ13				
4	IO_L44P_4	AK13				
4	IO_L45N_4	AL11				
4	IO_L45P_4/VREF_4	AM11				
4	IO_L46N_4	AE15				
4	IO_L46P_4	AF15				
4	IO_L47N_4	AG14				
4	IO_L47P_4	AH14				
4	IO_L48N_4	AL13				
4	IO_L48P_4	AL12				
4	IO_L49N_4	AD16				
4	IO_L49P_4	AE16				
4	IO_L50_4/No_Pair	AJ14				
4	IO_L53_4/No_Pair	AK14				
4	IO_L54N_4	AM14				
4	IO_L54P_4	AM13				
4	IO_L55N_4	AF16				
4	IO_L55P_4	AG16				
4	IO_L56N_4	AH15				
4	IO_L56P_4	AJ15				
4	IO_L57N_4	AL14				
4	IO_L57P_4/VREF_4	AL15				
4	IO_L67N_4	AD17				
4	IO_L67P_4	AE17				
4	IO_L68N_4	AH16				
4	IO_L68P_4	AJ16				
4	IO_L69N_4	AK16				
4	IO_L69P_4/VREF_4	AL16				
4	IO_L73N_4	AF17				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L21P_2	E6		
2	IO_L22N_2/VREF_2	F7		
2	IO_L22P_2	F8		
2	IO_L23N_2	M10		
2	IO_L23P_2	L10		
2	IO_L24N_2	G5		
2	IO_L24P_2	F5		
2	IO_L25N_2	F3		
2	IO_L25P_2	F4		
2	IO_L26N_2	M8		
2	IO_L26P_2	M9		
2	IO_L27N_2	F1		
2	IO_L27P_2	F2		
2	IO_L28N_2/VREF_2	G6		
2	IO_L28P_2	G7		
2	IO_L29N_2	M7		
2	IO_L29P_2	N8		
2	IO_L30N_2	G3		
2	IO_L30P_2	H4		
2	IO_L31N_2	G1		
2	IO_L31P_2	G2		
2	IO_L32N_2	N10		
2	IO_L32P_2	N11		
2	IO_L33N_2	H5		
2	IO_L33P_2	H6		
2	IO_L34N_2/VREF_2	H2		
2	IO_L34P_2	H3		
2	IO_L35N_2	N6		
2	IO_L35P_2	N7		
2	IO_L36N_2	K4		
2	IO_L36P_2	J4		
2	IO_L37N_2	J2		
2	IO_L37P_2	J3		
2	IO_L38N_2	P10		
2	IO_L38P_2	P11		
2	IO_L39N_2	K5		
2	IO_L39P_2	K6		
2	IO_L40N_2/VREF_2	L3		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L32P_7	N24		
7	IO_L32N_7	N25		
7	IO_L31P_7	G33		
7	IO_L31N_7	G34		
7	IO_L30P_7	H31		
7	IO_L30N_7	G32		
7	IO_L29P_7	N27		
7	IO_L29N_7	M28		
7	IO_L28P_7	G28		
7	IO_L28N_7/VREF_7	G29		
7	IO_L27P_7	F33		
7	IO_L27N_7	F34		
7	IO_L26P_7	M26		
7	IO_L26N_7	M27		
7	IO_L25P_7	F31		
7	IO_L25N_7	F32		
7	IO_L24P_7	F30		
7	IO_L24N_7	G30		
7	IO_L23P_7	L25		
7	IO_L23N_7	M25		
7	IO_L22P_7	F27		
7	IO_L22N_7/VREF_7	F28		
7	IO_L21P_7	E29		
7	IO_L21N_7	F29		
7	IO_L20P_7	L28		
7	IO_L20N_7	K28		
7	IO_L19P_7	D33		
7	IO_L19N_7	D34		
7	IO_L18P_7	D32		
7	IO_L18N_7	E32		
7	IO_L17P_7	K26		
7	IO_L17N_7	L26		
7	IO_L16P_7	D31		
7	IO_L16N_7/VREF_7	E31		
7	IO_L15P_7	D29		
7	IO_L15N_7	D30		
7	IO_L14P_7	J28		
7	IO_L14N_7	J29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L57N_5/VREF_5	AT23		
5	IO_L57P_5	AU23		
5	IO_L56N_5	AJ22		
5	IO_L56P_5	AK22		
5	IO_L55N_5	AN23		
5	IO_L55P_5	AP24		
5	IO_L54N_5	AL23		
5	IO_L54P_5	AM23		
5	IO_L53_5/No_Pair	AH23		
5	IO_L50_5/No_Pair	AG23		
5	IO_L49N_5	AR24		
5	IO_L49P_5	AR25		
5	IO_L48N_5	AL24		
5	IO_L48P_5	AM24		
5	IO_L47N_5	AH22		
5	IO_L47P_5	AJ23		
5	IO_L46N_5	AT25		
5	IO_L46P_5	AU25		
5	IO_L45N_5/VREF_5	AN25		
5	IO_L45P_5	AP25		
5	IO_L44N_5	AH24		
5	IO_L44P_5	AH25		
5	IO_L43N_5	AL25		
5	IO_L43P_5	AM25		
5	IO_L39N_5	AT26		
5	IO_L39P_5	AU26		
5	IO_L38N_5	AK24		
5	IO_L38P_5	AK25		
5	IO_L37N_5	AP26		
5	IO_L37P_5	AR26		
5	IO_L36N_5/VREF_5	AM26	NC	
5	IO_L36P_5	AN26	NC	
5	IO_L35N_5	AJ25	NC	
5	IO_L35P_5	AJ26	NC	
5	IO_L34N_5	AR27	NC	
5	IO_L34P_5	AT27	NC	
5	IO_L30N_5	AN27	NC	
5	IO_L30P_5	AP28	NC	

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L53P_6	AB30		
6	IO_L53N_6	AB31		
6	IO_L54P_6	AC38		
6	IO_L54N_6	AC39		
6	IO_L55P_6	AC34		
6	IO_L55N_6	AC35		
6	IO_L56P_6	AA28		
6	IO_L56N_6	AA29		
6	IO_L57P_6	AB38		
6	IO_L57N_6/VREF_6	AB39		
6	IO_L58P_6	AB36		
6	IO_L58N_6	AB37		
6	IO_L59P_6	AA30		
6	IO_L59N_6	AA31		
6	IO_L60P_6	AB34		
6	IO_L60N_6	AB35		
6	IO_L85P_6	AB32		
6	IO_L85N_6	AB33		
6	IO_L86P_6	AA27		
6	IO_L86N_6	Y27		
6	IO_L87P_6	AA36		
6	IO_L87N_6/VREF_6	AA37		
6	IO_L88P_6	AA34		
6	IO_L88N_6	AA35		
6	IO_L89P_6	Y28		
6	IO_L89N_6	Y29		
6	IO_L90P_6	AA32		
6	IO_L90N_6	AA33		
7	IO_L90P_7	Y36		
7	IO_L90N_7	Y37		
7	IO_L89P_7	Y31		
7	IO_L89N_7	W31		
7	IO_L88P_7	Y32		
7	IO_L88N_7/VREF_7	Y33		
7	IO_L87P_7	W36		
7	IO_L87N_7	W37		
7	IO_L86P_7	W27		

FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L01N_0/VRP_0		G34		
0	IO_L01P_0/VRN_0		H34		
0	IO_L02N_0		F34		
0	IO_L02P_0		E34		
0	IO_L03N_0		C34		
0	IO_L03P_0/VREF_0		D34		
0	IO_L05_0/No_Pair		K32		
0	IO_L06N_0		H33		
0	IO_L06P_0		J33		
0	IO_L07N_0		F33		
0	IO_L07P_0		G33		
0	IO_L08N_0		E33		
0	IO_L08P_0		D33		
0	IO_L09N_0		H32		
0	IO_L09P_0/VREF_0		J32		
0	IO_L19N_0		E32		
0	IO_L19P_0		F32		
0	IO_L20N_0		C33		
0	IO_L20P_0		C32		
0	IO_L21N_0		K31		
0	IO_L21P_0		L31		
0	IO_L25N_0		H31		
0	IO_L25P_0		J31		
0	IO_L26N_0		G31		
0	IO_L26P_0		F31		
0	IO_L27N_0		D31		
0	IO_L27P_0/VREF_0		E31		
0	IO_L28N_0		L30		
0	IO_L28P_0		M30		
0	IO_L29N_0		J30		
0	IO_L29P_0		K30		
0	IO_L30N_0		G30		
0	IO_L30P_0		H30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L02P_2		D7		
2	IO_L03N_2		E6		
2	IO_L03P_2		D6		
2	IO_L04N_2/VREF_2		G6		
2	IO_L04P_2		F7		
2	IO_L05N_2		D3		
2	IO_L05P_2		E3		
2	IO_L06N_2		D1		
2	IO_L06P_2		D2		
2	IO_L73N_2		E1		
2	IO_L73P_2		E2		
2	IO_L74N_2		F4		
2	IO_L74P_2		F3		
2	IO_L75N_2		F1		
2	IO_L75P_2		F2		
2	IO_L76N_2/VREF_2		G3		
2	IO_L76P_2		G4		
2	IO_L77N_2		G2		
2	IO_L77P_2		G1		
2	IO_L78N_2		G5		
2	IO_L78P_2		H6		
2	IO_L79N_2		H4		
2	IO_L79P_2		H5		
2	IO_L80N_2		H3		
2	IO_L80P_2		H2		
2	IO_L81N_2		H7		
2	IO_L81P_2		J8		
2	IO_L82N_2/VREF_2		J6		
2	IO_L82P_2		J7		
2	IO_L83N_2		J5		
2	IO_L83P_2		J4		
2	IO_L84N_2		J1		
2	IO_L84P_2		J2		
2	IO_L07N_2		K9		
2	IO_L07P_2		L10		
2	IO_L08N_2		K6		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD21		BB31		
N/A	GNDA21		AY31		
N/A	TXPPAD21		BB32		
N/A	TXNPAD21		BB33		
N/A	VTTXPAD21		BA33		
N/A	AVCCAUXTX21		BA32		
N/A	AVCCAUXRX22		BA34		
N/A	VTRXPAD22		BA35		
N/A	RXNPAD22		BB34		
N/A	RXPPAD22		BB35		
N/A	GNDA22		AY35		
N/A	TXPPAD22		BB36		
N/A	TXNPAD22		BB37		
N/A	VTTXPAD22		BA37		
N/A	AVCCAUXTX22		BA36		
N/A	AVCCAUXRX23		BA38		
N/A	VTRXPAD23		BA39		
N/A	RXNPAD23		BB38		
N/A	RXPPAD23		BB39		
N/A	GNDA23		AY39		
N/A	TXPPAD23		BB40		
N/A	TXNPAD23		BB41		
N/A	VTTXPAD23		BA41		
N/A	AVCCAUXTX23		BA40		
N/A	VCCINT		AB27		
N/A	VCCINT		AB16		
N/A	VCCINT		AC27		
N/A	VCCINT		AC16		
N/A	VCCINT		AD27		
N/A	VCCINT		AD16		
N/A	VCCINT		AE27		
N/A	VCCINT		AE16		
N/A	VCCINT		AF27		
N/A	VCCINT		AF26		
N/A	VCCINT		AF17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCINT		U26		
N/A	VCCINT		U17		
N/A	VCCINT		U16		
N/A	VCCINT		T27		
N/A	VCCINT		T26		
N/A	VCCINT		T25		
N/A	VCCINT		T24		
N/A	VCCINT		T23		
N/A	VCCINT		T22		
N/A	VCCINT		T21		
N/A	VCCINT		T20		
N/A	VCCINT		T19		
N/A	VCCINT		T18		
N/A	VCCINT		T17		
N/A	VCCINT		T16		
N/A	VCCINT		R28		
N/A	VCCINT		R27		
N/A	VCCINT		R26		
N/A	VCCINT		R17		
N/A	VCCINT		R16		
N/A	VCCINT		R15		
N/A	VCCINT		P29		
N/A	VCCINT		P28		
N/A	VCCINT		P27		
N/A	VCCINT		P16		
N/A	VCCINT		P15		
N/A	VCCINT		P14		
N/A	VCCINT		N30		
N/A	VCCINT		N13		
N/A	VCCAUX		AB42		
N/A	VCCAUX		AB41		
N/A	VCCAUX		AB2		
N/A	VCCAUX		AB1		
N/A	VCCAUX		AC42		
N/A	VCCAUX		AC1		
N/A	VCCAUX		AM32		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	