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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	804
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ff1148i

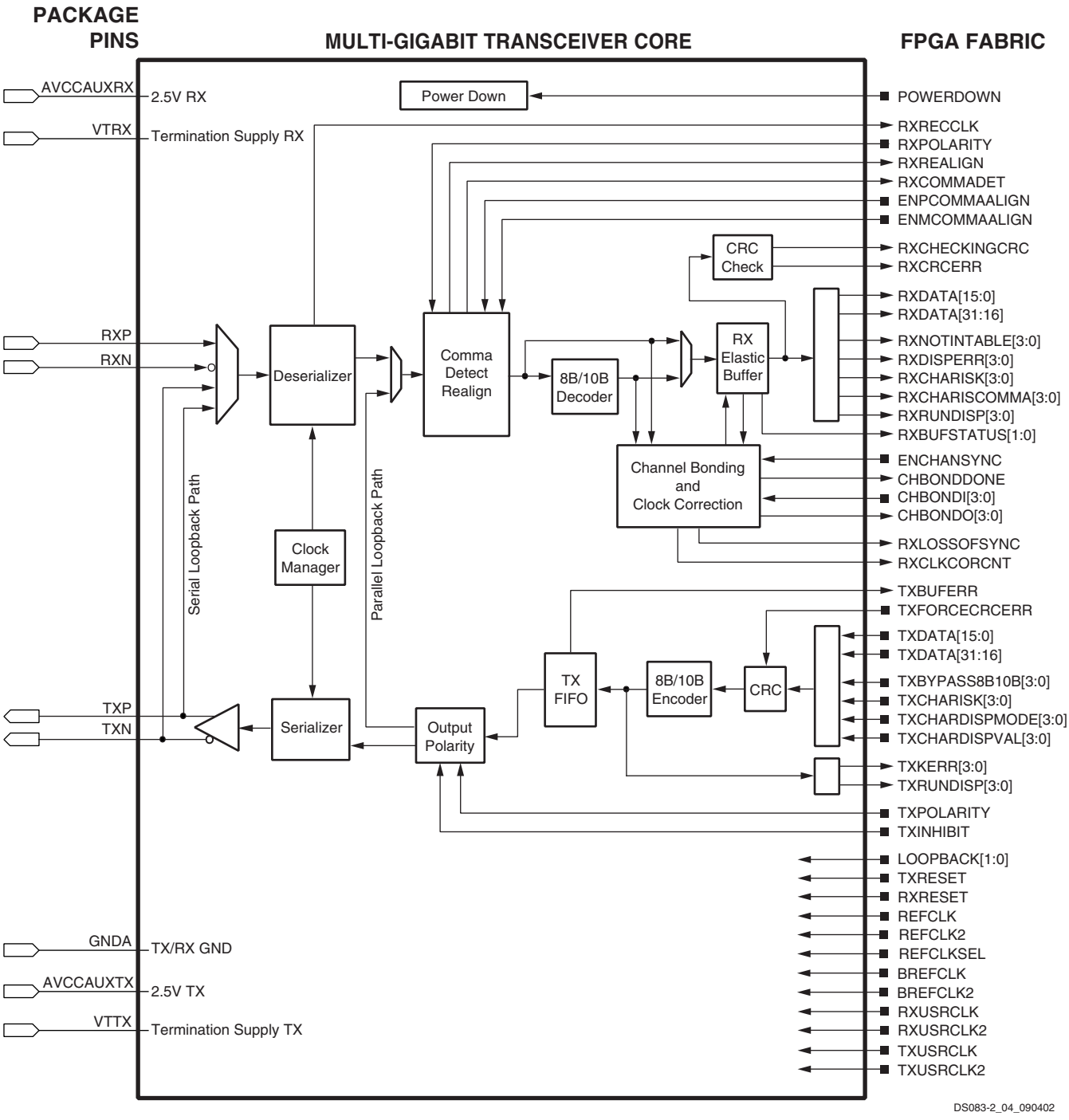


Figure 10: **RocketIO Transceiver Block Diagram**

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

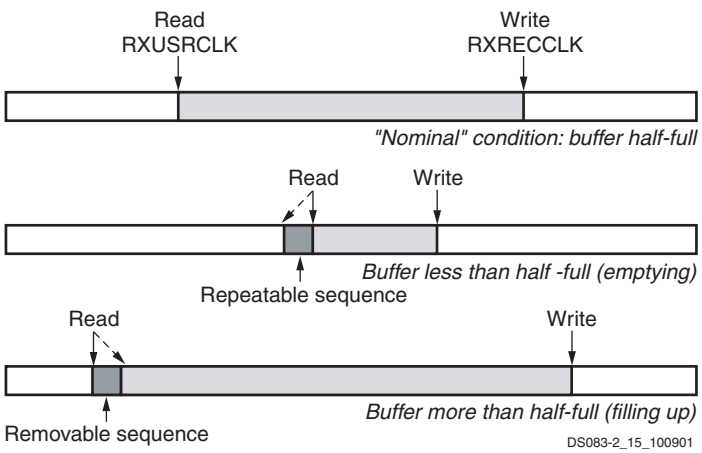


Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

nally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II Pro block SelectRAM+ memory to advantage.

Each block SelectRAM+ cell is a fully synchronous memory as illustrated in Figure 47. Input data bus and output data bus widths are identical.

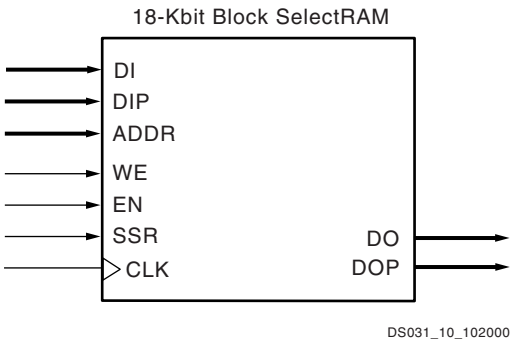


Figure 47: **18 Kb Block SelectRAM+ Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM+ has access to a common 18 Kb memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 22 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kb block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kb memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbs.

Table 22: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2).

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on V_{CCAUX}, V_{CCO}, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device											Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VPX20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VPX70	XC2VP100	
$I_{CCINTMIN}$	500	500	500	600	600	800	1050	1250	1700	1700	2200	mA
$I_{CCAUXMIN}$	250	250	250	250	250	250	250	250	250	250	250	mA
I_{CCOMIN}	100	100	100	100	100	100	100	100	100	100	100	mA

Notes:
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

Table 27: **RocketIO Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	1.0		3.125(1)	Gb/s
		Wirebond packages	1.0		2.5(1)	Gb/s
Serial data rate, half-speed clock(3) (2X oversampling)		Flipchip packages	0.600		1.0	Gb/s
		Wirebond packages	0.600		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}	2.126 Gb/s – 3.125 Gb/s			0.17	UI(2)
		1.0626 Gb/s – 2.125 Gb/s			0.08	UI
		1.0 Gb/s – 1.0625 Gb/s			0.05	UI
		600 Mb/s – 999 Mb/s			0.08(4)	UI
Serial data output random jitter	T_{RJ}	2.126 Gb/s – 3.125 Gb/s			0.18	UI
		1.0626 Gb/s – 2.125 Gb/s			0.19	UI
		1.0 Gb/s – 1.0625 Gb/s			0.18	UI
		600 Mb/s – 999 Mb/s			0.18(4)	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(5)	T_{TXLAT}	Including CRC		14	17	TXUSR CLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

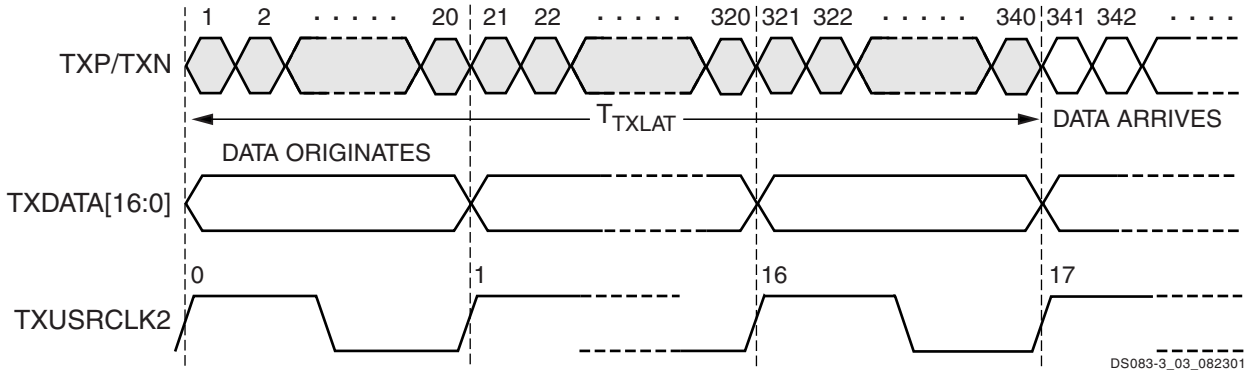


Figure 5: **RocketIO Transmit Latency (Maximum, Including CRC)**

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 55: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}.
3. IFF = Input Flip-Flop or Latch

Date	Version	Revision
09/15/05	4.4	• Table 2: Added Footnote (7) to AVCCAUXRX for RocketIO X (1.8V for all non-8B/10B-encoded data). • Table 3: - Power dissipation for 10.3125 Gb/s deleted. - Max $I_{CCAUXTX}$ and $I_{CCAUXRX}$ specifications added for Virtex-II Pro. • Table 11: Added specification for minimum p-p differential input voltage. • Table 22: - F_{GCLK}: Changed high end of range to 425 MHz. - T_{GJTT}: Changed measurement units to picoseconds and added maximum specifications for two bit rate ranges. - T_{LOCK}: Changed measurement units to microseconds and adderd typical specification. - T_{PHASE}: Changed measurement units to microseconds and adderd typical and maximum specifications. • Table 24: - All parameters: Deleted specifications for 10.3125 Gb/s. - T_{RJTOL}: Added typical specifications. - T_{JTOL}, T_{SJTOL}, and T_{DDJTOL}: Added typical and maximum specifications. • Table 26: Restructured table. Total Jitter parameter added. All jitter parameters respecified. • Table 28: Restructured table and added new specifications.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Table 15: Removed -7 designations for XC2VPX20 and XC2VPX70 devices.
03/05/07	4.6	*No changes in Module 3 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Changed I_{TRX} typical value in Table 3.

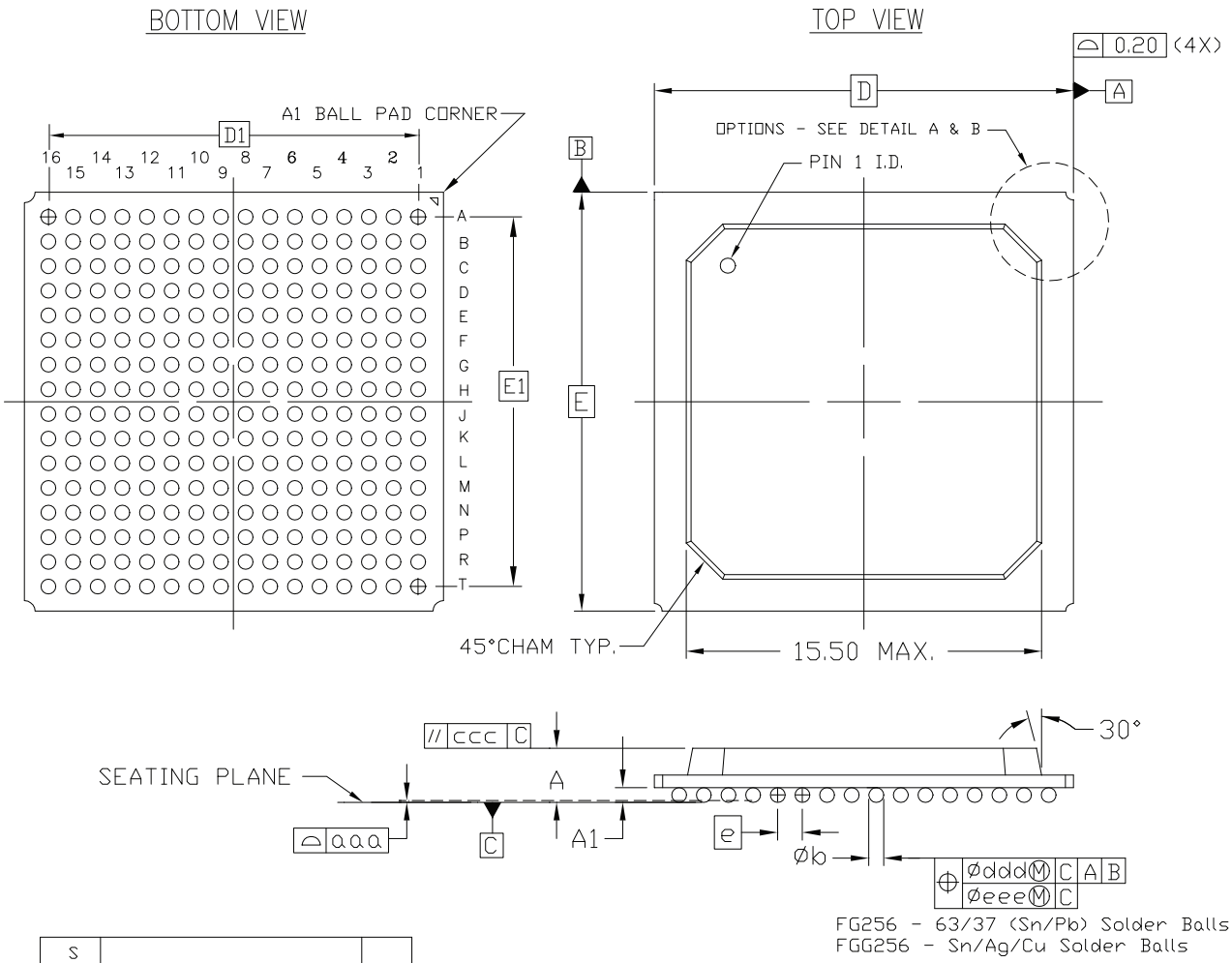
Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

Figure 1: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCAUX	L1			
N/A	VCCAUX	B21			
N/A	VCCAUX	B2			
N/A	VCCAUX	AB11			
N/A	VCCAUX	AA21			
N/A	VCCAUX	AA2			
N/A	VCCAUX	A12			
N/A	GND	Y3			
N/A	GND	Y20			
N/A	GND	W4			
N/A	GND	W19			
N/A	GND	V5			
N/A	GND	V18			
N/A	GND	P9			
N/A	GND	P14			
N/A	GND	P13			
N/A	GND	P12			
N/A	GND	P11			
N/A	GND	P10			
N/A	GND	N9			
N/A	GND	N14			
N/A	GND	N13			
N/A	GND	N12			
N/A	GND	N11			
N/A	GND	N10			
N/A	GND	M9			
N/A	GND	M14			
N/A	GND	M13			
N/A	GND	M12			
N/A	GND	M11			
N/A	GND	M10			
N/A	GND	M1			
N/A	GND	L9			
N/A	GND	L22			
N/A	GND	L14			
N/A	GND	L13			
N/A	GND	L12			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	IO_L02P_1		F7			
1	IO_L01N_1/VRP_1		E7			
1	IO_L01P_1/VRN_1		E6			
2	IO_L01N_2/VRP_2		A3			
2	IO_L01P_2/VRN_2		B3			
2	IO_L02N_2		G6			
2	IO_L02P_2		G5			
2	IO_L03N_2		C5			
2	IO_L03P_2		D5			
2	IO_L04N_2/VREF_2		C2			
2	IO_L04P_2		C1			
2	IO_L05N_2		J8			
2	IO_L05P_2		J7			
2	IO_L06N_2		C4			
2	IO_L06P_2		D3			
2	IO_L31N_2		D2	NC		
2	IO_L31P_2		D1	NC		
2	IO_L32N_2		H6	NC		
2	IO_L32P_2		H5	NC		
2	IO_L33N_2		E4	NC		
2	IO_L33P_2		E3	NC		
2	IO_L34N_2/VREF_2		E2	NC		
2	IO_L34P_2		E1	NC		
2	IO_L35N_2		K8	NC		
2	IO_L35P_2		K7	NC		
2	IO_L36N_2		F4	NC		
2	IO_L36P_2		F3	NC		
2	IO_L37N_2		F2	NC		
2	IO_L37P_2		F1	NC		
2	IO_L38N_2		J6	NC		
2	IO_L38P_2		J5	NC		
2	IO_L39N_2		G4	NC		
2	IO_L39P_2		G3	NC		
2	IO_L40N_2/VREF_2		G2	NC		
2	IO_L40P_2		G1	NC		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L57N_5/VREF_5	AT23		
5	IO_L57P_5	AU23		
5	IO_L56N_5	AJ22		
5	IO_L56P_5	AK22		
5	IO_L55N_5	AN23		
5	IO_L55P_5	AP24		
5	IO_L54N_5	AL23		
5	IO_L54P_5	AM23		
5	IO_L53_5/No_Pair	AH23		
5	IO_L50_5/No_Pair	AG23		
5	IO_L49N_5	AR24		
5	IO_L49P_5	AR25		
5	IO_L48N_5	AL24		
5	IO_L48P_5	AM24		
5	IO_L47N_5	AH22		
5	IO_L47P_5	AJ23		
5	IO_L46N_5	AT25		
5	IO_L46P_5	AU25		
5	IO_L45N_5/VREF_5	AN25		
5	IO_L45P_5	AP25		
5	IO_L44N_5	AH24		
5	IO_L44P_5	AH25		
5	IO_L43N_5	AL25		
5	IO_L43P_5	AM25		
5	IO_L39N_5	AT26		
5	IO_L39P_5	AU26		
5	IO_L38N_5	AK24		
5	IO_L38P_5	AK25		
5	IO_L37N_5	AP26		
5	IO_L37P_5	AR26		
5	IO_L36N_5/VREF_5	AM26	NC	
5	IO_L36P_5	AN26	NC	
5	IO_L35N_5	AJ25	NC	
5	IO_L35P_5	AJ26	NC	
5	IO_L34N_5	AR27	NC	
5	IO_L34P_5	AT27	NC	
5	IO_L30N_5	AN27	NC	
5	IO_L30P_5	AP28	NC	

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L75N_1/GCLK3P		G21		
1	IO_L75P_1/GCLK2S		F21		
1	IO_L74N_1/GCLK1P		J21		
1	IO_L74P_1/GCLK0S		K21		
1	IO_L73N_1		D20		
1	IO_L73P_1		C20		
1	IO_L69N_1/VREF_1		F20		
1	IO_L69P_1		E20		
1	IO_L68N_1		H20		
1	IO_L68P_1		J20		
1	IO_L67N_1		L20		
1	IO_L67P_1		K20		
1	IO_L66N_1/VREF_1		M20		
1	IO_L66P_1		M21		
1	IO_L65N_1		C19		
1	IO_L65P_1		D19		
1	IO_L64N_1		F19		
1	IO_L64P_1		E19		
1	IO_L60N_1		H19		
1	IO_L60P_1		G19		
1	IO_L59N_1		K19		
1	IO_L59P_1		J19		
1	IO_L58N_1		M19		
1	IO_L58P_1		L19		
1	IO_L57N_1/VREF_1		C17		
1	IO_L57P_1		C18		
1	IO_L56N_1		E18		
1	IO_L56P_1		E17		
1	IO_L55N_1		H18		
1	IO_L55P_1		G18		
1	IO_L54N_1		L18		
1	IO_L54P_1		K18		
1	IO_L53_1/No_Pair		D17		
1	IO_L50_1/No_Pair		D16		
1	IO_L49N_1		G17		
1	IO_L49P_1		F17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L87P_7		AA33		
7	IO_L87N_7		AA34		
7	IO_L86P_7		Y31		
7	IO_L86N_7		Y32		
7	IO_L85P_7		Y39		
7	IO_L85N_7		Y40		
7	IO_L60P_7		Y36		
7	IO_L60N_7		Y37		
7	IO_L59P_7		Y33		
7	IO_L59N_7		Y34		
7	IO_L58P_7		W41		
7	IO_L58N_7/VREF_7		W42		
7	IO_L57P_7		W39		
7	IO_L57N_7		W40		
7	IO_L56P_7		W31		
7	IO_L56N_7		W32		
7	IO_L55P_7		W37		
7	IO_L55N_7		W38		
7	IO_L54P_7		W35		
7	IO_L54N_7		W36		
7	IO_L53P_7		W33		
7	IO_L53N_7		W34		
7	IO_L52P_7		V41		
7	IO_L52N_7/VREF_7		V42		
7	IO_L51P_7		V38		
7	IO_L51N_7		V39		
7	IO_L50P_7		V31		
7	IO_L50N_7		U32		
7	IO_L49P_7		V35		
7	IO_L49N_7		V36		
7	IO_L48P_7		V32		
7	IO_L48N_7		V33		
7	IO_L47P_7		U31		
7	IO_L47N_7		T31		
7	IO_L46P_7		U41		
7	IO_L46N_7/VREF_7		U42		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD7		A20		
N/A	GNDA7		C21		
N/A	RXPPAD7		A19		
N/A	RXNPAD7		A18		
N/A	VTRXPAD7		B19		
N/A	AVCCAUXRX7		B18		
N/A	AVCCAUXTX8		B16		
N/A	VTTXPAD8		B17		
N/A	TXNPAD8		A17		
N/A	TXPPAD8		A16		
N/A	GNDA8		C16		
N/A	RXPPAD8		A15		
N/A	RXNPAD8		A14		
N/A	VTRXPAD8		B15		
N/A	AVCCAUXRX8		B14		
N/A	AVCCAUXTX9		B12		
N/A	VTTXPAD9		B13		
N/A	TXNPAD9		A13		
N/A	TXPPAD9		A12		
N/A	GNDA9		C12		
N/A	RXPPAD9		A11		
N/A	RXNPAD9		A10		
N/A	VTRXPAD9		B11		
N/A	AVCCAUXRX9		B10		
N/A	AVCCAUXTX10		B8		
N/A	VTTXPAD10		B9		
N/A	TXNPAD10		A9		
N/A	TXPPAD10		A8		
N/A	GNDA10		C8		
N/A	RXPPAD10		A7		
N/A	RXNPAD10		A6		
N/A	VTRXPAD10		B7		
N/A	AVCCAUXRX10		B6		
N/A	AVCCAUXTX11		B4		
N/A	VTTXPAD11		B5		
N/A	TXNPAD11		A5		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L79P_7	D41	
7	IO_L79N_7	D42	
7	IO_L78P_7	C39	
7	IO_L78N_7	C40	
7	IO_L77P_7	H34	
7	IO_L77N_7	H35	
7	IO_L76P_7	C37	
7	IO_L76N_7/VREF_7	D36	
7	IO_L75P_7	B38	
7	IO_L75N_7	C38	
7	IO_L74P_7	F34	
7	IO_L74N_7	G34	
7	IO_L73P_7	C35	
7	IO_L73N_7	C36	
7	IO_L06P_7	A39	
7	IO_L06N_7	B39	
7	IO_L05P_7	D34	
7	IO_L05N_7	D35	
7	IO_L04P_7	A37	
7	IO_L04N_7/VREF_7	B37	
7	IO_L03P_7	A36	
7	IO_L03N_7	B36	
7	IO_L02P_7	B34	
7	IO_L02N_7	C34	
7	IO_L01P_7/VRN_7	A35	
7	IO_L01N_7/VRP_7	B35	
7	VCCO_7	W39	
7	VCCO_7	P39	
7	VCCO_7	K39	
7	VCCO_7	F39	
7	VCCO_7	D37	
7	VCCO_7	W35	
7	VCCO_7	P35	
7	VCCO_7	K35	
7	VCCO_7	M33	
7	VCCO_7	H33	

Date	Version	Revision
11/17/04	4.1	• Table 4: Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
03/01/05	4.2	• Table 3: Corrected number of Differential I/O Pairs for XC2VP30-FF1152 from 340 to 316. • Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”.
06/20/05	4.3	*No changes in Module 4 for this revision.*
09/15/05	4.4	*No changes in Module 4 for this revision.*
10/10/05	4.5	*No changes in Module 4 for this revision.*
03/05/07	4.6	• Figure 2, page 29: Corrected NOTE 3. • Figure 7, page 161: Updated with drawing showing correct heat sink profile and detail.
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Updated Figure 3, page 50, with the newest FG676/FGG676 mechanical drawing.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)