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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	804
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ffg1148c

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

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The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

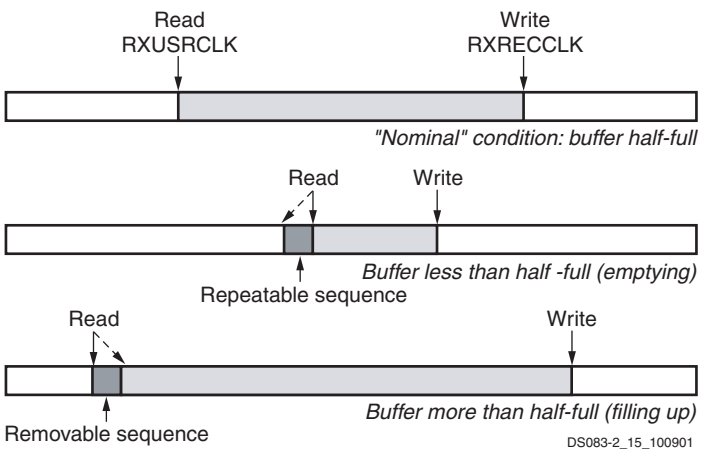

Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVTTL(1)	3.3	3.3	N/R	N/R	N/R
LVCMOS33(1)			N/R	N/R	N/R
LVDCI_33(1)			N/R	Series	N/R
PCIX(2)			N/R	N/R	N/R
PCI33_3(2)			N/R	N/R	N/R
PCI66_3(2)			N/R	N/R	N/R
LVDS_25	2.5	Note (3)	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
LVPECL_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
LVDS_25_DT			N/R	N/R	N/R
LVDSEXT_25_DT			N/R	N/R	N/R
LDT_25_DT			N/R	N/R	N/R
ULVDS_25_DT			N/R	N/R	N/R

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	Note (3)	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	Note (3)	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	Note (3)	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. See application note **XAPP659** for more detailed information.
2. See application note **XAPP653** for more detailed information.
3. Pin voltage must not exceed V_{CCO}.
4. N/R = no requirement.

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

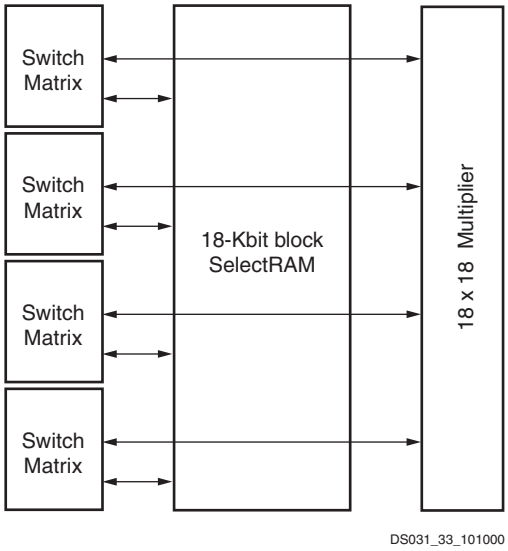

Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

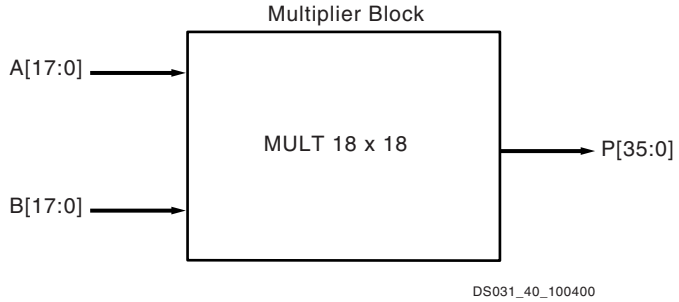

Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VTRXPAD6	B9			
N/A	AVCCAUXRX6	B10			
N/A	AVCCAUXTX7	B14			
N/A	VTTXPAD7	B13			
N/A	TXNPAD7	A13			
N/A	TXPPAD7	A14			
N/A	GNDA7	C14			
N/A	RXPPAD7	A15			
N/A	RXNPAD7	A16			
N/A	VTRXPAD7	B15			
N/A	AVCCAUXRX7	B16			
N/A	AVCCAUXTX9	B18	NC	NC	
N/A	VTTXPAD9	B17	NC	NC	
N/A	TXNPAD9	A17	NC	NC	
N/A	TXPPAD9	A18	NC	NC	
N/A	GNDA9	C17	NC	NC	
N/A	RXPPAD9	A19	NC	NC	
N/A	RXNPAD9	A20	NC	NC	
N/A	VTRXPAD9	B19	NC	NC	
N/A	AVCCAUXRX9	B20	NC	NC	
N/A	AVCCAUXRX16	AA20	NC	NC	
N/A	VTRXPAD16	AA19	NC	NC	
N/A	RXNPAD16	AB20	NC	NC	
N/A	RXPPAD16	AB19	NC	NC	
N/A	GNDA16	Y17	NC	NC	
N/A	TXPPAD16	AB18	NC	NC	
N/A	TXNPAD16	AB17	NC	NC	
N/A	VTTXPAD16	AA17	NC	NC	
N/A	AVCCAUXTX16	AA18	NC	NC	
N/A	AVCCAUXRX18	AA16			
N/A	VTRXPAD18	AA15			
N/A	RXNPAD18	AB16			
N/A	RXPPAD18	AB15			
N/A	GNDA18	Y14			
N/A	TXPPAD18	AB14			
N/A	TXNPAD18	AB13			
N/A	VTTXPAD18	AA13			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
2	IO_L31P_2	F26			
2	IO_L32N_2	G22			
2	IO_L32P_2	H22			
2	IO_L34N_2/VREF_2	G23			
2	IO_L34P_2	G24			
2	IO_L36N_2	G25			
2	IO_L36P_2	G26			
2	IO_L37N_2	H20			
2	IO_L37P_2	H21			
2	IO_L38N_2	H25			
2	IO_L38P_2	H26			
2	IO_L40N_2/VREF_2	J19			
2	IO_L40P_2	J20			
2	IO_L42N_2	J21			
2	IO_L42P_2	J22			
2	IO_L43N_2	J23			
2	IO_L43P_2	J24			
2	IO_L44N_2	J25			
2	IO_L44P_2	J26			
2	IO_L46N_2/VREF_2	K19			
2	IO_L46P_2	L19			
2	IO_L48N_2	K22			
2	IO_L48P_2	K23			
2	IO_L49N_2	K24			
2	IO_L49P_2	L24			
2	IO_L50N_2	K25			
2	IO_L50P_2	K26			
2	IO_L52N_2/VREF_2	L20			
2	IO_L52P_2	M20			
2	IO_L54N_2	L21			
2	IO_L54P_2	L22			
2	IO_L55N_2	L25			
2	IO_L55P_2	L26			
2	IO_L56N_2	M18			
2	IO_L56P_2	M19			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L41N_2		L8	NC		
2	IO_L41P_2		L7	NC		
2	IO_L42N_2		H4	NC		
2	IO_L42P_2		H3	NC		
2	IO_L43N_2		H2			
2	IO_L43P_2		J2			
2	IO_L44N_2		M8			
2	IO_L44P_2		M7			
2	IO_L45N_2		K6			
2	IO_L45P_2		K5			
2	IO_L46N_2/VREF_2		J1			
2	IO_L46P_2		K1			
2	IO_L47N_2		M6			
2	IO_L47P_2		M5			
2	IO_L48N_2		J4			
2	IO_L48P_2		J3			
2	IO_L49N_2		K2			
2	IO_L49P_2		L2			
2	IO_L50N_2		N8			
2	IO_L50P_2		N7			
2	IO_L51N_2		K4			
2	IO_L51P_2		K3			
2	IO_L52N_2/VREF_2		L1			
2	IO_L52P_2		M1			
2	IO_L53N_2		N6			
2	IO_L53P_2		N5			
2	IO_L54N_2		L5			
2	IO_L54P_2		L4			
2	IO_L55N_2		M2			
2	IO_L55P_2		N2			
2	IO_L56N_2		P9			
2	IO_L56P_2		R9			
2	IO_L57N_2		M4			
2	IO_L57P_2		M3			
2	IO_L58N_2/VREF_2		N1			
2	IO_L58P_2		P1			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L06P_3	AL2				
3	IO_L05N_3	AG7				
3	IO_L05P_3	AH8				
3	IO_L04N_3	AH5				
3	IO_L04P_3	AH6				
3	IO_L03N_3/VREF_3	AK3				
3	IO_L03P_3	AK4				
3	IO_L02N_3	AJ7				
3	IO_L02P_3	AJ8				
3	IO_L01N_3/VRP_3	AJ4				
3	IO_L01P_3/VRN_3	AJ5				
4	IO_L01N_4/BUSY/DOUT(1)	AL5				
4	IO_L01P_4/INIT_B	AL6				
4	IO_L02N_4/D0/DIN(1)	AG9				
4	IO_L02P_4/D1	AH9				
4	IO_L03N_4/D2	AK6				
4	IO_L03P_4/D3	AK7				
4	IO_L05_4/No_Pair	AF10				
4	IO_L06N_4/VRP_4	AL7				
4	IO_L06P_4/VRN_4	AM7				
4	IO_L07N_4	AE11				
4	IO_L07P_4/VREF_4	AF11				
4	IO_L08N_4	AG10				
4	IO_L08P_4	AH10				
4	IO_L09N_4	AK8				
4	IO_L09P_4/VREF_4	AL8				
4	IO_L19N_4	AE12	NC	NC		
4	IO_L19P_4	AF12	NC	NC		
4	IO_L20N_4	AJ9	NC	NC		
4	IO_L20P_4	AK9	NC	NC		
4	IO_L21N_4	AL9	NC	NC		
4	IO_L21P_4	AM9	NC	NC		
4	IO_L25N_4	AG11	NC	NC		
4	IO_L25P_4	AH11	NC	NC		
4	IO_L26N_4	AH12	NC	NC		
4	IO_L26P_4	AJ12	NC	NC		
4	IO_L27N_4	AK10	NC	NC		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M12		
N/A	VCCINT	AD11		
N/A	VCCINT	L11		
N/A	VCCAUX	AN34		
N/A	VCCAUX	AG34		
N/A	VCCAUX	U34		
N/A	VCCAUX	H34		
N/A	VCCAUX	B34		
N/A	VCCAUX	AP33		
N/A	VCCAUX	A33		
N/A	VCCAUX	AP27		
N/A	VCCAUX	A27		
N/A	VCCAUX	AP17		
N/A	VCCAUX	A17		
N/A	VCCAUX	AP8		
N/A	VCCAUX	A8		
N/A	VCCAUX	AP2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AN1		
N/A	VCCAUX	AG1		
N/A	VCCAUX	U1		
N/A	VCCAUX	H1		
N/A	VCCAUX	B1		
N/A	GND	AK34		
N/A	GND	AF34		
N/A	GND	AB34		
N/A	GND	W34		
N/A	GND	V34		
N/A	GND	T34		
N/A	GND	N34		
N/A	GND	J34		
N/A	GND	E34		
N/A	GND	AN33		
N/A	GND	B33		
N/A	GND	AM32		
N/A	GND	C32		
N/A	GND	AP30		
N/A	GND	AK30		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L59P_0	N21		
0	IO_L60N_0	E23		
0	IO_L60P_0	F22		
0	IO_L64N_0	D22		
0	IO_L64P_0	E22		
0	IO_L65N_0	H21		
0	IO_L65P_0	H20		
0	IO_L66N_0	G22		
0	IO_L66P_0/VREF_0	G21		
0	IO_L67N_0	D21		
0	IO_L67P_0	E21		
0	IO_L68N_0	J21		
0	IO_L68P_0	K21		
0	IO_L69N_0	C22		
0	IO_L69P_0/VREF_0	C21		
0	IO_L73N_0	F21		
0	IO_L73P_0	F20		
0	IO_L74N_0/GCLK7P	L21		
0	IO_L74P_0/GCLK6S	M21		
0	IO_L75N_0/GCLK5P	D20		
0	IO_L75P_0/GCLK4S	E20		
1	IO_L75N_1/GCLK3P	K20		
1	IO_L75P_1/GCLK2S	J20		
1	IO_L74N_1/GCLK1P	N20		
1	IO_L74P_1/GCLK0S	M20		
1	IO_L73N_1	E19		
1	IO_L73P_1	D19		
1	IO_L69N_1/VREF_1	G19		
1	IO_L69P_1	F19		
1	IO_L68N_1	L19		
1	IO_L68P_1	K19		
1	IO_L67N_1	J19		
1	IO_L67P_1	H19		
1	IO_L66N_1/VREF_1	C19		
1	IO_L66P_1	C18		
1	IO_L65N_1	N19		
1	IO_L65P_1	M19		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L64N_1	E18		
1	IO_L64P_1	D18		
1	IO_L60N_1	G18		
1	IO_L60P_1	F18		
1	IO_L59N_1	L18		
1	IO_L59P_1	K18		
1	IO_L58N_1	J18		
1	IO_L58P_1	H18		
1	IO_L57N_1/VREF_1	D17		
1	IO_L57P_1	C17		
1	IO_L56N_1	N18		
1	IO_L56P_1	M18		
1	IO_L55N_1	E17		
1	IO_L55P_1	E16		
1	IO_L54N_1	G17		
1	IO_L54P_1	F16		
1	IO_L53_1/No_Pair	J17		
1	IO_L50_1/No_Pair	H17		
1	IO_L49N_1	J16		
1	IO_L49P_1	H16		
1	IO_L48N_1	D15		
1	IO_L48P_1	C15		
1	IO_L47N_1	L17		
1	IO_L47P_1	K16		
1	IO_L46N_1	F15		
1	IO_L46P_1	E15		
1	IO_L45N_1/VREF_1	H15		
1	IO_L45P_1	G15		
1	IO_L44N_1	N17		
1	IO_L44P_1	M17		
1	IO_L43N_1	D14		
1	IO_L43P_1	C14		
1	IO_L39N_1	F14		
1	IO_L39P_1	E14		
1	IO_L38N_1	M16		
1	IO_L38P_1	M15		
1	IO_L37N_1	H14		
1	IO_L37P_1	G14		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L01N_0/VRP_0		G34		
0	IO_L01P_0/VRN_0		H34		
0	IO_L02N_0		F34		
0	IO_L02P_0		E34		
0	IO_L03N_0		C34		
0	IO_L03P_0/VREF_0		D34		
0	IO_L05_0/No_Pair		K32		
0	IO_L06N_0		H33		
0	IO_L06P_0		J33		
0	IO_L07N_0		F33		
0	IO_L07P_0		G33		
0	IO_L08N_0		E33		
0	IO_L08P_0		D33		
0	IO_L09N_0		H32		
0	IO_L09P_0/VREF_0		J32		
0	IO_L19N_0		E32		
0	IO_L19P_0		F32		
0	IO_L20N_0		C33		
0	IO_L20P_0		C32		
0	IO_L21N_0		K31		
0	IO_L21P_0		L31		
0	IO_L25N_0		H31		
0	IO_L25P_0		J31		
0	IO_L26N_0		G31		
0	IO_L26P_0		F31		
0	IO_L27N_0		D31		
0	IO_L27P_0/VREF_0		E31		
0	IO_L28N_0		L30		
0	IO_L28P_0		M30		
0	IO_L29N_0		J30		
0	IO_L29P_0		K30		
0	IO_L30N_0		G30		
0	IO_L30P_0		H30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L87P_4/VREF_4		AP15	NC	
4	IO_L37N_4		AV15		
4	IO_L37P_4		AU15		
4	IO_L38N_4		AY14		
4	IO_L38P_4		AY15		
4	IO_L39N_4		AM16		
4	IO_L39P_4		AL16		
4	IO_L43N_4		AP16		
4	IO_L43P_4		AN16		
4	IO_L44N_4		AR16		
4	IO_L44P_4		AT16		
4	IO_L45N_4		AV16		
4	IO_L45P_4/VREF_4		AU16		
4	IO_L46N_4		AL18		
4	IO_L46P_4		AL17		
4	IO_L47N_4		AM17		
4	IO_L47P_4		AN17		
4	IO_L48N_4		AR17		
4	IO_L48P_4		AP17		
4	IO_L49N_4		AU17		
4	IO_L49P_4		AT17		
4	IO_L50_4/No_Pair		AW16		
4	IO_L53_4/No_Pair		AW17		
4	IO_L54N_4		AN18		
4	IO_L54P_4		AM18		
4	IO_L55N_4		AT18		
4	IO_L55P_4		AR18		
4	IO_L56N_4		AV17		
4	IO_L56P_4		AV18		
4	IO_L57N_4		AY18		
4	IO_L57P_4/VREF_4		AY17		
4	IO_L58N_4		AM19		
4	IO_L58P_4		AL19		
4	IO_L59N_4		AP19		
4	IO_L59P_4		AN19		
4	IO_L60N_4		AT19		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L11N_0	M25	NC
0	IO_L11P_0	M26	NC
0	IO_L12N_0	F26	NC
0	IO_L12P_0	G26	NC
0	IO_L18N_0	B26	NC
0	IO_L18P_0/VREF_0	C26	NC
0	IO_L46N_0	G24	
0	IO_L46P_0	G25	
0	IO_L47N_0	K26	
0	IO_L47P_0	L26	
0	IO_L48N_0	E25	
0	IO_L48P_0	F25	
0	IO_L49N_0	C24	
0	IO_L49P_0	C25	
0	IO_L50_0/No_Pair	L24	
0	IO_L53_0/No_Pair	L25	
0	IO_L54N_0	A25	
0	IO_L54P_0	B25	
0	IO_L55N_0	H23	
0	IO_L55P_0	H24	
0	IO_L56N_0	J25	
0	IO_L56P_0	K25	
0	IO_L57N_0	E24	
0	IO_L57P_0/VREF_0	F24	
0	IO_L58N_0	D23	
0	IO_L58P_0	D24	
0	IO_L59N_0	J24	
0	IO_L59P_0	K24	
0	IO_L60N_0	A24	
0	IO_L60P_0	B24	
0	IO_L64N_0	F23	
0	IO_L64P_0	G23	
0	IO_L65N_0	M22	
0	IO_L65P_0	M23	
0	IO_L66N_0	B23	
0	IO_L66P_0/VREF_0	C23	
0	IO_L67N_0	H22	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L10N_5	AW27	NC
5	IO_L10P_5	AW26	NC
5	IO_L45N_5/VREF_5	AN27	
5	IO_L45P_5	AP27	
5	IO_L44N_5	AU27	
5	IO_L44P_5	AV27	
5	IO_L43N_5	AR27	
5	IO_L43P_5	AR26	
5	IO_L39N_5	AL27	
5	IO_L39P_5	AM27	
5	IO_L38N_5	BA28	
5	IO_L38P_5	BB28	
5	IO_L37N_5	AY28	
5	IO_L37P_5	AY27	
5	IO_L87N_5/VREF_5	AN28	
5	IO_L87P_5	AP28	
5	IO_L86N_5	AU28	
5	IO_L86P_5	AV28	
5	IO_L85N_5	AT28	
5	IO_L85P_5	AT27	
5	IO_L84N_5	AL28	
5	IO_L84P_5	AM28	
5	IO_L83_5/No_Pair	BA29	
5	IO_L80_5/No_Pair	BB29	
5	IO_L79N_5	AY29	
5	IO_L79P_5	AW28	
5	IO_L78N_5	AN29	
5	IO_L78P_5	AP29	
5	IO_L77N_5	AU29	
5	IO_L77P_5	AV29	
5	IO_L76N_5	AT29	
5	IO_L76P_5	AR28	
5	IO_L36N_5/VREF_5	AL29	
5	IO_L36P_5	AM29	
5	IO_L35N_5	AY30	
5	IO_L35P_5	BA30	
5	IO_L34N_5	AT30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	AG26	
N/A	VCCINT	AF26	
N/A	VCCINT	U26	
N/A	VCCINT	T26	
N/A	VCCINT	R26	
N/A	VCCINT	AG25	
N/A	VCCINT	T25	
N/A	VCCINT	AG24	
N/A	VCCINT	T24	
N/A	VCCINT	AG23	
N/A	VCCINT	T23	
N/A	VCCINT	AG22	
N/A	VCCINT	T22	
N/A	VCCINT	AG21	
N/A	VCCINT	T21	
N/A	VCCINT	AG20	
N/A	VCCINT	T20	
N/A	VCCINT	AG19	
N/A	VCCINT	T19	
N/A	VCCINT	AG18	
N/A	VCCINT	T18	
N/A	VCCINT	AH17	
N/A	VCCINT	AG17	
N/A	VCCINT	AF17	
N/A	VCCINT	U17	
N/A	VCCINT	T17	
N/A	VCCINT	R17	
N/A	VCCINT	AJ16	
N/A	VCCINT	AH16	
N/A	VCCINT	AG16	
N/A	VCCINT	AF16	
N/A	VCCINT	AE16	
N/A	VCCINT	AD16	
N/A	VCCINT	AC16	
N/A	VCCINT	AB16	
N/A	VCCINT	AA16	
N/A	VCCINT	Y16	