AMD Xilinx - XC2VP40-5FFG1148I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	804
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ffg1148i

Functional Description: RocketIO X Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO X multi-gigabit transceiver. For an in-depth discussion of the RocketIO X MGT, including digital and analog design considerations, refer to the **RocketIO X Transceiver User Guide.**

RocketIO X Overview

Either eight or twenty RocketIO X MGTs are available on the XC2VPX20 and XC2VPX70 devices, respectively. The XC2VPX20 MGT is designed to operate at any baud rate in the range of 2.488 Gb/s to 6.25 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 1. The XC2VPX70 MGT operates at a fixed 4.25 Gb/s per channel.

The RocketIO X MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 6.25 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The RocketIO X PCS has been significantly updated relative to the RocketIO PCS. In addition to the existing RocketIO PCS features, the RocketIO X PCS features 64B/66B encoder/decoder/scrambler/descrambler and SONET compatibility.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 4, page 3 shows a high-level block diagram of the RocketIO X transceiver and its FPGA interface signals.

Table 1: **Communications Standards Supported by RocketIO X Transceiver**(2)

Mode	Channels (Lanes)(1)	I/O Bit Rate (Gb/s)
SONET OC-48	1	2.488
PCI Express	1, 2, 4, 8, 16	2.5
Infiniband	1, 4, 12	2.5
XAUI (10-Gb Ethernet)	4	3.125
XAUI (10-Gb Fibre Channel)	4	3.1875
Aurora (Xilinx protocol)	1, 2, 3, 4,...	2.488 to 6.25
Custom Mode	1, 2, 3, 4,...	2.488 to 6.25

Notes:
1. One channel is considered to be one transceiver.
2. XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.

PMA

Transmitter Output

The RocketIO X transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 2. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω source resistors. The signal swing is created by switching the current in a common-source differential pair.

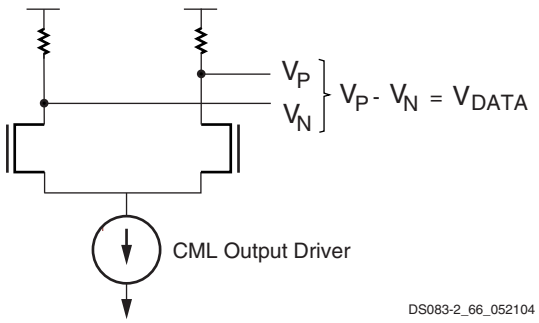

Figure 2: **CML Output Configuration**

Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by V_{TTX} at 1.5V. This configuration uses a CML approach with 50Ω termination to TXP and TXN as shown in Figure 3.

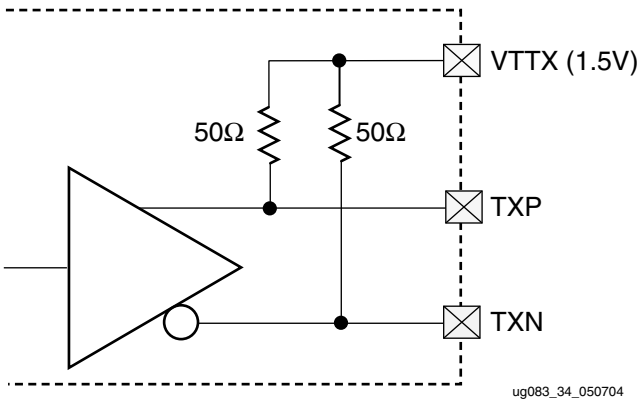

Figure 3: **RocketIO X Transmit Termination**

Output Swing and Emphasis

The output swing and emphasis levels are fully programmable. Each is controlled via attributes at configuration, and can be modified via the PMA attribute programming bus.

The programmable output swing control can adjust the differential peak-to-peak output level between 200 mV and 1600 mV.

With emphasis, the differential voltage swing is boosted to create a stronger rising or falling waveform. This method compensates for high frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Emphasis can be described from two perspectives, additive to the smaller voltage (V_{SM}) (pre-emphasis) or subtractive from the larger voltage (V_{LG}) (de-emphasis). The resulting benefits in compensating for channel loss are identical. It is simply a relative way of specifying the effect at the transmitter.

The equations for calculating pre-emphasis as a percentage and dB are as follows:

$$\text{Pre-Emphasis}_{\%} = ((V_{LG}-V_{SM}) / V_{SM}) \times 100$$
$$\text{Pre-Emphasis}_{dB} = 20 \log(V_{LG}/V_{SM})$$

The equations for calculating de-emphasis as a percentage and dB are as follows:

$$\text{De-Emphasis}_{\%} = (V_{LG} - V_{SM}) / V_{LG}) \times 100$$
$$\text{De-Emphasis}_{dB} = 20 \log(V_{SM}/V_{LG})$$

The pre-emphasis amount can be programmed in discrete steps between 0% and 500%. The de-emphasis amount can be programmed in discrete steps between 0% and 83%.

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 10, 16, 20, 32, or 40, depending on the operation mode. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

Synchronous serial data reception is facilitated by a clock and data recovery (CDR) circuit. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The CDR circuit extracts both phase and frequency from the incoming data stream.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{10}$, $^1/_{16}$, $^1/_{20}$, $^1/_{32}$, or $^1/_{40}$ the incoming data rate depending on the operating mode.

A sufficient number of transitions must be present in the data stream for CDR to work properly. The CDR circuit is guaranteed to work with 8B/10B and 64B/66B encoding. Further, CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Lock Control

The CDR circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100 ppm of the nominal frequency.

During normal operation, the receiver PLL automatically locks to incoming data (when present) or to the local reference clock (when data is not present). This is the default configuration for all primitives. This function can be overridden via the PMARXLOCKSEL port

When receive PLL lock is forced to the local reference, phase information from the incoming data stream is ignored. Data continues to be sampled, but synchronous to the local reference rather than relative to edges in the data stream.

Receive Equalization

In addition to transmit emphasis, the RocketIO X MGT provides a programmable active receive equalization feature to further compensate the effects of channel attenuation at high frequencies.

By adjusting RXFER, the right amount of equalization can be added to reverse the signal degradation caused by a printed circuit board, a backplane, or a line/switch card. RXFER can be set through software configuration or the PMA Attribute Bus.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver termination supply (V_{TRX}) is the center tap of differential termination to

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

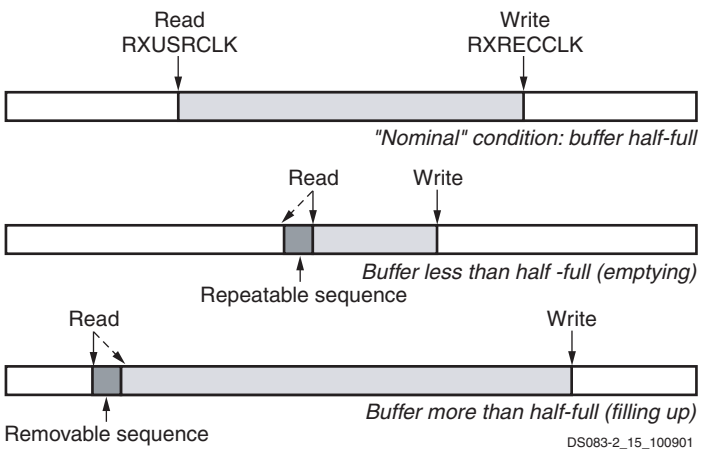

Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

Table 9: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LDT_25	2.5	N/R	N/R	0.500 – 0.740
LVDS_25	2.5	N/R	N/R	0.247 – 0.454
LVDSEXT_25	2.5	N/R	N/R	0.440 – 0.820
BLVDS_25	2.5	N/R	N/R	0.250 – 0.450
ULVDS_25	2.5	N/R	N/R	0.500 – 0.740
LVPECL_25	2.5	N/R	N/R	0.345 – 1.185
LDT_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740
LVDS_25_DT(1)	2.5	2.5	N/R	0.247 – 0.454
LVDSEXT_25_DT(1)	2.5	2.5	N/R	0.330 – 0.700
ULVDS_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740

Notes:
1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

Table 10: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R	Series
LVDCI_25	2.5	2.5	N/R	Series
LVDCI_DV2_25	2.5	2.5	N/R	Series
LVDCI_18	1.8	1.8	N/R	Series
LVDCI_DV2_18	1.8	1.8	N/R	Series
LVDCI_15	1.5	1.5	N/R	Series
LVDCI_DV2_15	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL18_I_DCI (3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split

Table 10: **Supported DCI I/O Standards *(Continued)***

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

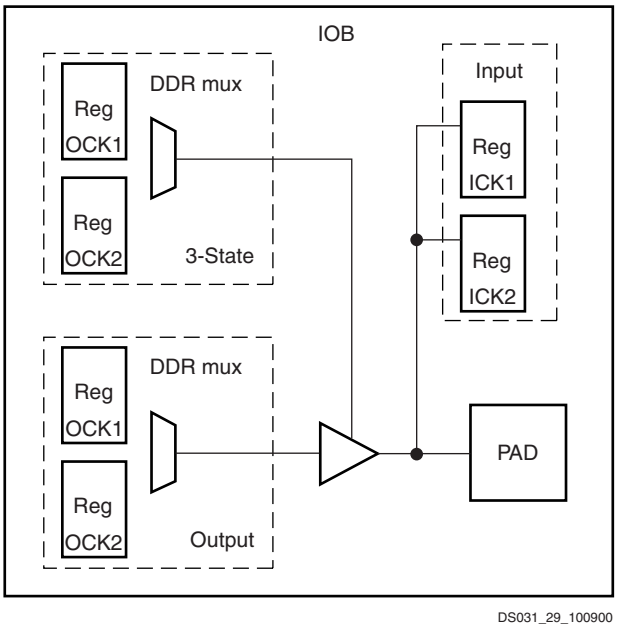

Figure 19: **Virtex-II Pro IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

Each block SelectRAM+ cell is a fully synchronous memory, as illustrated in Figure 48. The two ports have independent inputs and outputs and are independently clocked.

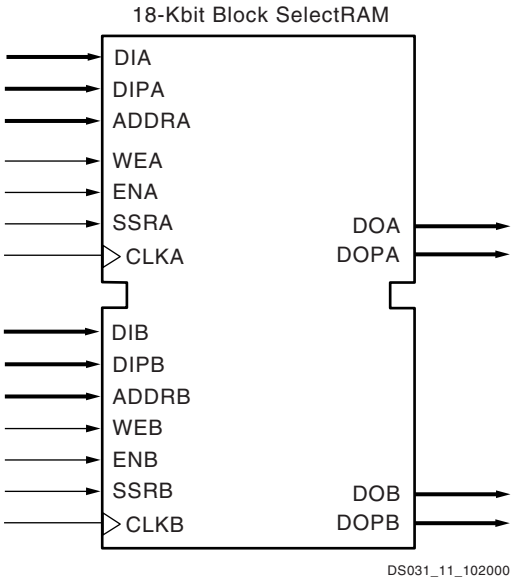

Figure 48: **18 Kb Block SelectRAM+ in Dual-Port Mode**

Port Aspect Ratios

Table 23 shows the depth and the width aspect ratios for the 18 Kb block SelectRAM+ resource. Virtex-II Pro block SelectRAM+ also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM+, and multipliers.

Table 23: **18 Kb Block SelectRAM+ Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II Pro block SelectRAM+ read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **WRITE_FIRST**

   The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO, as shown in Figure 49.

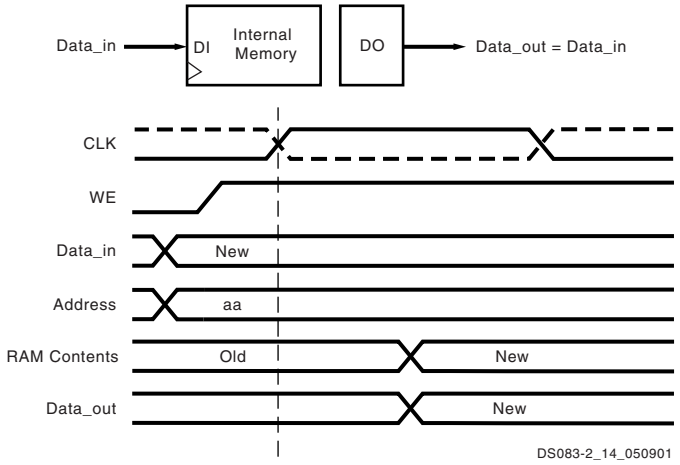

Figure 49: **WRITE_FIRST Mode**

2. **READ_FIRST**

The READ_FIRST option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 50.

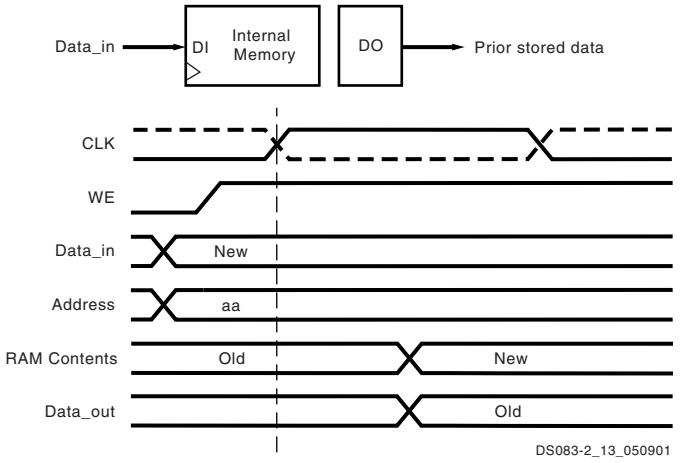

Figure 50: **READ_FIRST Mode**

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description[1]		Virtex-II Pro X	Virtex-II Pro	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to 1.6		V
V_{CCAUX}	Auxiliary supply voltage relative to GND		–0.5 to 3.0		V
V_{CCO}	Output drivers supply voltage relative to GND		–0.5 to 3.75		V
V_{BATT}	Key memory battery backup supply		–0.5 to 4.05		V
V_{REF}	Input reference voltage		–0.3 to 3.75		V
V_{IN}	3.3V I/O input voltage relative to GND (user and dedicated I/Os)		–0.3 to 4.05[3]		V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5		V
V_{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)		–0.3 to 4.05[3]		V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5		V
AVCCAUXRX	Receive auxilliary supply voltage relative to GNDA (analog ground)		–0.5 to 2.0	–0.5 to 3.0	V
AVCCAUXTX	Transmit auxilliary supply voltage relative to GNDA (analog ground)		–0.5 to 3.0	–0.5 to 3.0	V
V_{TRX}	Terminal receive supply voltage relative to GND		–0.5 to 3.0	–0.5 to 3.0	V
V_{TTX}	Terminal transmit supply voltage relative to GND		–0.5 to 1.6	–0.5 to 3.0	V
T_{STG}	Storage temperature (ambient)		–65 to +150		°C
T_{SOL}	Maximum soldering temperature[2]	All regular FG/FF flip-chip packages	+220		°C
		Pb-free FGG256 wire-bond package	N/A	+260	°C
		Pb-free FGG456 and FGG676 wire-bond packages	N/A	+250	°C
T_J	Maximum junction temperature[2]		+125		°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

RocketIO DC Input and Output Levels

Table 11: **RocketIO X Input/Output Voltage Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-Peak Differential Input Voltage(1)	DV_{IN}		250		2000	mV
Single-Ended Output Voltage Swing(2,3)	DV_{OUT}		0	400	900	mV
Peak-to-Peak Differential Output Voltage(2,3)	DV_{PPOUT}		0	800	1800	mV

Notes:
1. See Table 24, page 15, for minimum eye sensitivity.
2. Output swing levels are selectable using TXDOWNLEVEL attribute. Refer to the ***RocketIO X Transceiver User Guide*** for details.
3. Output preemphasis levels are selectable using the TXEMPHLEVEL attribute. Refer to the ***RocketIO X Transceiver User Guide*** for details.

Table 12: **RocketIO Input/Output Voltage Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-Peak Differential Input Voltage	DV_{IN}		175		2000	mV
Differential Input Impedance	$DIMP_{IN}$	TERMINATION_IMP = 50	90		125	Ω
		TERMINATION_IMP = 75	135		187.5	Ω
Single-Ended Output Voltage Swing(1,2)	DV_{OUT}		400		800	mV
Peak-to-Peak Differential Output Voltage(1,2)	DV_{PPOUT}		800	800	1600	mV

Notes:
1. Output swing levels are selectable using TX_DIFF_CTRL attribute. Refer to the ***RocketIO Transceiver User Guide*** for details.
2. Output preemphasis levels are selectable at 10% (default), 20%, 25%, and 33% using the TX_PREEMPHASIS attribute. Refer to the ***RocketIO Transceiver User Guide*** for details.

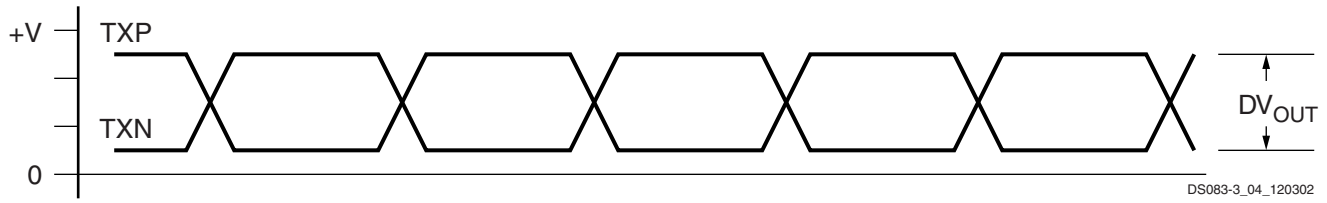

Figure 1: **Single-Ended Output Voltage Swing**

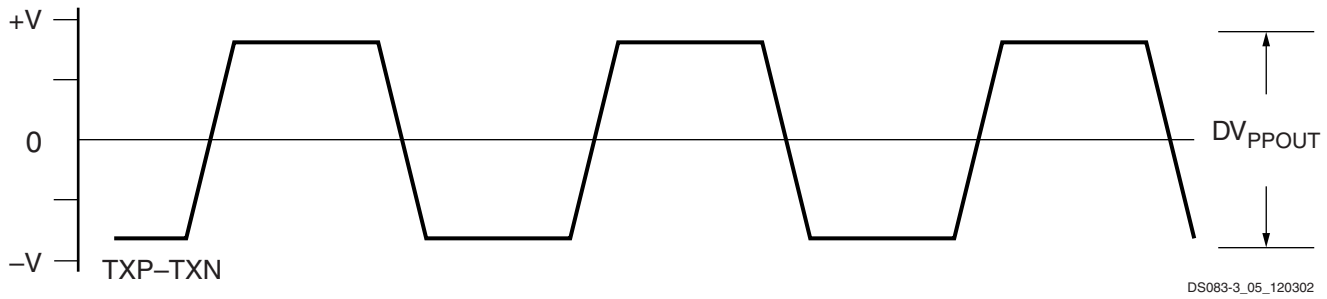

Figure 2: **Peak-to-Peak Differential Output Voltage**

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	AVCCAUXRX7	B13
N/A	AVCCAUXRX18	R13
N/A	VTRXPAD18	R12
N/A	RXNPAD18	T13
N/A	RXPPAD18	T12
N/A	GNDA18	P11
N/A	TXPPAD18	T11
N/A	TXNPAD18	T10
N/A	VTTXPAD18	R10
N/A	AVCCAUXTX18	R11
N/A	AVCCAUXRX19	R7
N/A	VTRXPAD19	R6
N/A	RXNPAD19	T7
N/A	RXPPAD19	T6
N/A	GNDA19	P6
N/A	TXPPAD19	T5
N/A	TXNPAD19	T4
N/A	VTTXPAD19	R4
N/A	AVCCAUXTX19	R5
N/A	VCCINT	N4
N/A	VCCINT	N13
N/A	VCCINT	M5
N/A	VCCINT	M12
N/A	VCCINT	E5
N/A	VCCINT	E12
N/A	VCCINT	D4
N/A	VCCINT	D13
N/A	VCCAUX	R16
N/A	VCCAUX	R1
N/A	VCCAUX	B16
N/A	VCCAUX	B1
N/A	GND	T16
N/A	GND	T1
N/A	GND	R2

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	K7			
7	VCCO_7	J7			
7	VCCO_7	H6			
7	VCCO_7	G6			
N/A	CCLK	W20			
N/A	PROG_B	B1			
N/A	DONE	Y18			
N/A	M0	Y4			
N/A	M1	W3			
N/A	M2	Y5			
N/A	TCK	B22			
N/A	TDI	D3			
N/A	TDO	D20			
N/A	TMS	A21			
N/A	PWRDWN_B	Y19			
N/A	HSWAP_EN	A2			
N/A	RSVD	C18			
N/A	VBATT	C19			
N/A	DXP	C4			
N/A	DXN	C5			
N/A	AVCCAUXTX4	B4	NC	NC	
N/A	VTTXPAD4	B3	NC	NC	
N/A	TXNPAD4	A3	NC	NC	
N/A	TXPPAD4	A4	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	RXPPAD4	A5	NC	NC	
N/A	RXNPAD4	A6	NC	NC	
N/A	VTRXPAD4	B5	NC	NC	
N/A	AVCCAUXRX4	B6	NC	NC	
N/A	AVCCAUXTX6	B8			
N/A	VTTXPAD6	B7			
N/A	TXNPAD6	A7			
N/A	TXPPAD6	A8			
N/A	GNDA6	C9			
N/A	RXPPAD6	A9			
N/A	RXNPAD6	A10			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VTRXPAD6	B9			
N/A	AVCCAUXRX6	B10			
N/A	AVCCAUXTX7	B14			
N/A	VTTXPAD7	B13			
N/A	TXNPAD7	A13			
N/A	TXPPAD7	A14			
N/A	GNDA7	C14			
N/A	RXPPAD7	A15			
N/A	RXNPAD7	A16			
N/A	VTRXPAD7	B15			
N/A	AVCCAUXRX7	B16			
N/A	AVCCAUXTX9	B18	NC	NC	
N/A	VTTXPAD9	B17	NC	NC	
N/A	TXNPAD9	A17	NC	NC	
N/A	TXPPAD9	A18	NC	NC	
N/A	GNDA9	C17	NC	NC	
N/A	RXPPAD9	A19	NC	NC	
N/A	RXNPAD9	A20	NC	NC	
N/A	VTRXPAD9	B19	NC	NC	
N/A	AVCCAUXRX9	B20	NC	NC	
N/A	AVCCAUXRX16	AA20	NC	NC	
N/A	VTRXPAD16	AA19	NC	NC	
N/A	RXNPAD16	AB20	NC	NC	
N/A	RXPPAD16	AB19	NC	NC	
N/A	GNDA16	Y17	NC	NC	
N/A	TXPPAD16	AB18	NC	NC	
N/A	TXNPAD16	AB17	NC	NC	
N/A	VTTXPAD16	AA17	NC	NC	
N/A	AVCCAUXTX16	AA18	NC	NC	
N/A	AVCCAUXRX18	AA16			
N/A	VTRXPAD18	AA15			
N/A	RXNPAD18	AB16			
N/A	RXPPAD18	AB15			
N/A	GNDA18	Y14			
N/A	TXPPAD18	AB14			
N/A	TXNPAD18	AB13			
N/A	VTTXPAD18	AA13			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	H4			
N/A	GND	H23			
N/A	GND	K6			
N/A	GND	K21			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M3			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M24			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	R3			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L01N_0/VRP_0		E25			
0	IO_L01P_0/VRN_0		E24			
0	IO_L02N_0		F24			
0	IO_L02P_0		F23			
0	IO_L03N_0		E23			
0	IO_L03P_0/VREF_0		E22			
0	IO_L05_0/No_Pair		G23			
0	IO_L06N_0		H22			
0	IO_L06P_0		G22			
0	IO_L07N_0		F22			
0	IO_L07P_0		F21			
0	IO_L08N_0		D24			
0	IO_L08P_0		C24			
0	IO_L09N_0		H21			
0	IO_L09P_0/VREF_0		G21			
0	IO_L37N_0		E21			
0	IO_L37P_0		D21			
0	IO_L38N_0		D23			
0	IO_L38P_0		C23			
0	IO_L39N_0		H20			
0	IO_L39P_0		G20			
0	IO_L43N_0		E20			
0	IO_L43P_0		D20			
0	IO_L44N_0		B23			
0	IO_L44P_0		A23			
0	IO_L45N_0		H19			
0	IO_L45P_0/VREF_0		G19			
0	IO_L46N_0		E19	NC		
0	IO_L46P_0		E18	NC		
0	IO_L47N_0		C22	NC		
0	IO_L47P_0		B22	NC		
0	IO_L48N_0		F20	NC		
0	IO_L48P_0		F19	NC		
0	IO_L49N_0		G17	NC		
0	IO_L49P_0		F17	NC		
0	IO_L50_0/No_Pair		B21	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L34N_0		E30		
0	IO_L34P_0		F30		
0	IO_L35N_0		D30		
0	IO_L35P_0		C30		
0	IO_L36N_0		M28		
0	IO_L36P_0/VREF_0		M29		
0	IO_L78N_0		K29	NC	
0	IO_L78P_0		L29	NC	
0	IO_L83_0/No_Pair		H29	NC	
0	IO_L84N_0		F29	NC	
0	IO_L84P_0		G29	NC	
0	IO_L85N_0		D29	NC	
0	IO_L85P_0		E29	NC	
0	IO_L86N_0		L28	NC	
0	IO_L86P_0		K28	NC	
0	IO_L87N_0		H28	NC	
0	IO_L87P_0/VREF_0		J28	NC	
0	IO_L37N_0		E28		
0	IO_L37P_0		F28		
0	IO_L38N_0		C29		
0	IO_L38P_0		C28		
0	IO_L39N_0		L27		
0	IO_L39P_0		M27		
0	IO_L43N_0		J27		
0	IO_L43P_0		K27		
0	IO_L44N_0		H27		
0	IO_L44P_0		G27		
0	IO_L45N_0		E27		
0	IO_L45P_0/VREF_0		F27		
0	IO_L46N_0		M25		
0	IO_L46P_0		M26		
0	IO_L47N_0		L26		
0	IO_L47P_0		K26		
0	IO_L48N_0		H26		
0	IO_L48P_0		J26		
0	IO_L49N_0		F26		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L37N_5		AU28		
5	IO_L37P_5		AV28		
5	IO_L87N_5/VREF_5		AP28	NC	
5	IO_L87P_5		AR28	NC	
5	IO_L86N_5		AN28	NC	
5	IO_L86P_5		AM28	NC	
5	IO_L85N_5		AV29	NC	
5	IO_L85P_5		AW29	NC	
5	IO_L84N_5		AT29	NC	
5	IO_L84P_5		AU29	NC	
5	IO_L83_5/No_Pair		AR29	NC	
5	IO_L78N_5		AM29	NC	
5	IO_L78P_5		AN29	NC	
5	IO_L36N_5/VREF_5		AL29		
5	IO_L36P_5		AL28		
5	IO_L35N_5		AY30		
5	IO_L35P_5		AW30		
5	IO_L34N_5		AU30		
5	IO_L34P_5		AV30		
5	IO_L30N_5		AR30		
5	IO_L30P_5		AT30		
5	IO_L29N_5		AN30		
5	IO_L29P_5		AP30		
5	IO_L28N_5		AL30		
5	IO_L28P_5		AM30		
5	IO_L27N_5/VREF_5		AV31		
5	IO_L27P_5		AW31		
5	IO_L26N_5		AU31		
5	IO_L26P_5		AT31		
5	IO_L25N_5		AP31		
5	IO_L25P_5		AR31		
5	IO_L21N_5		AM31		
5	IO_L21P_5		AN31		
5	IO_L20N_5		AY32		
5	IO_L20P_5		AY33		
5	IO_L19N_5		AU32		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AU25		
N/A	GND		AU18		
N/A	GND		AU6		
N/A	GND		AV38		
N/A	GND		AV22		
N/A	GND		AV21		
N/A	GND		AV5		
N/A	GND		AW39		
N/A	GND		AW32		
N/A	GND		AW28		
N/A	GND		AW15		
N/A	GND		AW11		
N/A	GND		AW4		
N/A	GND		AY42		
N/A	GND		AY41		
N/A	GND		AY40		
N/A	GND		AY3		
N/A	GND		AY2		
N/A	GND		AY1		
N/A	GND		BA42		
N/A	GND		BA1		
N/A	GND		AA38		
N/A	GND		AA35		
N/A	GND		AA32		
N/A	GND		AA26		
N/A	GND		AA25		
N/A	GND		AA24		
N/A	GND		AA23		
N/A	GND		AA22		
N/A	GND		AA21		
N/A	GND		AA20		
N/A	GND		AA19		
N/A	GND		AA18		
N/A	GND		AA17		
N/A	GND		AA11		
N/A	GND		AA8		

Date	Version	Revision
11/17/04	4.1	• Table 4: Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
03/01/05	4.2	• Table 3: Corrected number of Differential I/O Pairs for XC2VP30-FF1152 from 340 to 316. • Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”.
06/20/05	4.3	*No changes in Module 4 for this revision.*
09/15/05	4.4	*No changes in Module 4 for this revision.*
10/10/05	4.5	*No changes in Module 4 for this revision.*
03/05/07	4.6	• Figure 2, page 29: Corrected NOTE 3. • Figure 7, page 161: Updated with drawing showing correct heat sink profile and detail.
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Updated Figure 3, page 50, with the newest FG676/FGG676 mechanical drawing.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)