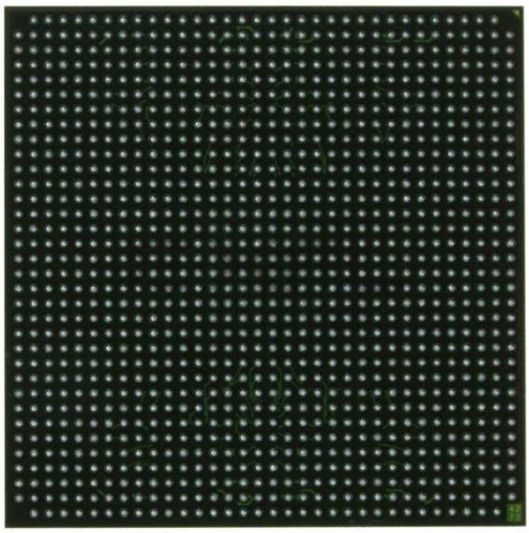

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ffg1152c

Virtex-II Pro / Virtex-II Pro X Device/Package Combinations and Maximum I/Os

Offerings include ball grid array (BGA) packages with 1.0 mm pitch. In addition to traditional wire-bond interconnect (FG/FGG packages), flip-chip interconnect (FF packages) is used in some of the BGA offerings. Flip-chip interconnect construction supports more I/Os than are possible in wire-bond versions of similar packages, providing a high pin count and excellent power dissipation.

The device/package combination table (Table 3) details the maximum number of user I/Os and RocketIO / RocketIO X MGTs for each device and package using wire-bond or flip-chip technology.

The FF1148 and FF1696 packages have no RocketIO transceivers bonded out. Extra SelectIO-Ultra resources occupy available pins in these packages, resulting in a higher user I/O count. These packages are available for the XC2VP40, XC2VP50, and XC2VP100 devices only.

The I/Os per package count includes all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), VBATT, and the RocketIO / RocketIO X transceiver pins.

Table 3: **Virtex-II Pro Device/Package Combinations and Maximum Number of Available I/Os**

Package(1)	FG256/ FGG256	FG456/ FGG456	FG676	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**
Size (mm)	**17 x 17**	**23 x 23**	**26 x 26**	**27 x 27**	**31 x 31**	**35 x 35**	**35 x 35**	**40 x 40**	**42.5 x 42.5**	**42.5 x 42.5**
XC2VP2	140 / 4	156 / 4		204 / 4						
XC2VP4	140 / 4	248 / 4		348 / 4						
XC2VP7		248 / 8		396 / 8	396 / 8					
XC2VP20			404 / 8		556 / 8	564 / 8				
XC2VPX20					552 / 8(2)					
XC2VP30			416 / 8		556 / 8	644 / 8				
XC2VP40			416 / 8			692 / 12	804 / 0(3)			
XC2VP50						692 / 16	812 / 0(3)	852 / 16		
XC2VP70								964 / 16	996 / 20	
XC2VPX70									992 / 20(2)	
XC2VP100									1,040 / 20	1,164 / 0(3)

Notes:
1. Wirebond packages FG256, FG456, and FG676 are also available in Pb-free versions FGG256, FGG456, and FGG676. See Virtex-II Pro Ordering Examples for details on how to order.
2. Virtex-II Pro X device is equipped with RocketIO X transceiver cores.
3. The RocketIO transceivers in devices in the FF1148 and FF1696 packages are not bonded out to the package pins.

Maximum Performance

Maximum performance of the RocketIO / RocketIO X transceiver and the PowerPC processor block varies, depending on package style and speed grade. See Table 4 for details. Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics contains the rest of the FPGA fabric performance parameters.

Table 4: **Maximum RocketIO / RocketIO X Transceiver and Processor Block Performance**

Device	Speed Grade			Units
	-7(1)	-6	-5	
RocketIO X Transceiver FlipChip (FF)	N/A	6.25(3)	4.25(3)	Gb/s
RocketIO Transceiver FlipChip (FF)	3.125	3.125	2.0	Gb/s
RocketIO Transceiver Wirebond (FG)	2.5	2.5	2.0	Gb/s
PowerPC Processor Block	400(2)	350(2)	300	MHz

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1 to identify dual-processor devices.
3. XC2VPX70 is only available at fixed 4.25 Gb/s baud rate.

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

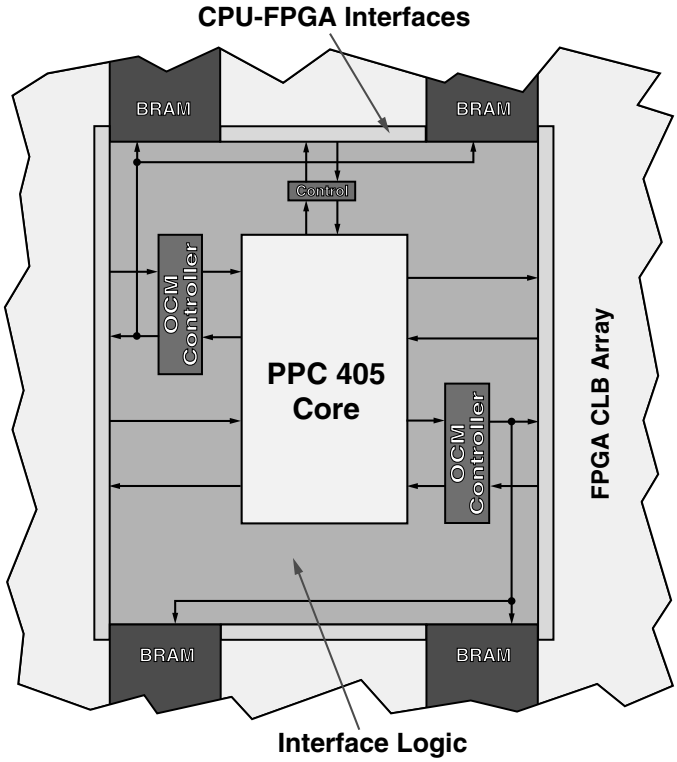

Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

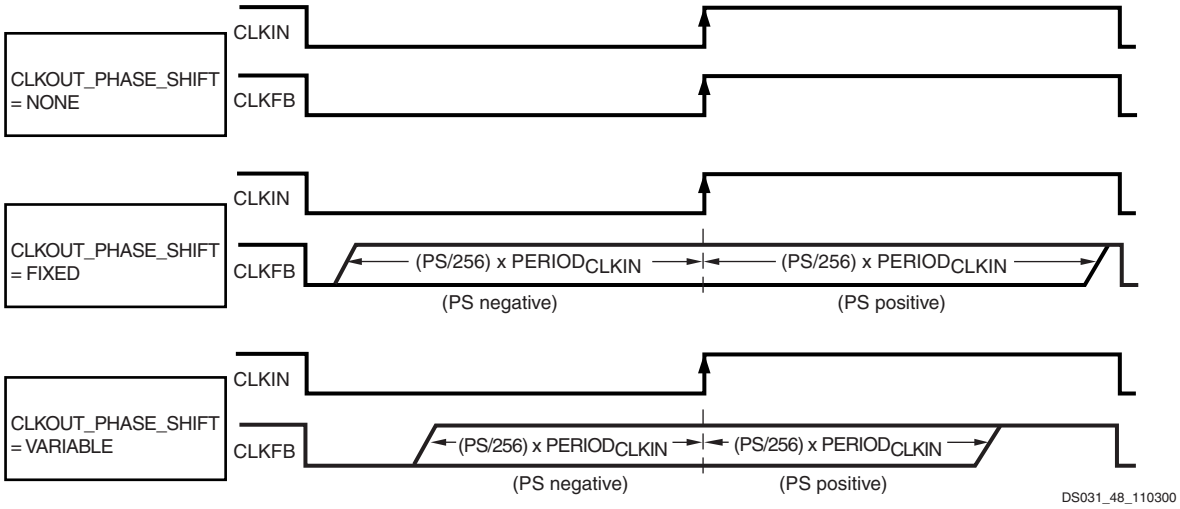

Figure 63: **Fine-Phase Shifting Effects**

Two separate components of the phase shift range must be understood:

- PHASE_SHIFT attribute range
- FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

$$\text{Phase Shift (ns)} = (\text{PHASE\_SHIFT}/256) * \text{PERIOD}_{\text{CLKIN}}$$

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit. Across process, voltage, and temperature, this absolute range is guaranteed to be as specified under **DCM Timing Parameters** in Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Absolute range (fixed mode) = ± FINE_SHIFT_RANGE

Absolute range (variable mode) = ± FINE_SHIFT_RANGE/2

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric, dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line, thus dividing the total delay line range in half. In fixed mode, since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertion into either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If $\text{PERIOD}_{\text{CLKIN}} = 2 * \text{FINE\_SHIFT\_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 128, and in variable mode it is limited to ± 64.
- If $\text{PERIOD}_{\text{CLKIN}} = \text{FINE\_SHIFT\_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 255, and in variable mode it is limited to ± 128.
- If $\text{PERIOD}_{\text{CLKIN}} \leq 0.5 * \text{FINE\_SHIFT\_RANGE}$, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to Table 30. For actual values, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics. The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high-frequency mode.

High or low-frequency mode is selected by an attribute.

Table 30: **DCM Frequency Ranges**

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Table 19: **Processor Block JTAG Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	$T_{PCCK_}$JTAG/ $T_{PCKC_}$JTAG	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
JTAG reset input	$T_{PCCK_}$JTAGRST/ $T_{PCKC_}$JTAGRST	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
Clock to Out					
JTAG control outputs	$T_{PCKCO_}$JTAG	1.34	1.54	1.69	ns, max

Table 20: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMDSOCMCLK)					
Data-Side On-Chip Memory data bus inputs	$T_{PDCK_}$DSOCM/ $T_{PCKD_}$DSOCM	0.73/ 0.83	0.84/ 0.95	0.92/ 1.05	ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	$T_{PCKCO_}$DSOCM	1.58	1.82	1.99	ns, max
Data-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$DSOCM	1.46	1.68	1.84	ns, max
Data-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$DSOCM	0.90	1.03	1.13	ns, max

Table 21: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMISOCMCLK)					
Instruction-Side On-Chip Memory data bus inputs	$T_{PDCK_}$ISOCM/ $T_{PCKD_}$ISOCM	0.81/ 0.68	0.93/ 0.78	1.02/ 0.86	ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	$T_{PCKCO_}$ISOCM	1.33	1.53	1.68	ns, max
Instruction-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$ISOCM	1.52	1.75	1.92	ns, max
Instruction-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$ISOCM	1.35	1.55	1.70	ns, max

Table 35: **IOB Input Switching Characteristics *(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.61	0.86/–0.63	0.90/–0.67	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2	2.28/–1.89	2.60/–2.15	2.95/–2.43	ns, max
		XC2VP4	2.55/–2.10	2.87/–2.36	3.21/–2.65	ns, max
		XC2VP7	2.48/–2.05	2.82/–2.32	3.15/–2.60	ns, max
		XC2VP20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VPX20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VP30	2.67/–2.07	3.09/–2.42	3.49/–2.73	ns, max
		XC2VP40	3.28/–2.56	3.61/–2.83	4.01/–3.15	ns, max
		XC2VP50	3.84/–3.02	4.08/–3.21	4.42/–3.48	ns, max
		XC2VP70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VPX70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VP100	N/A	6.48/–5.13	7.04/–5.57	ns, max
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 39.

Table 36: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.59	0.68	0.75	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.59	0.68	0.75	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.59	0.68	0.75	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.49	0.57	0.62	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.27	0.31	0.35	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.27	0.31	0.35	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.17	0.20	0.22	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.17	0.20	0.22	ns
LVDS, 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.33	0.37	0.41	ns
LVDS, 2.5V, with Differential Termination (DT)	LVDS_25_DT	$T_{ILVDS\_25\_DT}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DT	LVDSEXT_25_DT	$T_{ILVDSEXT\_25\_DT}$	0.33	0.37	0.41	ns
ULVDS, 2.5V, with DT	ULVDS_25_DT	$T_{IULVDS\_25\_DT}$	0.31	0.36	0.40	ns
LDT, 2.5V, with DT	LDT_25_DT	$T_{ILDT\_25\_DT}$	0.31	0.36	0.40	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 39 shows the test setup parameters used for measuring Input standard adjustments (see Table 36, page 25).

Table 39: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.3	1.65	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Tnscvr Logic), Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1.15 – 0.3	1.15 + 0.3	1.15	

Notes:

1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See ***Virtex-II Pro Platform FPGA User Guide*** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.

Multiplier Switching Characteristics

Table 45: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T_{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T_{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T_{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T_{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T_{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T_{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T_{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T_{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T_{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T_{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T_{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T_{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T_{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T_{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T_{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T_{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T_{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T_{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T_{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T_{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T_{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T_{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T_{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T_{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T_{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T_{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T_{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T_{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T_{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T_{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T_{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T_{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T_{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T_{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T_{MULT_P0}	1.13	1.27	1.43	ns, max

Master/Slave SelectMAP Parameters

Figure 10 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

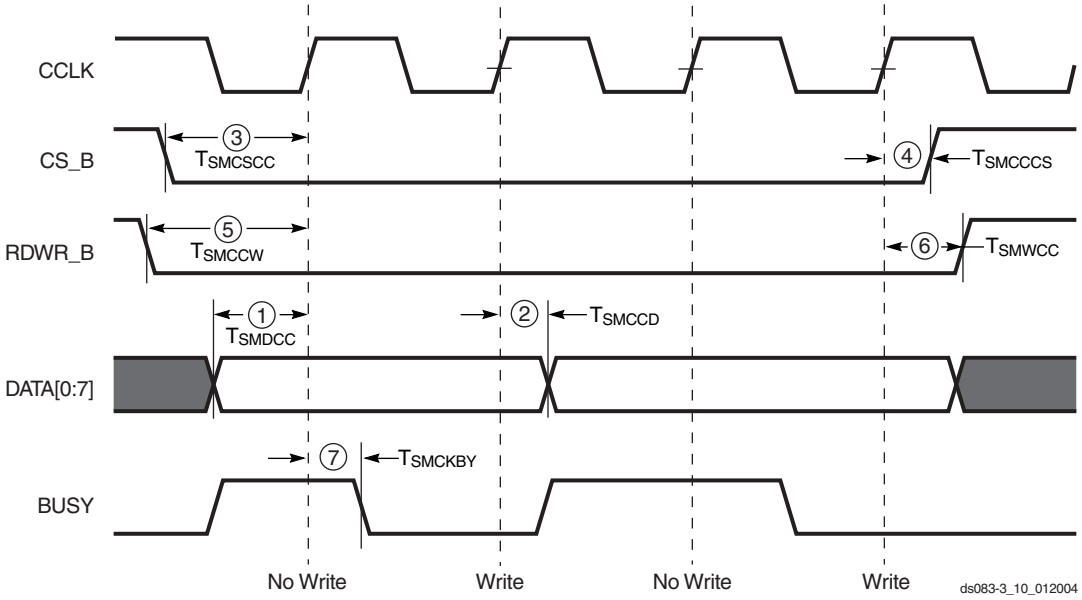

Figure 10: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 51: **SelectMAP Mode Write Timing Characteristics**

	Description	Device	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	XC2VP2	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
		XC2VP4			5.0/0.0	ns, min
		XC2VP7			5.0/0.0	ns, min
		XC2VP20			5.0/0.0	ns, min
		XC2VPX20			5.0/0.0	ns, min
		XC2VP30			5.0/0.0	ns, min
		XC2VP40			5.0/0.0	ns, min
		XC2VP50			5.0/0.0	ns, min
		XC2VP70			6.0/0.0	ns, min
		XC2VPX70			6.0/0.0	ns, min
		XC2VP100			7.5/0.0	ns, min
	CS_B setup/hold		3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold		5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay		7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency			$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency			$F_{CC\_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake			F_{CCNH}	50	MHz, max

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
5	IO_L74P_5/GCLK4P	AB14			
5	IO_L73N_5	AA14			
5	IO_L73P_5	Y14			
5	IO_L69N_5/VREF_5	W14			
5	IO_L69P_5	W15			
5	IO_L68N_5	AD15			
5	IO_L68P_5	AC15			
5	IO_L67N_5	AB15			
5	IO_L67P_5	AA15			
5	IO_L45N_5/VREF_5	AC16	NC	NC	
5	IO_L45P_5	AB16	NC	NC	
5	IO_L44N_5	Y15	NC	NC	
5	IO_L44P_5	Y16	NC	NC	
5	IO_L43N_5	AC17	NC	NC	
5	IO_L43P_5	AB17	NC	NC	
5	IO_L39N_5	AA16	NC	NC	
5	IO_L39P_5	AA17	NC	NC	
5	IO_L38N_5	W16	NC	NC	
5	IO_L38P_5	Y17	NC	NC	
5	IO_L37N_5	AD18	NC	NC	
5	IO_L37P_5	AC18	NC	NC	
5	IO_L09N_5/VREF_5	AA18			
5	IO_L09P_5	Y18			
5	IO_L08N_5	AF19			
5	IO_L08P_5	AE19			
5	IO_L07N_5/VREF_5	AD19			
5	IO_L07P_5	AC19			
5	IO_L06N_5/VRP_5	AB18			
5	IO_L06P_5/VRN_5	AB19			
5	IO_L05_5/No_Pair	Y19			
5	IO_L03N_5/D4	AA19			
5	IO_L03P_5/D5	AA20			
5	IO_L02N_5/D6	AC20			
5	IO_L02P_5/D7	AB20			
5	IO_L01N_5/RDWR_B	AD21			
5	IO_L01P_5/CS_B	AC21			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L58P_3	W6				
3	IO_L57N_3/VREF_3	Y3				
3	IO_L57P_3	Y4				
3	IO_L56N_3	W7				
3	IO_L56P_3	W8				
3	IO_L55N_3	Y6				
3	IO_L55P_3	Y7				
3	IO_L54N_3	AA2				
3	IO_L54P_3	AB2				
3	IO_L53N_3	W9				
3	IO_L53P_3	W10				
3	IO_L52N_3	AA3				
3	IO_L52P_3	AA4				
3	IO_L51N_3/VREF_3	AB1				
3	IO_L51P_3	AC1				
3	IO_L50N_3	Y9				
3	IO_L50P_3	Y10				
3	IO_L49N_3	AA5				
3	IO_L49P_3	AA6				
3	IO_L48N_3	AB3				
3	IO_L48P_3	AB4				
3	IO_L47N_3	AA7				
3	IO_L47P_3	AA8				
3	IO_L46N_3	AB5				
3	IO_L46P_3	AB6				
3	IO_L45N_3/VREF_3	AC2				
3	IO_L45P_3	AD2				
3	IO_L44N_3	AA9				
3	IO_L44P_3	AA10				
3	IO_L43N_3	AC3				
3	IO_L43P_3	AC4				
3	IO_L42N_3	AD1				
3	IO_L42P_3	AE1				
3	IO_L41N_3	AB7				
3	IO_L41P_3	AB8				
3	IO_L40N_3	AC6				
3	IO_L40P_3	AC7				
3	IO_L39N_3/VREF_3	AD3				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L17N_3	AH9		
3	IO_L17P_3	AJ9		
3	IO_L16N_3	AK7		
3	IO_L16P_3	AL7		
3	IO_L15N_3/VREF_3	AK4		
3	IO_L15P_3	AL4		
3	IO_L14N_3	AJ7		
3	IO_L14P_3	AJ8		
3	IO_L13N_3	AK3		
3	IO_L13P_3	AL3		
3	IO_L12N_3	AL5		
3	IO_L12P_3	AL6		
3	IO_L11N_3	AK8		
3	IO_L11P_3	AL8		
3	IO_L10N_3	AL1		
3	IO_L10P_3	AL2		
3	IO_L09N_3/VREF_3	AM6		
3	IO_L09P_3	AM7		
3	IO_L08N_3	AL9		
3	IO_L08P_3	AM9		
3	IO_L07N_3	AM5		
3	IO_L07P_3	AN5		
3	IO_L06N_3	AM1		
3	IO_L06P_3	AM2		
3	IO_L05N_3	AN8		
3	IO_L05P_3	AN9		
3	IO_L04N_3	AN6		
3	IO_L04P_3	AP6		
3	IO_L03N_3/VREF_3	AN4		
3	IO_L03P_3	AP4		
3	IO_L02N_3	AN7		
3	IO_L02P_3	AP7		
3	IO_L01N_3/VRP_3	AN3		
3	IO_L01P_3/VRN_3	AP3		
4	IO_L01N_4/BUSY/DOUT(1)	AK10		
4	IO_L01P_4/INIT_B	AJ10		
4	IO_L02N_4/D0/DIN(1)	AF11		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L06N_6	AM34		
6	IO_L07P_6	AN30		
6	IO_L07N_6	AM30		
6	IO_L08P_6	AM26		
6	IO_L08N_6	AL26		
6	IO_L09P_6	AM28		
6	IO_L09N_6/VREF_6	AM29		
6	IO_L10P_6	AL33		
6	IO_L10N_6	AL34		
6	IO_L11P_6	AL27		
6	IO_L11N_6	AK27		
6	IO_L12P_6	AL29		
6	IO_L12N_6	AL30		
6	IO_L13P_6	AL32		
6	IO_L13N_6	AK32		
6	IO_L14P_6	AJ27		
6	IO_L14N_6	AJ28		
6	IO_L15P_6	AL31		
6	IO_L15N_6/VREF_6	AK31		
6	IO_L16P_6	AL28		
6	IO_L16N_6	AK28		
6	IO_L17P_6	AJ26		
6	IO_L17N_6	AH26		
6	IO_L18P_6	AJ33		
6	IO_L18N_6	AJ34		
6	IO_L19P_6	AJ31		
6	IO_L19N_6	AJ32		
6	IO_L20P_6	AG27		
6	IO_L20N_6	AG28		
6	IO_L21P_6	AK29		
6	IO_L21N_6/VREF_6	AJ29		
6	IO_L22P_6	AH33		
6	IO_L22N_6	AH34		
6	IO_L23P_6	AF27		
6	IO_L23N_6	AE27		
6	IO_L24P_6	AJ30		
6	IO_L24N_6	AH30		
6	IO_L25P_6	AH28		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L09P_7		K36		
7	IO_L09N_7		K35		
7	IO_L08P_7		K38		
7	IO_L08N_7		K37		
7	IO_L07P_7		L33		
7	IO_L07N_7		K34		
7	IO_L84P_7		J41		
7	IO_L84N_7		J42		
7	IO_L83P_7		J39		
7	IO_L83N_7		J38		
7	IO_L82P_7		J36		
7	IO_L82N_7/VREF_7		J37		
7	IO_L81P_7		J35		
7	IO_L81N_7		H36		
7	IO_L80P_7		H41		
7	IO_L80N_7		H40		
7	IO_L79P_7		H38		
7	IO_L79N_7		H39		
7	IO_L78P_7		H37		
7	IO_L78N_7		G38		
7	IO_L77P_7		G42		
7	IO_L77N_7		G41		
7	IO_L76P_7		G39		
7	IO_L76N_7/VREF_7		G40		
7	IO_L75P_7		F41		
7	IO_L75N_7		F42		
7	IO_L74P_7		F40		
7	IO_L74N_7		F39		
7	IO_L73P_7		E41		
7	IO_L73N_7		E42		
7	IO_L06P_7		D41		
7	IO_L06N_7		D42		
7	IO_L05P_7		E40		
7	IO_L05N_7		D40		
7	IO_L04P_7		F36		
7	IO_L04N_7/VREF_7		G37		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AU25		
N/A	GND		AU18		
N/A	GND		AU6		
N/A	GND		AV38		
N/A	GND		AV22		
N/A	GND		AV21		
N/A	GND		AV5		
N/A	GND		AW39		
N/A	GND		AW32		
N/A	GND		AW28		
N/A	GND		AW15		
N/A	GND		AW11		
N/A	GND		AW4		
N/A	GND		AY42		
N/A	GND		AY41		
N/A	GND		AY40		
N/A	GND		AY3		
N/A	GND		AY2		
N/A	GND		AY1		
N/A	GND		BA42		
N/A	GND		BA1		
N/A	GND		AA38		
N/A	GND		AA35		
N/A	GND		AA32		
N/A	GND		AA26		
N/A	GND		AA25		
N/A	GND		AA24		
N/A	GND		AA23		
N/A	GND		AA22		
N/A	GND		AA21		
N/A	GND		AA20		
N/A	GND		AA19		
N/A	GND		AA18		
N/A	GND		AA17		
N/A	GND		AA11		
N/A	GND		AA8		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L38P_3	AE9	
3	IO_L37N_3	AH3	
3	IO_L37P_3	AJ3	
3	IO_L36N_3	AJ1	
3	IO_L36P_3	AJ2	
3	IO_L35N_3	AE6	
3	IO_L35P_3	AE7	
3	IO_L34N_3	AK6	
3	IO_L34P_3	AK7	
3	IO_L33N_3/VREF_3	AK3	
3	IO_L33P_3	AK4	
3	IO_L32N_3	AE12	
3	IO_L32P_3	AF12	
3	IO_L31N_3	AL5	
3	IO_L31P_3	AL6	
3	IO_L30N_3	AL3	
3	IO_L30P_3	AL4	
3	IO_L29N_3	AF10	
3	IO_L29P_3	AF11	
3	IO_L28N_3	AK2	
3	IO_L28P_3	AL2	
3	IO_L27N_3/VREF_3	AL7	
3	IO_L27P_3	AM6	
3	IO_L26N_3	AF7	
3	IO_L26P_3	AF8	
3	IO_L25N_3	AM4	
3	IO_L25P_3	AM5	
3	IO_L24N_3	AM1	
3	IO_L24P_3	AM2	
3	IO_L23N_3	AG10	
3	IO_L23P_3	AG11	
3	IO_L22N_3	AM7	
3	IO_L22P_3	AN7	
3	IO_L21N_3/VREF_3	AN5	
3	IO_L21P_3	AN6	
3	IO_L20N_3	AG8	
3	IO_L20P_3	AG9	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L52P_6	AF40	
6	IO_L52N_6	AF41	
6	IO_L53P_6	AC36	
6	IO_L53N_6	AC37	
6	IO_L54P_6	AE41	
6	IO_L54N_6	AE42	
6	IO_L55P_6	AE40	
6	IO_L55N_6	AD40	
6	IO_L56P_6	AC31	
6	IO_L56N_6	AC32	
6	IO_L57P_6	AE38	
6	IO_L57N_6/VREF_6	AE39	
6	IO_L58P_6	AD41	
6	IO_L58N_6	AD42	
6	IO_L59P_6	AB35	
6	IO_L59N_6	AB36	
6	IO_L60P_6	AD37	
6	IO_L60N_6	AD38	
6	IO_L85P_6	AC40	
6	IO_L85N_6	AC41	
6	IO_L86P_6	AB33	
6	IO_L86N_6	AB34	
6	IO_L87P_6	AC39	
6	IO_L87N_6/VREF_6	AB39	
6	IO_L88P_6	AB40	
6	IO_L88N_6	AB41	
6	IO_L89P_6	AB31	
6	IO_L89N_6	AB32	
6	IO_L90P_6	AB37	
6	IO_L90N_6	AB38	
7	IO_L90P_7	AA40	
7	IO_L90N_7	AA41	
7	IO_L89P_7	AA35	
7	IO_L89N_7	AA36	
7	IO_L88P_7	Y39	
7	IO_L88N_7/VREF_7	AA39	