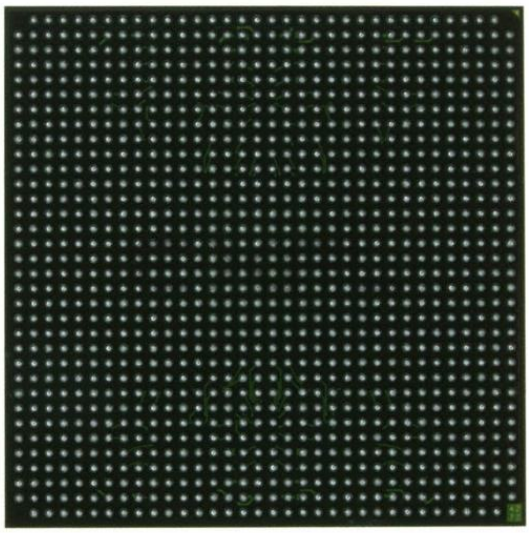

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5ffg1152i

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011 **Product Specification**

Virtex-II Pro[1] Array Functional Description

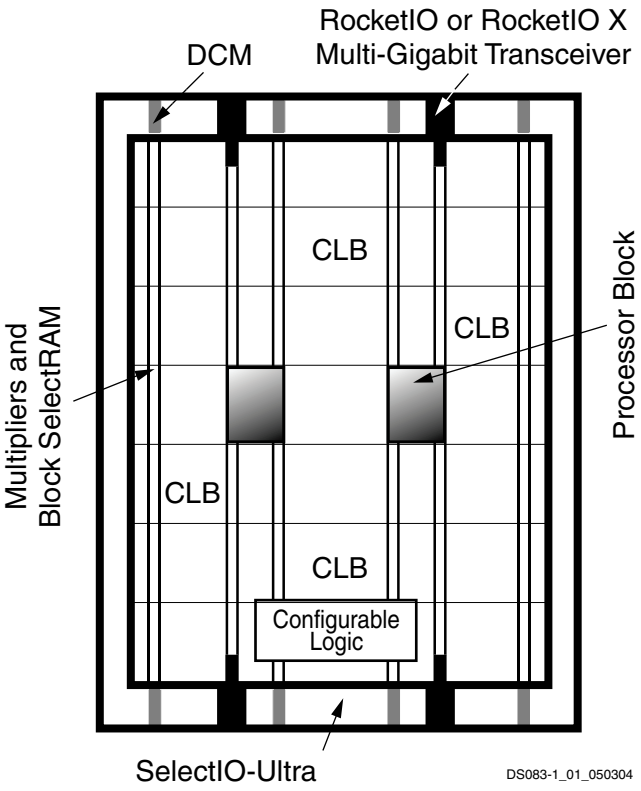

Figure 1: **Virtex-II Pro Generic Architecture Overview**

This module describes the following Virtex™-II Pro functional components, as shown in Figure 1:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in Module 3 of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see **PowerPC Processor Reference Guide** and **PowerPC 405 Processor Block Reference Guide**.
- For detailed RocketIO transceiver digital/analog design considerations, see **RocketIO Transceiver User Guide**.
- For detailed RocketIO X transceiver digital/analog design considerations, see **RocketIO X Transceiver User Guide**,
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see **Virtex-II Pro Platform FPGA User Guide**.

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

- Functional Description: RocketIO X Multi-Gigabit Transceiver (MGT)
- Functional Description: RocketIO Multi-Gigabit Transceiver (MGT)
- Functional Description: Processor Block
- Functional Description: Embedded PowerPC 405 Core
- Functional Description: FPGA
- Revision History

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX}, the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 µm has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Functional Description: RocketIO X Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO X multi-gigabit transceiver. For an in-depth discussion of the RocketIO X MGT, including digital and analog design considerations, refer to the **RocketIO X Transceiver User Guide.**

RocketIO X Overview

Either eight or twenty RocketIO X MGTs are available on the XC2VPX20 and XC2VPX70 devices, respectively. The XC2VPX20 MGT is designed to operate at any baud rate in the range of 2.488 Gb/s to 6.25 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 1. The XC2VPX70 MGT operates at a fixed 4.25 Gb/s per channel.

The RocketIO X MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 6.25 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The RocketIO X PCS has been significantly updated relative to the RocketIO PCS. In addition to the existing RocketIO PCS features, the RocketIO X PCS features 64B/66B encoder/decoder/scrambler/descrambler and SONET compatibility.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 4, page 3 shows a high-level block diagram of the RocketIO X transceiver and its FPGA interface signals.

Table 1: **Communications Standards Supported by RocketIO X Transceiver**(2)

Mode	Channels (Lanes)(1)	I/O Bit Rate (Gb/s)
SONET OC-48	1	2.488
PCI Express	1, 2, 4, 8, 16	2.5
Infiniband	1, 4, 12	2.5
XAUI (10-Gb Ethernet)	4	3.125
XAUI (10-Gb Fibre Channel)	4	3.1875
Aurora (Xilinx protocol)	1, 2, 3, 4,...	2.488 to 6.25
Custom Mode	1, 2, 3, 4,...	2.488 to 6.25

Notes:
1. One channel is considered to be one transceiver.
2. XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.

PMA

Transmitter Output

The RocketIO X transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 2. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω source resistors. The signal swing is created by switching the current in a common-source differential pair.

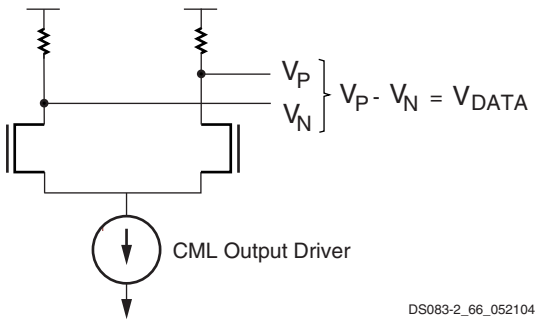

Figure 2: **CML Output Configuration**

Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by V_{TTX} at 1.5V. This configuration uses a CML approach with 50Ω termination to TXP and TXN as shown in Figure 3.

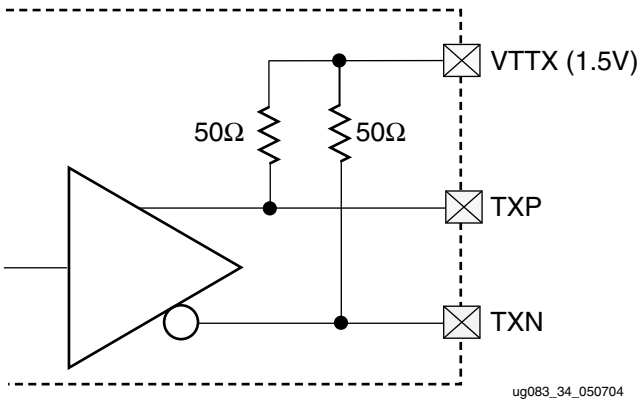

Figure 3: **RocketIO X Transmit Termination**

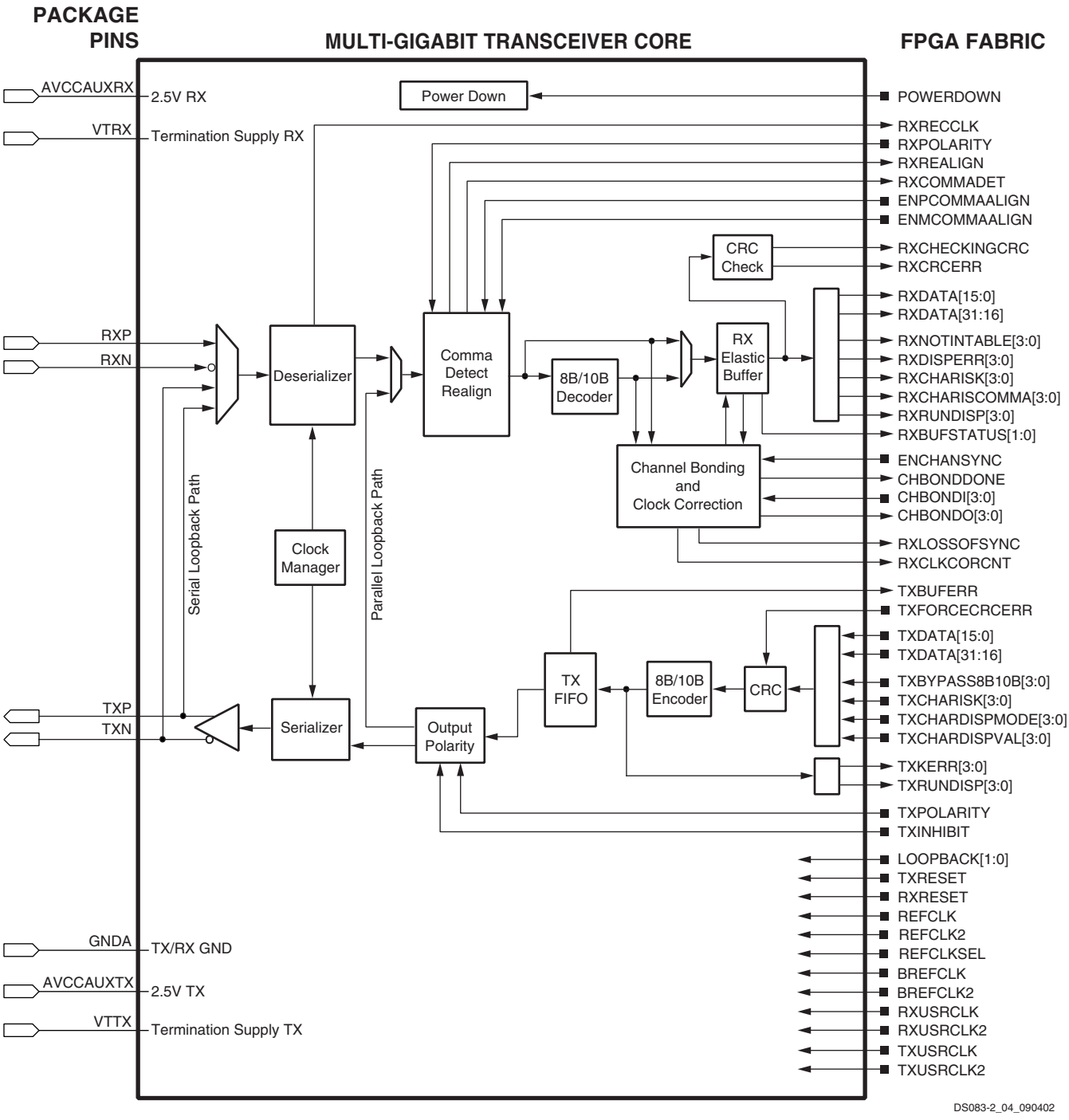

Figure 10: **RocketIO Transceiver Block Diagram**

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

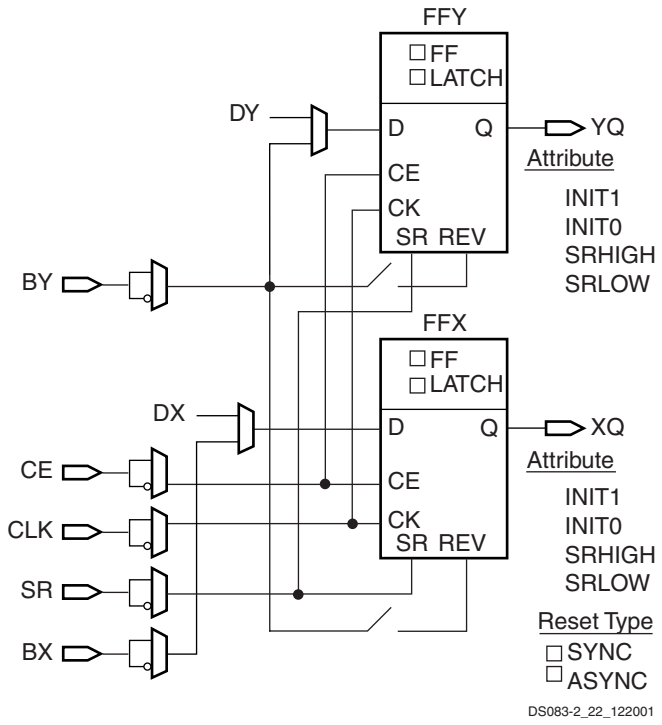

Figure 35: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM
- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: **Distributed SelectRAM+ Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

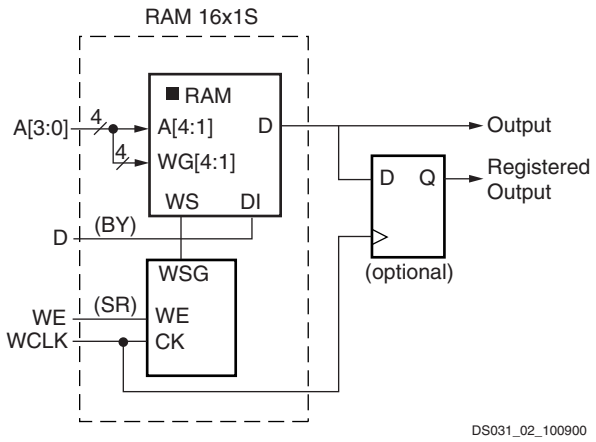

Figure 36: **Distributed SelectRAM+ (RAM16x1S)**

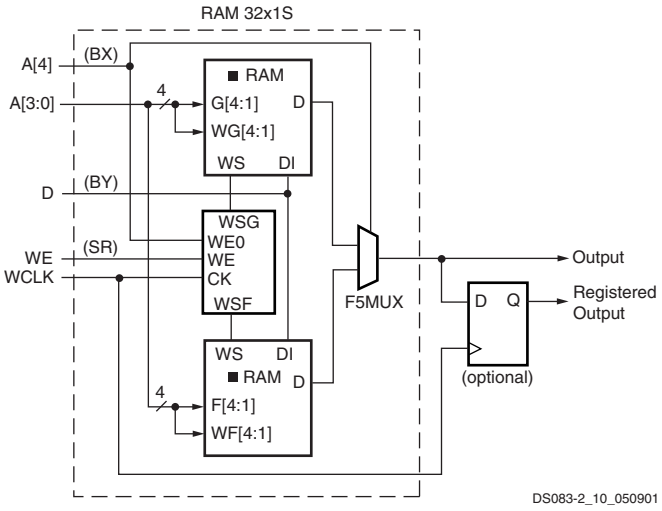

Figure 37: **Single-Port Distributed SelectRAM+ (RAM32x1S)**

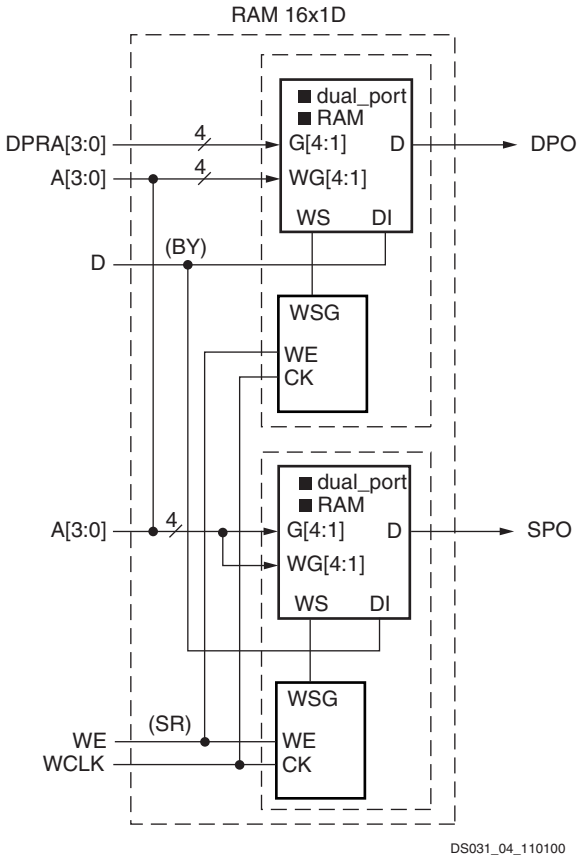

Figure 38: **Dual-Port Distributed SelectRAM+ (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

Table 17: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

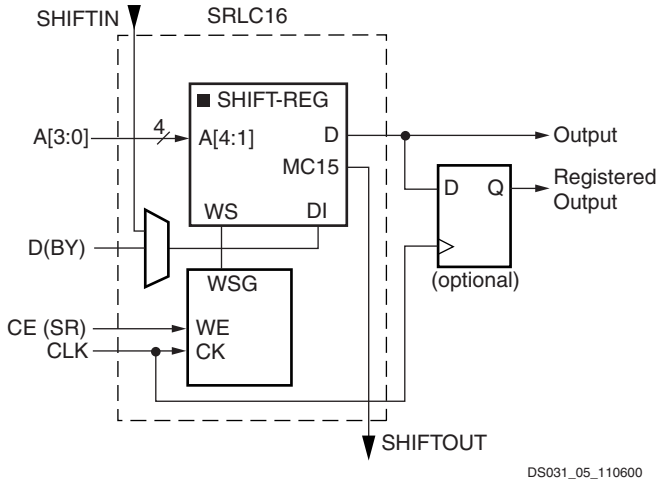

Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

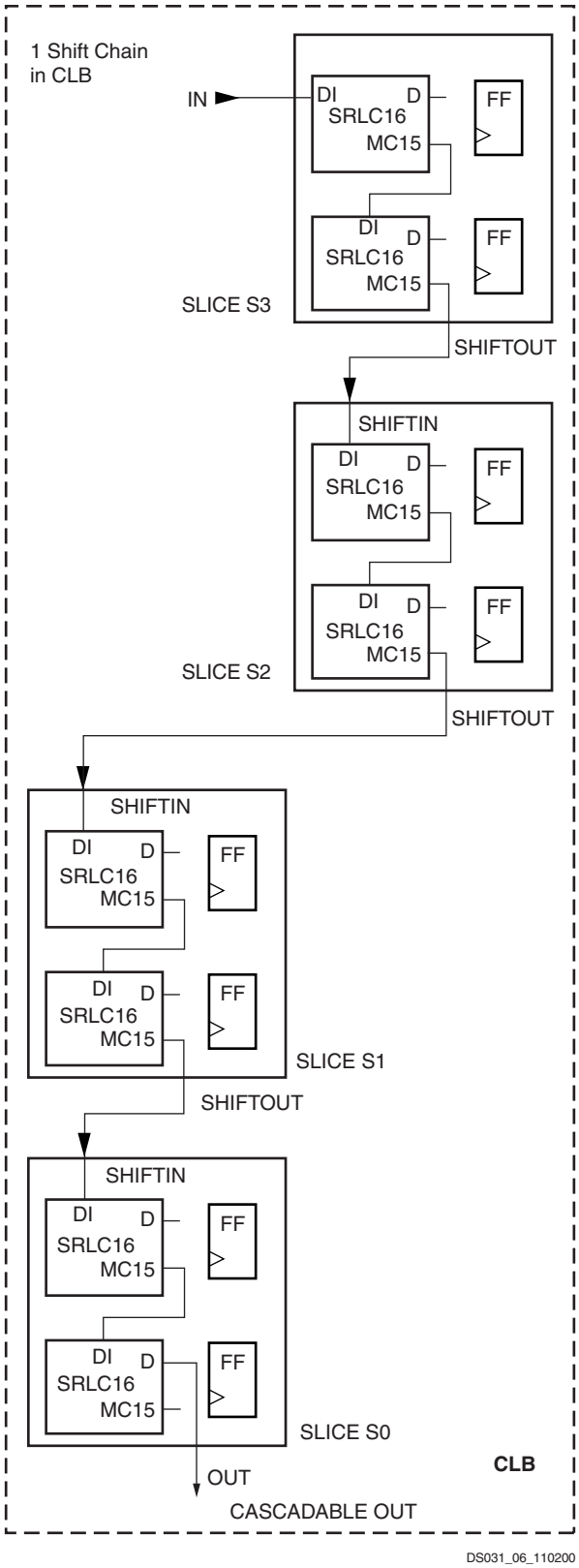

Figure 40: **Cascadable Shift Register**

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
5	IO_L06N_5/VRP_5	P5
5	IO_L06P_5/VRN_5	N5
5	IO_L03N_5/D4	T3
5	IO_L03P_5/D5	T2
5	IO_L02N_5/D6	P4
5	IO_L02P_5/D7	R3
5	IO_L01N_5/RDWR_B	P3
5	IO_L01P_5/CS_B	P2
6	IO_L01P_6/VRN_6	M3
6	IO_L01N_6/VRP_6	M2
6	IO_L02P_6	N1
6	IO_L02N_6	M1
6	IO_L03P_6	M4
6	IO_L03N_6/VREF_6	L5
6	IO_L05P_6	L4
6	IO_L05N_6	L3
6	IO_L06P_6	L2
6	IO_L06N_6	L1
6	IO_L85P_6	K4
6	IO_L85N_6	K3
6	IO_L87P_6	K2
6	IO_L87N_6/VREF_6	K1
6	IO_L89P_6	K5
6	IO_L89N_6	J4
6	IO_L90P_6	J3
6	IO_L90N_6	J2
7	IO_L90P_7	J1
7	IO_L90N_7	H1
7	IO_L88P_7	H2
7	IO_L88N_7/VREF_7	H3
7	IO_L86P_7	H4
7	IO_L86N_7	G5
7	IO_L85P_7	G1

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L52P_7	M7			
7	IO_L52N_7/VREF_7	L7			
7	IO_L50P_7	K1			
7	IO_L50N_7	K2			
7	IO_L49P_7	L3			
7	IO_L49N_7	K3			
7	IO_L48P_7	K4			
7	IO_L48N_7	K5			
7	IO_L46P_7	L8			
7	IO_L46N_7/VREF_7	K8			
7	IO_L44P_7	J1			
7	IO_L44N_7	J2			
7	IO_L43P_7	J3			
7	IO_L43N_7	J4			
7	IO_L42P_7	J5			
7	IO_L42N_7	J6			
7	IO_L40P_7	J7			
7	IO_L40N_7/VREF_7	J8			
7	IO_L38P_7	H1			
7	IO_L38N_7	H2			
7	IO_L37P_7	H6			
7	IO_L37N_7	H7			
7	IO_L36P_7	G1			
7	IO_L36N_7	G2			
7	IO_L34P_7	G3			
7	IO_L34N_7/VREF_7	G4			
7	IO_L32P_7	H5			
7	IO_L32N_7	G5			
7	IO_L31P_7	F1			
7	IO_L31N_7	F2			
7	IO_L24P_7	F3	NC		
7	IO_L24N_7	F4	NC		
7	IO_L06P_7	G6			
7	IO_L06N_7	F6			
7	IO_L04P_7	E1			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	VCCO_3	AB24			
4	VCCO_4	U14			
4	VCCO_4	U15			
4	VCCO_4	V16			
4	VCCO_4	V17			
4	VCCO_4	AC16			
4	VCCO_4	AD19			
4	VCCO_4	AD22			
5	VCCO_5	U12			
5	VCCO_5	U13			
5	VCCO_5	V10			
5	VCCO_5	V11			
5	VCCO_5	AC11			
5	VCCO_5	AD5			
5	VCCO_5	AD8			
6	VCCO_6	P10			
6	VCCO_6	R10			
6	VCCO_6	T4			
6	VCCO_6	T9			
6	VCCO_6	U9			
6	VCCO_6	W3			
6	VCCO_6	AB3			
7	VCCO_7	E3			
7	VCCO_7	H3			
7	VCCO_7	K9			
7	VCCO_7	L4			
7	VCCO_7	L9			
7	VCCO_7	M10			
7	VCCO_7	N10			
N/A	PROG_B	B1			
N/A	HSWAP_EN	B3			
N/A	DXP	A3			
N/A	DXN	C4			
N/A	AVCCAUXTX4	B5			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	RSVD	C23			
N/A	VBATT	A24			
N/A	TMS	B24			
N/A	TCK	B26			
N/A	TDO	D24			
N/A	CCLK	AE24			
N/A	PWRDWN_B	AF24			
N/A	DONE	AD23			
N/A	AVCCAUXRX16	AE23			
N/A	VTRXPAD16	AE22			
N/A	RXNPAD16	AF23			
N/A	RXPPAD16	AF22			
N/A	GNDA16	AD21			
N/A	TXPPAD16	AF21			
N/A	TXNPAD16	AF20			
N/A	VTTXPAD16	AE20			
N/A	AVCCAUXTX16	AE21			
N/A	AVCCAUXRX18	AE18			
N/A	VTRXPAD18	AE17			
N/A	RXNPAD18	AF18			
N/A	RXPPAD18	AF17			
N/A	GNDA18	AD16			
N/A	TXPPAD18	AF16			
N/A	TXNPAD18	AF15			
N/A	VTTXPAD18	AE15			
N/A	AVCCAUXTX18	AE16			
N/A	AVCCAUXRX19	AE12			
N/A	VTRXPAD19	AE11			
N/A	RXNPAD19	AF12			
N/A	RXPPAD19	AF11			
N/A	GNDA19	AD11			
N/A	TXPPAD19	AF10			
N/A	TXNPAD19	AF9			
N/A	VTTXPAD19	AE9			
N/A	AVCCAUXTX19	AE10			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	TXPPAD19		AK19			
N/A	TXNPAD19		AK20			
N/A	VTTXPAD19		AJ20			
N/A	AVCCAUXTX19		AJ19			
N/A	AVCCAUXRX21		AJ24			
N/A	VTRXPAD21		AJ25			
N/A	RXNPAD21		AK24			
N/A	RXPPAD21		AK25			
N/A	GNDA21		AH25			
N/A	TXPPAD21		AK26			
N/A	TXNPAD21		AK27			
N/A	VTTXPAD21		AJ27			
N/A	AVCCAUXTX21		AJ26			
N/A	VCCAUX		AK29			
N/A	VCCAUX		AK16			
N/A	VCCAUX		AK15			
N/A	VCCAUX		AK2			
N/A	VCCAUX		AJ30			
N/A	VCCAUX		AJ1			
N/A	VCCAUX		T30			
N/A	VCCAUX		T1			
N/A	VCCAUX		R30			
N/A	VCCAUX		R1			
N/A	VCCAUX		B30			
N/A	VCCAUX		B1			
N/A	VCCAUX		A29			
N/A	VCCAUX		A16			
N/A	VCCAUX		A15			
N/A	VCCAUX		A2			
N/A	VCCINT		Y19			
N/A	VCCINT		Y18			
N/A	VCCINT		Y17			
N/A	VCCINT		Y16			
N/A	VCCINT		Y15			
N/A	VCCINT		Y14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L34P_6	AE30				
6	IO_L34N_6	AE31				
6	IO_L35P_6	AD27				
6	IO_L35N_6	AD28				
6	IO_L36P_6	AF33				
6	IO_L36N_6	AE33				
6	IO_L37P_6	AD29				
6	IO_L37N_6	AD30				
6	IO_L38P_6	AB25				
6	IO_L38N_6	AB26				
6	IO_L39P_6	AD31				
6	IO_L39N_6/VREF_6	AD32				
6	IO_L40P_6	AC28				
6	IO_L40N_6	AC29				
6	IO_L41P_6	AB27				
6	IO_L41N_6	AB28				
6	IO_L42P_6	AE34				
6	IO_L42N_6	AD34				
6	IO_L43P_6	AC31				
6	IO_L43N_6	AC32				
6	IO_L44P_6	AA25				
6	IO_L44N_6	AA26				
6	IO_L45P_6	AD33				
6	IO_L45N_6/VREF_6	AC33				
6	IO_L46P_6	AB29				
6	IO_L46N_6	AB30				
6	IO_L47P_6	AA27				
6	IO_L47N_6	AA28				
6	IO_L48P_6	AB31				
6	IO_L48N_6	AB32				
6	IO_L49P_6	AA29				
6	IO_L49N_6	AA30				
6	IO_L50P_6	Y25				
6	IO_L50N_6	Y26				
6	IO_L51P_6	AC34				
6	IO_L51N_6/VREF_6	AB34				
6	IO_L52P_6	AA31				
6	IO_L52N_6	AA32				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AF30		
N/A	GND	AB30		
N/A	GND	W30		
N/A	GND	T30		
N/A	GND	N30		
N/A	GND	J30		
N/A	GND	E30		
N/A	GND	A30		
N/A	GND	AP26		
N/A	GND	AK26		
N/A	GND	AB26		
N/A	GND	W26		
N/A	GND	T26		
N/A	GND	N26		
N/A	GND	E26		
N/A	GND	A26		
N/A	GND	AE25		
N/A	GND	K25		
N/A	GND	AP22		
N/A	GND	AK22		
N/A	GND	AF22		
N/A	GND	J22		
N/A	GND	E22		
N/A	GND	A22		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	R21		
N/A	GND	AA20		
N/A	GND	Y20		
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	R20		
N/A	GND	P20		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L49N_2	U5		
2	IO_L49P_2	U6		
2	IO_L50N_2	U13		
2	IO_L50P_2	V13		
2	IO_L51N_2	U4		
2	IO_L51P_2	T4		
2	IO_L52N_2/VREF_2	U1		
2	IO_L52P_2	U2		
2	IO_L53N_2	V9		
2	IO_L53P_2	V10		
2	IO_L54N_2	V7		
2	IO_L54P_2	V8		
2	IO_L55N_2	V5		
2	IO_L55P_2	V6		
2	IO_L56N_2	V11		
2	IO_L56P_2	V12		
2	IO_L57N_2	V3		
2	IO_L57P_2	V4		
2	IO_L58N_2/VREF_2	V1		
2	IO_L58P_2	V2		
2	IO_L59N_2	W10		
2	IO_L59P_2	W11		
2	IO_L60N_2	W7		
2	IO_L60P_2	W8		
2	IO_L85N_2	W5		
2	IO_L85P_2	W6		
2	IO_L86N_2	W12		
2	IO_L86P_2	W13		
2	IO_L87N_2	W3		
2	IO_L87P_2	W4		
2	IO_L88N_2/VREF_2	Y7		
2	IO_L88P_2	Y8		
2	IO_L89N_2	W9		
2	IO_L89P_2	Y9		
2	IO_L90N_2	Y3		
2	IO_L90P_2	Y4		
3	IO_L90N_3	AA7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L87P_7	AA37	
7	IO_L87N_7	AA38	
7	IO_L86P_7	AA33	
7	IO_L86N_7	AA34	
7	IO_L85P_7	Y40	
7	IO_L85N_7	Y41	
7	IO_L60P_7	W41	
7	IO_L60N_7	W42	
7	IO_L59P_7	AA31	
7	IO_L59N_7	AA32	
7	IO_L58P_7	V40	
7	IO_L58N_7/VREF_7	W40	
7	IO_L57P_7	W37	
7	IO_L57N_7	W38	
7	IO_L56P_7	Y36	
7	IO_L56N_7	Y37	
7	IO_L55P_7	V41	
7	IO_L55N_7	V42	
7	IO_L54P_7	V38	
7	IO_L54N_7	V39	
7	IO_L53P_7	Y31	
7	IO_L53N_7	Y32	
7	IO_L52P_7	U40	
7	IO_L52N_7/VREF_7	U41	
7	IO_L51P_7	T40	
7	IO_L51N_7	U39	
7	IO_L50P_7	Y35	
7	IO_L50N_7	W36	
7	IO_L49P_7	T37	
7	IO_L49N_7	U37	
7	IO_L48P_7	T41	
7	IO_L48N_7	T42	
7	IO_L47P_7	Y33	
7	IO_L47N_7	W34	
7	IO_L46P_7	T38	
7	IO_L46N_7/VREF_7	T39	
7	IO_L45P_7	R36	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	AG26	
N/A	VCCINT	AF26	
N/A	VCCINT	U26	
N/A	VCCINT	T26	
N/A	VCCINT	R26	
N/A	VCCINT	AG25	
N/A	VCCINT	T25	
N/A	VCCINT	AG24	
N/A	VCCINT	T24	
N/A	VCCINT	AG23	
N/A	VCCINT	T23	
N/A	VCCINT	AG22	
N/A	VCCINT	T22	
N/A	VCCINT	AG21	
N/A	VCCINT	T21	
N/A	VCCINT	AG20	
N/A	VCCINT	T20	
N/A	VCCINT	AG19	
N/A	VCCINT	T19	
N/A	VCCINT	AG18	
N/A	VCCINT	T18	
N/A	VCCINT	AH17	
N/A	VCCINT	AG17	
N/A	VCCINT	AF17	
N/A	VCCINT	U17	
N/A	VCCINT	T17	
N/A	VCCINT	R17	
N/A	VCCINT	AJ16	
N/A	VCCINT	AH16	
N/A	VCCINT	AG16	
N/A	VCCINT	AF16	
N/A	VCCINT	AE16	
N/A	VCCINT	AD16	
N/A	VCCINT	AC16	
N/A	VCCINT	AB16	
N/A	VCCINT	AA16	
N/A	VCCINT	Y16	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	