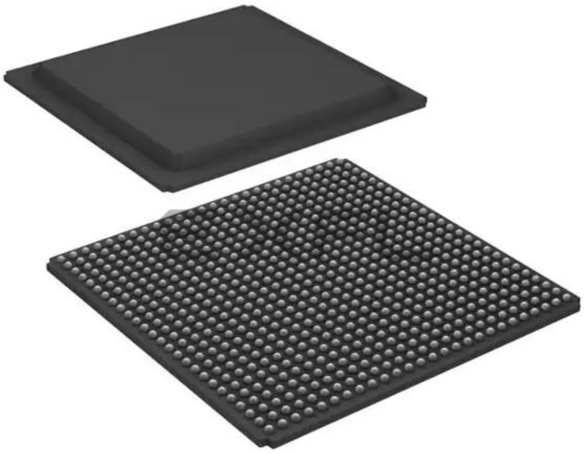

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4848 |
| Number of Logic Elements/Cells | 43632 |
| Total RAM Bits | 3538944 |
| Number of I/O | 416 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5fg676c |

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011 **Product Specification**

## Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
  - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTs)
  - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
  - Flexible logic resources
  - SRAM-based in-system configuration
  - Active Interconnect technology
  - SelectRAM™+ memory hierarchy
  - Dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectI/O™-Ultra technology
  - XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in Table 1.

*Table 1:* **Virtex-II Pro / Virtex-II Pro X FPGA Family Members**

| Device[1] | RocketIO Transceiver Blocks | PowerPC Processor Blocks | Logic Cells[2] | CLB (1 = 4 slices = max 128 bits) | | 18 X 18 Bit Multiplier Blocks | Block SelectRAM+ | | DCMs | Maximum User I/O Pads |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Slices | Max Distr RAM (Kb) | | 18 Kb Blocks | Max Block RAM (Kb) | | |
| XC2VP2 | 4 | 0 | 3,168 | 1,408 | 44 | 12 | 12 | 216 | 4 | 204 |
| XC2VP4 | 4 | 1 | 6,768 | 3,008 | 94 | 28 | 28 | 504 | 4 | 348 |
| XC2VP7 | 8 | 1 | 11,088 | 4,928 | 154 | 44 | 44 | 792 | 4 | 396 |
| XC2VP20 | 8 | 2 | 20,880 | 9,280 | 290 | 88 | 88 | 1,584 | 8 | 564 |
| XC2VPX20 | 8[4] | 1 | 22,032 | 9,792 | 306 | 88 | 88 | 1,584 | 8 | 552 |
| XC2VP30 | 8 | 2 | 30,816 | 13,696 | 428 | 136 | 136 | 2,448 | 8 | 644 |
| XC2VP40 | 0[3], 8, or 12 | 2 | 43,632 | 19,392 | 606 | 192 | 192 | 3,456 | 8 | 804 |
| XC2VP50 | 0[3] or 16 | 2 | 53,136 | 23,616 | 738 | 232 | 232 | 4,176 | 8 | 852 |
| XC2VP70 | 16 or 20 | 2 | 74,448 | 33,088 | 1,034 | 328 | 328 | 5,904 | 8 | 996 |
| XC2VPX70 | 20[4] | 2 | 74,448 | 33,088 | 1,034 | 308 | 308 | 5,544 | 8 | 992 |
| XC2VP100 | 0[3] or 20 | 2 | 99,216 | 44,096 | 1,378 | 444 | 444 | 7,992 | 12 | 1,164 |

**Notes:**
1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

## RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
  - Includes specific baud rates used by various standards, as listed in Table 4, Module 2.
- Fixed-Speed Full-Duplex Tranceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
  - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
  - 200 mV to 1600 mV, peak-peak
  - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
  - "x8" and "x10" clocking/data paths
  - 64B/66B clocking support

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

### *Transmitter Buffer*

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

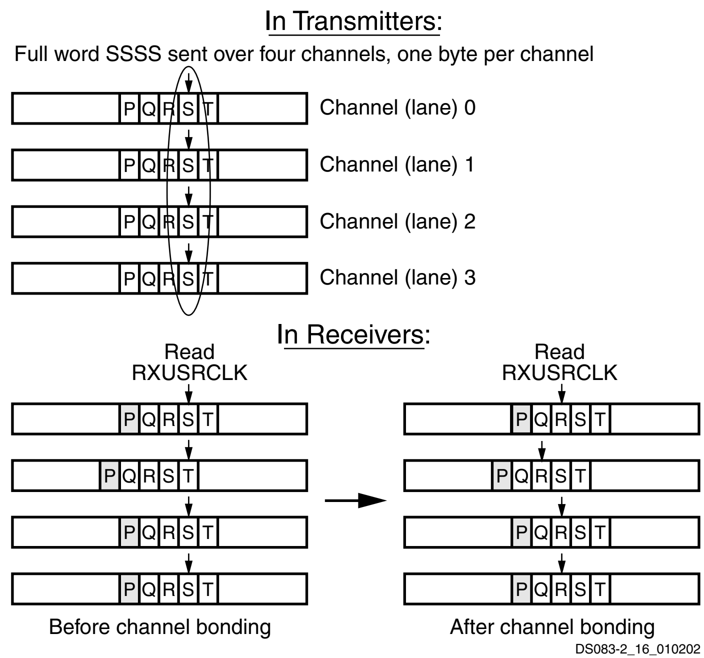



*Figure 7:* **Channel Bonding (Alignment)**

## RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

*Table 3:* **Supported RocketIO X Transceiver Primitives**

| Primitive | Description |
|---|---|
| GT10_CUSTOM | Fully customizable by user |
| GT10_OC48_1 | SONET OC-48, 1-byte data path |
| GT10_OC48_2 | SONET OC-48, 2-byte data path |
| GT10_OC48_4 | SONET OC-48, 4-byte data path |
| GT10_PCI_EXPRESS_1 | PCI Express, 1-byte data path |
| GT10_PCI_EXPRESS_2 | PCI Express, 2-byte data path |
| GT10_PCI_EXPRESS_4 | PCI Express, 4-byte data path |
| GT10_INFINIBAND_1 | Infiniband, 1-byte data path |
| GT10_INFINIBAND_2 | Infiniband, 2-byte data path |
| GT10_INFINIBAND_4 | Infiniband, 4-byte data path |

CRC may adjust certain trailing bytes to generate the required running disparity at the end of the packet.

On the receiver side, the CRC logic verifies the received CRC value, supporting the same standards as above.

The CRC logic also supports a user mode, with a simple data packet stucture beginning and ending with user-defined SOP and EOP characters.

### *Loopback*

In order to facilitate testing without having the need to either apply patterns or measure data at GHz rates, two programmable loop-back features are available.

One option, serial loopback, places the gigabit transceiver into a state where transmit data is directly fed back to the receiver. An important point to note is that the feedback path is at the output pads of the transmitter. This tests the entirety of the transmitter and receiver.

The second option, parallel loopback, checks the digital circuitry. When parallel loopback is enabled, the serial loopback path is disabled. However, the transmitter outputs remain active, and data can be transmitted. If TXINHIBIT is asserted, TXP is forced to 0 until TXINHIBIT is de-asserted.

### *Reset*

The receiver and transmitter have their own synchronous reset inputs. The transmitter reset recenters the transmission FIFO, and resets all transmitter registers and the 8B/10B decoder. The receiver reset recenters the receiver elastic buffer, and resets all receiver registers and the 8B/10B encoder. Neither reset has any effect on the PLLs.

### *Power*

All RocketIO transceivers in the FPGA, whether instantiated in the design or not, must be connected to power and ground. Unused transceivers can be powered by any 2.5V source, and passive filtering is not required.

### *Power Down*

The Power Down module is controlled by the transceiver's POWERDOWN input pin. The Power Down pin on the FPGA package has no effect on the transceiver.

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

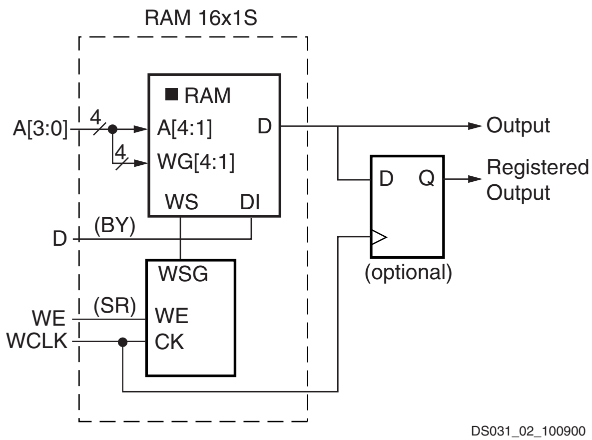



*Figure 36:* **Distributed SelectRAM+ (RAM16x1S)**

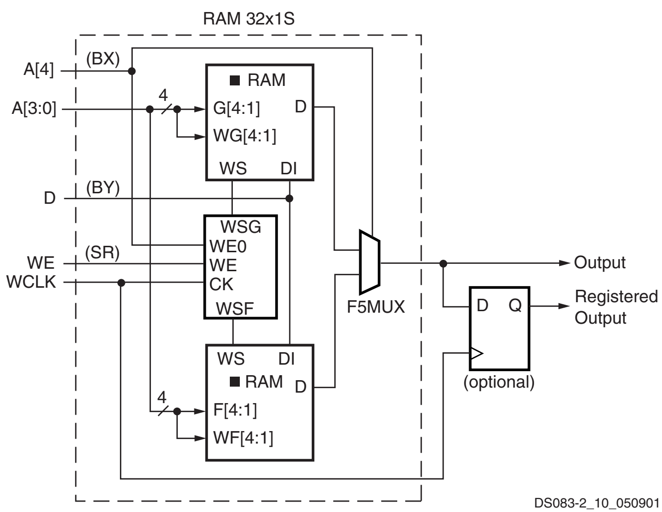



*Figure 37:* **Single-Port Distributed SelectRAM+ (RAM32x1S)**

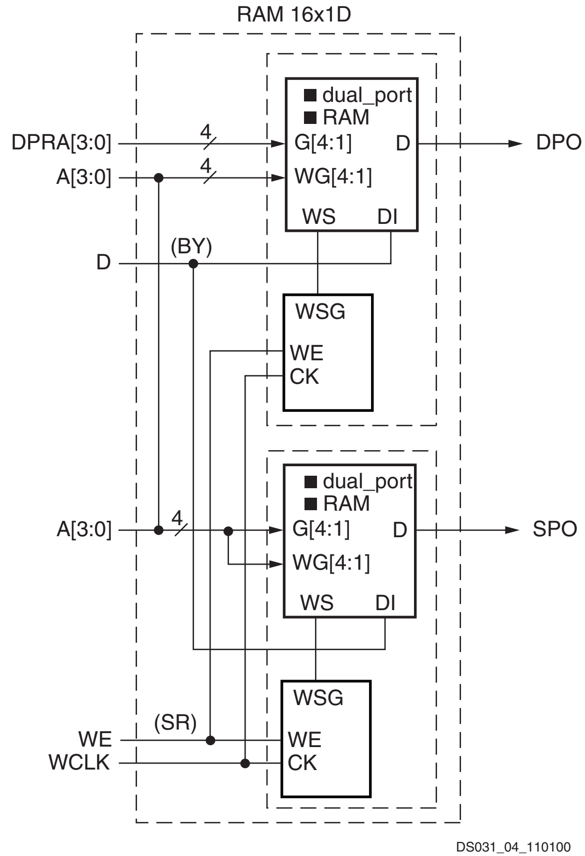



*Figure 38:* **Dual-Port Distributed SelectRAM+ (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

*Table 17:* **ROM Configuration**

| ROM | Number of LUTs |
|---|---|
| 16 x 1 | 1 |
| 32 x 1 | 2 |
| 64 x 1 | 4 |
| 128 x 1 | 8 (1 CLB) |
| 256 x 1 | 16 (2 CLBs) |

*Table 34:* **RocketIO TXUSRCLK2 Switching Characteristics**

| Description | Symbol | Speed Grade -7 | Speed Grade -6 | Speed Grade -5 | Units |
|---|---|---|---|---|---|
| **Setup and Hold Relative to Clock (TXUSRCLK2)** | | | | | |
| CONFIGENABLE control input | $T_{GCCK}$_CFGEN/$T_{GCKC}$_CFGEN | 0.35/ 0.10 | 0.35/ 0.10 | 0.39/ 0.11 | ns, min |
| TXBYPASS8B10B control inputs | $T_{GCCK}$_TBYP/$T_{GCKC}$_TBYP | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXFORCECRCERR control input | $T_{GCCK}$_TCRCE/$T_{GCKC}$_TCRCE | 0.39/ 0.12 | 0.44/ 0.14 | 0.49/ 0.15 | ns, min |
| TXPOLARITY control input | $T_{GCCK}$_TPOL/$T_{GCKC}$_TPOL | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXINHIBIT control inputs | $T_{GCCK}$_TINH/$T_{GCKC}$_TINH | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| LOOPBACK control inputs | $T_{GCCK}$_LBK/$T_{GCKC}$_LBK | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXRESET control input | $T_{GCCK}$_TRST/$T_{GCKC}$_TRST | 0.02/ 0.10 | 0.02/ 0.10 | 0.02/ 0.11 | ns, min |
| TXCHARISK control inputs | $T_{GCCK}$_TKCH/$T_{GCKC}$_TKCH | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXCHARDISPMODE control inputs | $T_{GCCK}$_TCDM/$T_{GCKC}$_TCDM | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXCHARDISPVAL control inputs | $T_{GCCK}$_TCDV/$T_{GCKC}$_TCDV | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| CONFIGIN data input | $T_{GDCK}$_CFGIN/$T_{GCKD}$_CFGIN | 0.35/ 0.10 | 0.35/ 0.10 | 0.39/ 0.11 | ns, min |
| TXDATA data inputs | $T_{GDCK}$_TDAT/$T_{GCKD}$_TDAT | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| **Clock to Out** | | | | | |
| TXBUFERR status output | $T_{GCKST}$_TBERR | 0.54 | 0.54 | 0.60 | ns, max |
| TXKERR status outputs | $T_{GCKST}$_TKERR | 0.41 | 0.41 | 0.46 | ns, max |
| TXRUNDISP status outputs | $T_{GCKST}$_TRDIS | 0.41 | 0.41 | 0.46 | ns, max |
| CONFIGOUT data output | $T_{GCKDO}$_CFGOUT | 0.25 | 0.25 | 0.28 | ns, max |
| **Clock** | | | | | |
| TXUSRCLK2 minimum pulse width, High | $T_{GPWH}$_TX2 | 1.42 | 1.42 | 2.25 | ns, min |
| TXUSRCLK2 minimum pulse width, Low | $T_{GPWL}$_TX2 | 1.42 | 1.42 | 2.25 | ns, min |

*Table 5:* **FG256/FGG256 — XC2VP2 and XC2VP4**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 7 | VCCO_7 | G6 |
| | | |
| N/A | CCLK | N15 |
| N/A | PROG_B | D1 |
| N/A | DONE | P16 |
| N/A | M0 | N3 |
| N/A | M1 | N2 |
| N/A | M2 | P1 |
| N/A | TCK | D16 |
| N/A | TDI | E1 |
| N/A | TDO | E16 |
| N/A | TMS | C16 |
| N/A | PWRDWN_B | N14 |
| N/A | HSWAP_EN | C1 |
| N/A | RSVD | D14 |
| N/A | VBATT | D15 |
| N/A | DXP | D2 |
| N/A | DXN | D3 |
| N/A | AVCCAUXTX6 | B5 |
| N/A | VTTXPAD6 | B4 |
| N/A | TXNPAD6 | A4 |
| N/A | TXPPAD6 | A5 |
| N/A | GNDA6 | C6 |
| N/A | RXPPAD6 | A6 |
| N/A | RXNPAD6 | A7 |
| N/A | VTRXPAD6 | B6 |
| N/A | AVCCAUXRX6 | B7 |
| N/A | AVCCAUXTX7 | B11 |
| N/A | VTTXPAD7 | B10 |
| N/A | TXNPAD7 | A10 |
| N/A | TXPPAD7 | A11 |
| N/A | GNDA7 | C11 |
| N/A | RXPPAD7 | A12 |
| N/A | RXNPAD7 | A13 |
| N/A | VTRXPAD7 | B12 |

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| 0 | IO_L55N_0 | G12 | | | |
| 0 | IO_L55P_0 | F12 | | | |
| 0 | IO_L57N_0 | E12 | | | |
| 0 | IO_L57P_0/VREF_0 | F13 | | | |
| 0 | IO_L67N_0 | D12 | | | |
| 0 | IO_L67P_0 | C12 | | | |
| 0 | IO_L69N_0 | J13 | | | |
| 0 | IO_L69P_0/VREF_0 | H13 | | | |
| 0 | IO_L74N_0/GCLK7P | E13 | | | |
| 0 | IO_L74P_0/GCLK6S | D13 | | | |
| 0 | IO_L75N_0/GCLK5P | C13 | | | |
| 0 | IO_L75P_0/GCLK4S | B13 | | | |
| | | | | | |
| 1 | IO_L75N_1/GCLK3P | B14 | | | |
| 1 | IO_L75P_1/GCLK2S | C14 | | | |
| 1 | IO_L74N_1/GCLK1P | D14 | | | |
| 1 | IO_L74P_1/GCLK0S | E14 | | | |
| 1 | IO_L69N_1/VREF_1 | H14 | | | |
| 1 | IO_L69P_1 | J14 | | | |
| 1 | IO_L67N_1 | C15 | | | |
| 1 | IO_L67P_1 | D15 | | | |
| 1 | IO_L57N_1/VREF_1 | F14 | | | |
| 1 | IO_L57P_1 | E15 | | | |
| 1 | IO_L55N_1 | F15 | | | |
| 1 | IO_L55P_1 | G15 | | | |
| 1 | IO_L54N_1 | H15 | | | |
| 1 | IO_L54P_1 | J15 | | | |
| 1 | IO_L53_1/No_Pair | F16 | | | |
| 1 | IO_L50_1/No_Pair | G16 | | | |
| 1 | IO_L49N_1 | C17 | | | |
| 1 | IO_L49P_1 | D17 | | | |
| 1 | IO_L48N_1 | E16 | | | |
| 1 | IO_L48P_1 | E17 | | | |
| 1 | IO_L46N_1 | H16 | | | |
| 1 | IO_L46P_1 | H17 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| N/A | RXPPAD7 | | A12 | | | |
| N/A | RXNPAD7 | | A11 | | | |
| N/A | VTRXPAD7 | | B12 | | | |
| N/A | AVCCAUXRX7 | | B11 | | | |
| N/A | AVCCAUXTX9 | | B6 | | | |
| N/A | VTTXPAD9 | | B7 | | | |
| N/A | TXNPAD9 | | A7 | | | |
| N/A | TXPPAD9 | | A6 | | | |
| N/A | GNDA9 | | C6 | | | |
| N/A | RXPPAD9 | | A5 | | | |
| N/A | RXNPAD9 | | A4 | | | |
| N/A | VTRXPAD9 | | B5 | | | |
| N/A | AVCCAUXRX9 | | B4 | | | |
| N/A | AVCCAUXRX16 | | AJ4 | | | |
| N/A | VTRXPAD16 | | AJ5 | | | |
| N/A | RXNPAD16 | | AK4 | | | |
| N/A | RXPPAD16 | | AK5 | | | |
| N/A | GNDA16 | | AH6 | | | |
| N/A | TXPPAD16 | | AK6 | | | |
| N/A | TXNPAD16 | | AK7 | | | |
| N/A | VTTXPAD16 | | AJ7 | | | |
| N/A | AVCCAUXTX16 | | AJ6 | | | |
| N/A | AVCCAUXRX18 | | AJ11 | | | |
| N/A | VTRXPAD18 | | AJ12 | | | |
| N/A | RXNPAD18 | | AK11 | | | |
| N/A | RXPPAD18 | | AK12 | | | |
| N/A | GNDA18 | | AH12 | | | |
| N/A | TXPPAD18 | | AK13 | | | |
| N/A | TXNPAD18 | | AK14 | | | |
| N/A | VTTXPAD18 | | AJ14 | | | |
| N/A | AVCCAUXTX18 | | AJ13 | | | |
| N/A | AVCCAUXRX19 | | AJ17 | | | |
| N/A | VTRXPAD19 | | AJ18 | | | |
| N/A | RXNPAD19 | | AK17 | | | |
| N/A | RXPPAD19 | | AK18 | | | |
| N/A | GNDA19 | | AH19 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 2 | IO_L57N_2 | R4 | | | | |
| 2 | IO_L57P_2 | R3 | | | | |
| 2 | IO_L58N_2/VREF_2 | R2 | | | | |
| 2 | IO_L58P_2 | T2 | | | | |
| 2 | IO_L59N_2 | T8 | | | | |
| 2 | IO_L59P_2 | T7 | | | | |
| 2 | IO_L60N_2 | T6 | | | | |
| 2 | IO_L60P_2 | T5 | | | | |
| 2 | IO_L85N_2 | T4 | | | | |
| 2 | IO_L85P_2 | T3 | | | | |
| 2 | IO_L86N_2 | U10 | | | | |
| 2 | IO_L86P_2 | U9 | | | | |
| 2 | IO_L87N_2 | U6 | | | | |
| 2 | IO_L87P_2 | U5 | | | | |
| 2 | IO_L88N_2/VREF_2 | U2 | | | | |
| 2 | IO_L88P_2 | V2 | | | | |
| 2 | IO_L89N_2 | U8 | | | | |
| 2 | IO_L89P_2 | U7 | | | | |
| 2 | IO_L90N_2 | U4 | | | | |
| 2 | IO_L90P_2 | U3 | | | | |
| | | | | | | |
| 3 | IO_L90N_3 | V3 | | | | |
| 3 | IO_L90P_3 | V4 | | | | |
| 3 | IO_L89N_3 | V7 | | | | |
| 3 | IO_L89P_3 | V8 | | | | |
| 3 | IO_L88N_3 | V5 | | | | |
| 3 | IO_L88P_3 | V6 | | | | |
| 3 | IO_L87N_3/VREF_3 | W2 | | | | |
| 3 | IO_L87P_3 | Y2 | | | | |
| 3 | IO_L86N_3 | V9 | | | | |
| 3 | IO_L86P_3 | V10 | | | | |
| 3 | IO_L85N_3 | W3 | | | | |
| 3 | IO_L85P_3 | W4 | | | | |
| 3 | IO_L60N_3 | Y1 | | | | |
| 3 | IO_L60P_3 | AA1 | | | | |
| 3 | IO_L59N_3 | V11 | | | | |
| 3 | IO_L59P_3 | W11 | | | | |
| 3 | IO_L58N_3 | W5 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 7 | IO_L51P_7 | N31 | | |
| 7 | IO_L51N_7 | P31 | | |
| 7 | IO_L50P_7 | T27 | | |
| 7 | IO_L50N_7 | R28 | | |
| 7 | IO_L49P_7 | M33 | | |
| 7 | IO_L49N_7 | M34 | | |
| 7 | IO_L48P_7 | M31 | | |
| 7 | IO_L48N_7 | M32 | | |
| 7 | IO_L47P_7 | R24 | | |
| 7 | IO_L47N_7 | R25 | | |
| 7 | IO_L46P_7 | M29 | | |
| 7 | IO_L46N_7/VREF_7 | M30 | | |
| 7 | IO_L45P_7 | L33 | | |
| 7 | IO_L45N_7 | L34 | | |
| 7 | IO_L44P_7 | P27 | | |
| 7 | IO_L44N_7 | P28 | | |
| 7 | IO_L43P_7 | L29 | | |
| 7 | IO_L43N_7 | L30 | | |
| 7 | IO_L42P_7 | K33 | | |
| 7 | IO_L42N_7 | K34 | | |
| 7 | IO_L41P_7 | P26 | | |
| 7 | IO_L41N_7 | R26 | | |
| 7 | IO_L40P_7 | K32 | | |
| 7 | IO_L40N_7/VREF_7 | L32 | | |
| 7 | IO_L39P_7 | K29 | | |
| 7 | IO_L39N_7 | K30 | | |
| 7 | IO_L38P_7 | P24 | | |
| 7 | IO_L38N_7 | P25 | | |
| 7 | IO_L37P_7 | J32 | | |
| 7 | IO_L37N_7 | J33 | | |
| 7 | IO_L36P_7 | J31 | | |
| 7 | IO_L36N_7 | K31 | | |
| 7 | IO_L35P_7 | N28 | | |
| 7 | IO_L35N_7 | N29 | | |
| 7 | IO_L34P_7 | H32 | | |
| 7 | IO_L34N_7/VREF_7 | H33 | | |
| 7 | IO_L33P_7 | H29 | | |
| 7 | IO_L33N_7 | H30 | | |

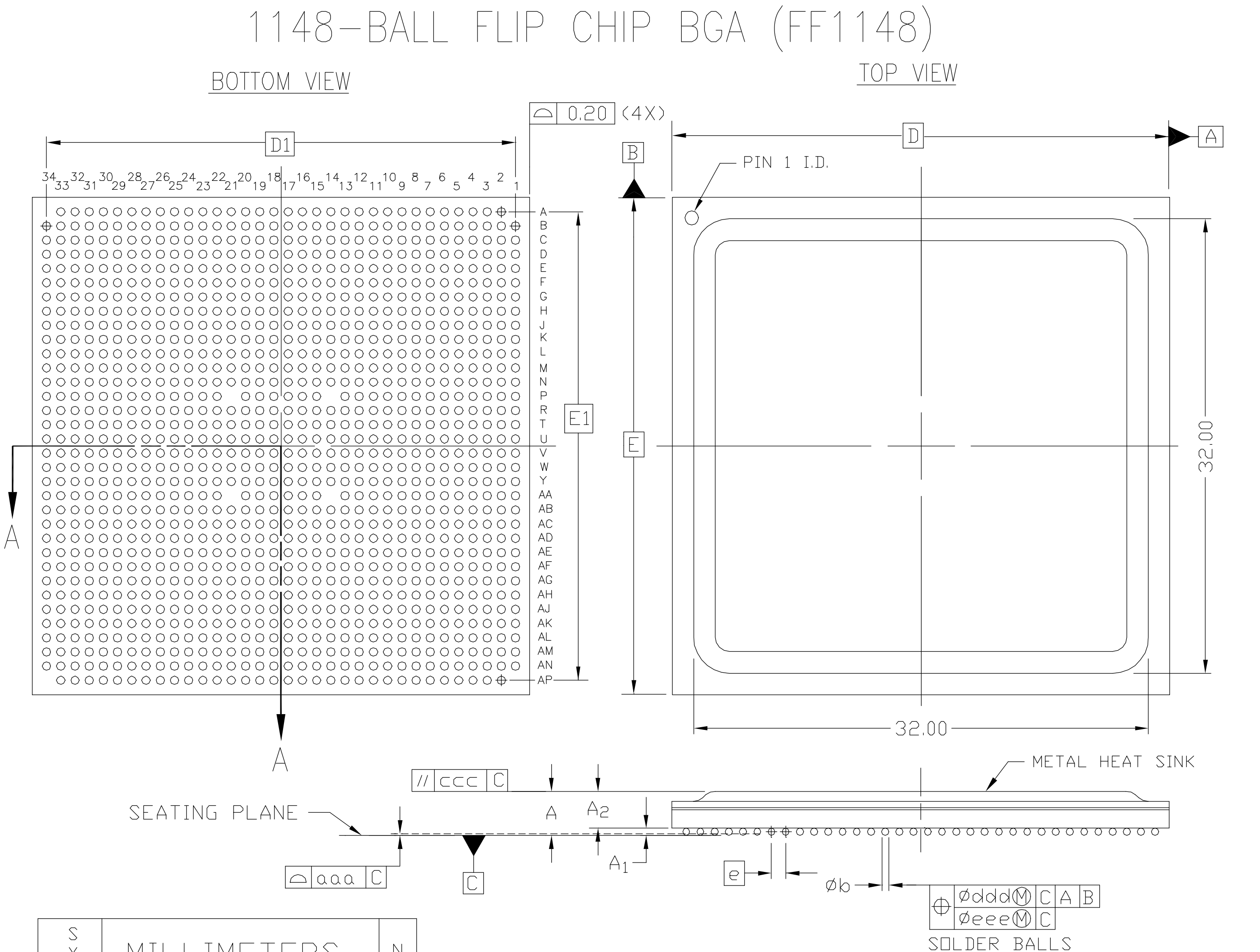
*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

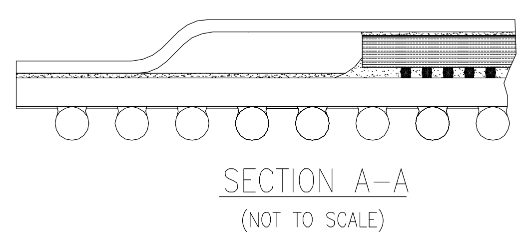
| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 4 | VCCO_4 | AD12 | | |
| 4 | VCCO_4 | AL11 | | |
| 4 | VCCO_4 | AG11 | | |
| 3 | VCCO_3 | AB12 | | |
| 3 | VCCO_3 | AA12 | | |
| 3 | VCCO_3 | Y12 | | |
| 3 | VCCO_3 | W12 | | |
| 3 | VCCO_3 | V12 | | |
| 3 | VCCO_3 | AC11 | | |
| 3 | VCCO_3 | AF9 | | |
| 3 | VCCO_3 | AM8 | | |
| 3 | VCCO_3 | AH8 | | |
| 3 | VCCO_3 | AD8 | | |
| 3 | VCCO_3 | Y8 | | |
| 3 | VCCO_3 | AM4 | | |
| 3 | VCCO_3 | AH4 | | |
| 3 | VCCO_3 | AD4 | | |
| 3 | VCCO_3 | Y4 | | |
| 3 | VCCO_3 | AK2 | | |
| 2 | VCCO_2 | U12 | | |
| 2 | VCCO_2 | T12 | | |
| 2 | VCCO_2 | R12 | | |
| 2 | VCCO_2 | P12 | | |
| 2 | VCCO_2 | N12 | | |
| 2 | VCCO_2 | M11 | | |
| 2 | VCCO_2 | J9 | | |
| 2 | VCCO_2 | R8 | | |
| 2 | VCCO_2 | L8 | | |
| 2 | VCCO_2 | G8 | | |
| 2 | VCCO_2 | C8 | | |
| 2 | VCCO_2 | R4 | | |
| 2 | VCCO_2 | L4 | | |
| 2 | VCCO_2 | G4 | | |
| 2 | VCCO_2 | C4 | | |
| 2 | VCCO_2 | E2 | | |
| 1 | VCCO_1 | M17 | | |
| 1 | VCCO_1 | M16 | | |
| 1 | VCCO_1 | M15 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 1 | VCCO_1 | H15 | | |
| 1 | VCCO_1 | D15 | | |
| 1 | VCCO_1 | M14 | | |
| 1 | VCCO_1 | M13 | | |
| 1 | VCCO_1 | L12 | | |
| 1 | VCCO_1 | H11 | | |
| 1 | VCCO_1 | D11 | | |
| 0 | VCCO_0 | H24 | | |
| 0 | VCCO_0 | D24 | | |
| 0 | VCCO_0 | L23 | | |
| 0 | VCCO_0 | M22 | | |
| 0 | VCCO_0 | M21 | | |
| 0 | VCCO_0 | M20 | | |
| 0 | VCCO_0 | H20 | | |
| 0 | VCCO_0 | D20 | | |
| 0 | VCCO_0 | M19 | | |
| 0 | VCCO_0 | M18 | | |
| | | | | |
| N/A | CCLK | AG9 | | |
| N/A | PROG_B | G26 | | |
| N/A | DONE | AF10 | | |
| N/A | M0 | AG25 | | |
| N/A | M1 | AG26 | | |
| N/A | M2 | AF25 | | |
| N/A | TCK | G9 | | |
| N/A | TDI | F26 | | |
| N/A | TDO | F9 | | |
| N/A | TMS | H10 | | |
| N/A | PWRDWN_B | AG10 | | |
| N/A | HSWAP_EN | H25 | | |
| N/A | RSVD | H9 | | |
| N/A | VBATT | J10 | | |
| N/A | DXP | J25 | | |
| N/A | DXN | H26 | | |
| | | | | |
| N/A | VCCINT | AD24 | | |
| N/A | VCCINT | L24 | | |
| N/A | VCCINT | AC23 | | |

## FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | — | 3.20 | 3.40 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | — | — | 2.80 | |
| D/E | 35.00 BASIC | | | |
| $D_1/E_1$ | 33.00 REF | | | |
| e | 1.00 BASIC | | | |
| Øb | 0.50 | 0.60 | 0.70 | |
| aaa | — | — | 0.20 | |
| ccc | — | — | 0.35 | |
| ddd | — | — | 0.30 | |
| eee | — | — | 0.10 | |
| M | 34 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

*Figure 7:* **FF1148 Flip-Chip Fine-Pitch BGA Package Specifications**

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 0 | IO_L34P_0 | E27 | NC | |
| 0 | IO_L35N_0 | L26 | NC | |
| 0 | IO_L35P_0 | L25 | NC | |
| 0 | IO_L36N_0 | G26 | NC | |
| 0 | IO_L36P_0/VREF_0 | H26 | NC | |
| 0 | IO_L37N_0 | E26 | | |
| 0 | IO_L37P_0 | F26 | | |
| 0 | IO_L38N_0 | K25 | | |
| 0 | IO_L38P_0 | K24 | | |
| 0 | IO_L39N_0 | C26 | | |
| 0 | IO_L39P_0 | D26 | | |
| 0 | IO_L43N_0 | H25 | | |
| 0 | IO_L43P_0 | J25 | | |
| 0 | IO_L44N_0 | M25 | | |
| 0 | IO_L44P_0 | M24 | | |
| 0 | IO_L45N_0 | F25 | | |
| 0 | IO_L45P_0/VREF_0 | G25 | | |
| 0 | IO_L46N_0 | C25 | | |
| 0 | IO_L46P_0 | D25 | | |
| 0 | IO_L47N_0 | L23 | | |
| 0 | IO_L47P_0 | M22 | | |
| 0 | IO_L48N_0 | H24 | | |
| 0 | IO_L48P_0 | J24 | | |
| 0 | IO_L49N_0 | E25 | | |
| 0 | IO_L49P_0 | E24 | | |
| 0 | IO_L50_0/No_Pair | N23 | | |
| 0 | IO_L53_0/No_Pair | M23 | | |
| 0 | IO_L54N_0 | H23 | | |
| 0 | IO_L54P_0 | J23 | | |
| 0 | IO_L55N_0 | F24 | | |
| 0 | IO_L55P_0 | G23 | | |
| 0 | IO_L56N_0 | K22 | | |
| 0 | IO_L56P_0 | L22 | | |
| 0 | IO_L57N_0 | C23 | | |
| 0 | IO_L57P_0/VREF_0 | D23 | | |
| 0 | IO_L58N_0 | H22 | | |
| 0 | IO_L58P_0 | J22 | | |
| 0 | IO_L59N_0 | N22 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 1 | IO_L64N_1 | E18 | | |
| 1 | IO_L64P_1 | D18 | | |
| 1 | IO_L60N_1 | G18 | | |
| 1 | IO_L60P_1 | F18 | | |
| 1 | IO_L59N_1 | L18 | | |
| 1 | IO_L59P_1 | K18 | | |
| 1 | IO_L58N_1 | J18 | | |
| 1 | IO_L58P_1 | H18 | | |
| 1 | IO_L57N_1/VREF_1 | D17 | | |
| 1 | IO_L57P_1 | C17 | | |
| 1 | IO_L56N_1 | N18 | | |
| 1 | IO_L56P_1 | M18 | | |
| 1 | IO_L55N_1 | E17 | | |
| 1 | IO_L55P_1 | E16 | | |
| 1 | IO_L54N_1 | G17 | | |
| 1 | IO_L54P_1 | F16 | | |
| 1 | IO_L53_1/No_Pair | J17 | | |
| 1 | IO_L50_1/No_Pair | H17 | | |
| 1 | IO_L49N_1 | J16 | | |
| 1 | IO_L49P_1 | H16 | | |
| 1 | IO_L48N_1 | D15 | | |
| 1 | IO_L48P_1 | C15 | | |
| 1 | IO_L47N_1 | L17 | | |
| 1 | IO_L47P_1 | K16 | | |
| 1 | IO_L46N_1 | F15 | | |
| 1 | IO_L46P_1 | E15 | | |
| 1 | IO_L45N_1/VREF_1 | H15 | | |
| 1 | IO_L45P_1 | G15 | | |
| 1 | IO_L44N_1 | N17 | | |
| 1 | IO_L44P_1 | M17 | | |
| 1 | IO_L43N_1 | D14 | | |
| 1 | IO_L43P_1 | C14 | | |
| 1 | IO_L39N_1 | F14 | | |
| 1 | IO_L39P_1 | E14 | | |
| 1 | IO_L38N_1 | M16 | | |
| 1 | IO_L38P_1 | M15 | | |
| 1 | IO_L37N_1 | H14 | | |
| 1 | IO_L37P_1 | G14 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 3 | IO_L09P_3 | AM3 | | |
| 3 | IO_L08N_3 | AK8 | | |
| 3 | IO_L08P_3 | AK9 | | |
| 3 | IO_L07N_3 | AN6 | | |
| 3 | IO_L07P_3 | AN7 | | |
| 3 | IO_L84N_3 | AN3 | NC | |
| 3 | IO_L84P_3 | AN4 | NC | |
| 3 | IO_L82N_3 | AN1 | NC | |
| 3 | IO_L82P_3 | AN2 | NC | |
| 3 | IO_L81N_3/VREF_3 | AN5 | NC | |
| 3 | IO_L81P_3 | AP5 | NC | |
| 3 | IO_L79N_3 | AP3 | NC | |
| 3 | IO_L79P_3 | AP4 | NC | |
| 3 | IO_L78N_3 | AP1 | NC | |
| 3 | IO_L78P_3 | AP2 | NC | |
| 3 | IO_L76N_3 | AR2 | NC | |
| 3 | IO_L76P_3 | AR3 | NC | |
| 3 | IO_L75N_3/VREF_3 | AT1 | NC | |
| 3 | IO_L75P_3 | AT2 | NC | |
| 3 | IO_L73N_3 | AT5 | NC | |
| 3 | IO_L73P_3 | AU5 | NC | |
| 3 | IO_L06N_3 | AR6 | | |
| 3 | IO_L06P_3 | AT6 | | |
| 3 | IO_L05N_3 | AL9 | | |
| 3 | IO_L05P_3 | AM8 | | |
| 3 | IO_L04N_3 | AP7 | | |
| 3 | IO_L04P_3 | AR7 | | |
| 3 | IO_L03N_3/VREF_3 | AM9 | | |
| 3 | IO_L03P_3 | AN9 | | |
| 3 | IO_L02N_3 | AR8 | | |
| 3 | IO_L02P_3 | AT8 | | |
| 3 | IO_L01N_3/VRP_3 | AT7 | | |
| 3 | IO_L01P_3/VRN_3 | AU7 | | |
| | | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | AT9 | | |
| 4 | IO_L01P_4/INIT_B | AR9 | | |
| 4 | IO_L02N_4/D0/DIN(1) | AK11 | | |
| 4 | IO_L02P_4/D1 | AK12 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | IO_L17N_3 | | AL9 | | |
| 3 | IO_L17P_3 | | AL10 | | |
| 3 | IO_L16N_3 | | AM1 | | |
| 3 | IO_L16P_3 | | AM2 | | |
| 3 | IO_L15N_3/VREF_3 | | AM3 | | |
| 3 | IO_L15P_3 | | AN3 | | |
| 3 | IO_L14N_3 | | AM8 | | |
| 3 | IO_L14P_3 | | AM9 | | |
| 3 | IO_L13N_3 | | AM4 | | |
| 3 | IO_L13P_3 | | AM5 | | |
| 3 | IO_L12N_3 | | AM6 | | |
| 3 | IO_L12P_3 | | AM7 | | |
| 3 | IO_L11N_3 | | AN9 | | |
| 3 | IO_L11P_3 | | AM10 | | |
| 3 | IO_L10N_3 | | AN1 | | |
| 3 | IO_L10P_3 | | AN2 | | |
| 3 | IO_L09N_3/VREF_3 | | AN5 | | |
| 3 | IO_L09P_3 | | AN6 | | |
| 3 | IO_L08N_3 | | AN7 | | |
| 3 | IO_L08P_3 | | AN8 | | |
| 3 | IO_L07N_3 | | AP1 | | |
| 3 | IO_L07P_3 | | AP2 | | |
| 3 | IO_L84N_3 | | AP4 | | |
| 3 | IO_L84P_3 | | AP5 | | |
| 3 | IO_L83N_3 | | AR7 | | |
| 3 | IO_L83P_3 | | AP8 | | |
| 3 | IO_L82N_3 | | AP6 | | |
| 3 | IO_L82P_3 | | AP7 | | |
| 3 | IO_L81N_3/VREF_3 | | AR2 | | |
| 3 | IO_L81P_3 | | AR3 | | |
| 3 | IO_L80N_3 | | AT5 | | |
| 3 | IO_L80P_3 | | AR6 | | |
| 3 | IO_L79N_3 | | AR4 | | |
| 3 | IO_L79P_3 | | AR5 | | |
| 3 | IO_L78N_3 | | AT1 | | |
| 3 | IO_L78P_3 | | AT2 | | |

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 5 | IO_L19P_5 | | AV32 | | |
| 5 | IO_L09N_5/VREF_5 | | AP32 | | |
| 5 | IO_L09P_5 | | AR32 | | |
| 5 | IO_L08N_5 | | AW33 | | |
| 5 | IO_L08P_5 | | AV33 | | |
| 5 | IO_L07N_5/VREF_5 | | AT33 | | |
| 5 | IO_L07P_5 | | AU33 | | |
| 5 | IO_L06N_5/VRP_5 | | AP33 | | |
| 5 | IO_L06P_5/VRN_5 | | AR33 | | |
| 5 | IO_L05_5/No_Pair | | AN32 | | |
| 5 | IO_L03N_5/D4 | | AW34 | | |
| 5 | IO_L03P_5/D5 | | AY34 | | |
| 5 | IO_L02N_5/D6 | | AV34 | | |
| 5 | IO_L02P_5/D7 | | AU34 | | |
| 5 | IO_L01N_5/RDWR_B | | AR34 | | |
| 5 | IO_L01P_5/CS_B | | AT34 | | |
| | | | | | |
| 6 | IO_L01P_6/VRN_6 | | AW37 | | |
| 6 | IO_L01N_6/VRP_6 | | AV37 | | |
| 6 | IO_L02P_6 | | AW36 | | |
| 6 | IO_L02N_6 | | AV36 | | |
| 6 | IO_L03P_6 | | AY37 | | |
| 6 | IO_L03N_6/VREF_6 | | AY38 | | |
| 6 | IO_L04P_6 | | AU36 | | |
| 6 | IO_L04N_6 | | AT37 | | |
| 6 | IO_L05P_6 | | AU35 | | |
| 6 | IO_L05N_6 | | AT35 | | |
| 6 | IO_L06P_6 | | AW41 | | |
| 6 | IO_L06N_6 | | AW42 | | |
| 6 | IO_L73P_6 | | AV41 | | |
| 6 | IO_L73N_6 | | AV42 | | |
| 6 | IO_L74P_6 | | AW40 | | |
| 6 | IO_L74N_6 | | AV40 | | |
| 6 | IO_L75P_6 | | AU39 | | |
| 6 | IO_L75N_6/VREF_6 | | AU40 | | |
| 6 | IO_L76P_6 | | AU41 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 1 | IO_L57P_1 | E19 | |
| 1 | IO_L56N_1 | K18 | |
| 1 | IO_L56P_1 | J18 | |
| 1 | IO_L55N_1 | H19 | |
| 1 | IO_L55P_1 | H20 | |
| 1 | IO_L54N_1 | B18 | |
| 1 | IO_L54P_1 | A18 | |
| 1 | IO_L53_1/No_Pair | L18 | |
| 1 | IO_L50_1/No_Pair | L19 | |
| 1 | IO_L49N_1 | C18 | |
| 1 | IO_L49P_1 | C19 | |
| 1 | IO_L48N_1 | F18 | |
| 1 | IO_L48P_1 | E18 | |
| 1 | IO_L47N_1 | L17 | |
| 1 | IO_L47P_1 | K17 | |
| 1 | IO_L46N_1 | G18 | |
| 1 | IO_L46P_1 | G19 | |
| 1 | IO_L18N_1/VREF_1 | C17 | NC |
| 1 | IO_L18P_1 | B17 | NC |
| 1 | IO_L12N_1 | G17 | NC |
| 1 | IO_L12P_1 | F17 | NC |
| 1 | IO_L11N_1 | M17 | NC |
| 1 | IO_L11P_1 | M18 | NC |
| 1 | IO_L10N_1 | B16 | NC |
| 1 | IO_L10P_1 | A16 | NC |
| 1 | IO_L45N_1/VREF_1 | D16 | |
| 1 | IO_L45P_1 | D17 | |
| 1 | IO_L44N_1 | K16 | |
| 1 | IO_L44P_1 | J16 | |
| 1 | IO_L43N_1 | F16 | |
| 1 | IO_L43P_1 | E16 | |
| 1 | IO_L39N_1 | H16 | |
| 1 | IO_L39P_1 | H17 | |
| 1 | IO_L38N_1 | M16 | |
| 1 | IO_L38P_1 | L16 | |
| 1 | IO_L37N_1 | B15 | |
| 1 | IO_L37P_1 | A15 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 1 | IO_L21P_1 | H13 | |
| 1 | IO_L20N_1 | L12 | |
| 1 | IO_L20P_1 | K12 | |
| 1 | IO_L19N_1 | B11 | |
| 1 | IO_L19P_1 | A11 | |
| 1 | IO_L09N_1/VREF_1 | E11 | |
| 1 | IO_L09P_1 | D11 | |
| 1 | IO_L08N_1 | J11 | |
| 1 | IO_L08P_1 | H11 | |
| 1 | IO_L07N_1 | G11 | |
| 1 | IO_L07P_1 | F11 | |
| 1 | IO_L06N_1 | B10 | |
| 1 | IO_L06P_1 | A10 | |
| 1 | IO_L05_1/No_Pair | G10 | |
| 1 | IO_L03N_1/VREF_1 | C10 | |
| 1 | IO_L03P_1 | C11 | |
| 1 | IO_L02N_1 | L11 | |
| 1 | IO_L02P_1 | K11 | |
| 1 | IO_L01N_1/VRP_1 | F10 | |
| 1 | IO_L01P_1/VRN_1 | E10 | |
| | | | |
| 2 | IO_L01N_2/VRP_2 | B8 | |
| 2 | IO_L01P_2/VRN_2 | A8 | |
| 2 | IO_L02N_2 | C9 | |
| 2 | IO_L02P_2 | B9 | |
| 2 | IO_L03N_2 | B7 | |
| 2 | IO_L03P_2 | A7 | |
| 2 | IO_L04N_2/VREF_2 | B6 | |
| 2 | IO_L04P_2 | A6 | |
| 2 | IO_L05N_2 | D8 | |
| 2 | IO_L05P_2 | D9 | |
| 2 | IO_L06N_2 | B4 | |
| 2 | IO_L06P_2 | A4 | |
| 2 | IO_L73N_2 | C7 | |
| 2 | IO_L73P_2 | C8 | |
| 2 | IO_L74N_2 | G9 | |
| 2 | IO_L74P_2 | F9 | |