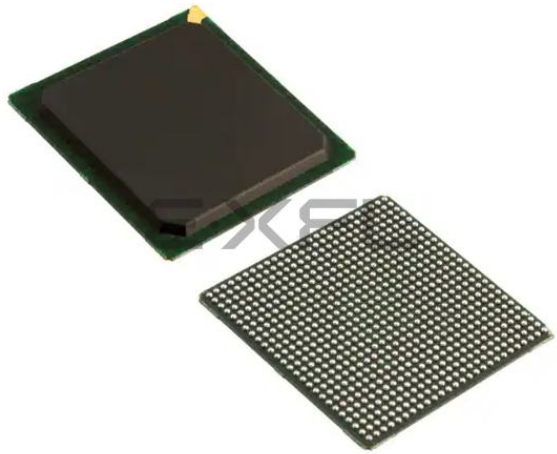

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Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-5fgg676c

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Virtex-II Pro X			Virtex-II Pro			Units
		Min	Typ	Max	Min	Typ	Max	
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	1.25			1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			2.0			V
I_{REF}	V_{REF} current per pin			10			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10			10	µA
C_{IN}	Input capacitance (sample-tested)			10			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)			150			150	µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample-tested)			150			150	µA
I_{BATT} (1)	Battery supply current	Note (2)			Note (2)			nA
$I_{CCAUXTX}$	Operating AVCCAUXTX supply current		115			60	105	mA
$I_{CCAUXRX}$	Operating AVCCAUXRX supply current		85			35	75	mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC-coupled		55			30		mA
	Operating I_{TTX} supply current when transmitter is DC-coupled	N/A	N/A	N/A		15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC-coupled		15			0		mA
	Operating I_{TRX} supply current when receiver is DC-coupled	N/A	N/A	N/A		15		
P_{CPU}	Power dissipation of PowerPC™ 405 processor block		0.9			0.9		mW/ MHz
P_{RXTX} (3)	Power dissipation of MGT @ 1.25 Gb/s per channel	N/A	N/A	N/A		230		mW
	Power dissipation of MGT @ 2.5 Gb/s per channel		290			310		mW
	Power dissipation of MGT @ 3.125 Gb/s per channel		310			350		mW
	Power dissipation of MGT @ 4.25 Gb/s per channel		450		N/A	N/A	N/A	mW
	Power dissipation of MGT @ 6.25 Gb/s per channel		525		N/A	N/A	N/A	mW

Notes:

1. Characterized, not tested.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

3. Total dissipation of fully operational PMA and PCS combined. This power is the average power supply dissipation per MGT. The averaging was done by simultaneously turning on all eight transceivers and dividing the total power supply dissipation by eight.

SelectIO-Ultra DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, max	V, min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	24	–24
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.2	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI66_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCIX	–0.2	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)
GTLP	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.2	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL_I	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	8(2)	–8(2)
HSTL_II	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	16(2)	–16(2)
HSTL_III	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	24(2)	–8(2)
HSTL_IV	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	48(2)	–8(2)
SSTL2_I	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	6.7	–6.7
SSTL18_II	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		440	600	780	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

Table 31: **RocketIO X RXUSRCLK2 Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
RXDEC64B66BUSE RXDEC8B10BUSE control input	$T_{GCCK\_}RDEC/T_{GCCK\_}RDEC$				ns, min
RXDESCRAM64B66BUSE control input	$T_{GCCK\_}RDES/T_{GCCK\_}RDES$				ns, min
RXINTDATAWIDTH control input	$T_{GCCK\_}RIDATW/T_{GCCK\_}RIDATW$				ns, min
RXSLIDE control input	$T_{GCCK\_}RXSLIDE/T_{GCCK\_}RXSLIDE$				ns, min
Clock to Out					
PMARXLOCK status output	$T_{GCKST\_}PLCK$				ns, max
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$				ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$				ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$				ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$				ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$				ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$				ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$				ns, max
RXBUFSTATUS status outputs	$T_{GCKST\_}RBSTA$				ns, max
CHBONDDONE status output	$T_{GCKST\_}CHBD$				ns, max
RXCHARISK status outputs	$T_{GCKST\_}RKCH$				ns, max
RXRUNDISP status outputs	$T_{GCKST\_}RRDIS$				ns, max
RXDATA data outputs	$T_{GCKDO\_}RDAT$				ns, max
Clock					
RXUSRCLK2 minimum pulse width, High	T_{RX2PWH}				ns, min
RXUSRCLK2 minimum pulse width, Low	T_{RX2PWL}				ns, min

Table 32: **RocketIO RXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK2)					
RXRESET control input	$T_{GCCK\_}RRST/T_{GCKC\_}RRST$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
RXPOLARITY control input	$T_{GCCK\_}RPOL/T_{GCKC\_}RPOL$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
ENCHANSYNC control input	$T_{GCCK\_}ECSY/T_{GCKC\_}ECSY$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
Clock to Out					
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$	0.50	0.50	0.55	ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$	0.50	0.50	0.55	ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$	0.50	0.50	0.55	ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$	0.41	0.41	0.46	ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$	0.41	0.41	0.46	ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$	0.50	0.50	0.55	ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$	0.41	0.41	0.46	ns, max

Clock Distribution Switching Characteristics

Table 41: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Global Clock Buffer I input to O output	T_{GIO}	0.05	0.057	0.064	ns, max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.49/–0.10	0.54/–0.12	0.60/–0.13	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 34 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 42: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.28	0.32	0.36	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.59	0.65	0.73	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.63	0.70	0.79	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.29	0.32	0.36	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}	0.29	0.32	0.36	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}	0.29	0.32	0.36	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.11	0.13	0.14	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.23	0.24	0.27	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.37	0.38	0.42	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.57	0.64	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.21/–0.04	0.24/–0.05	0.27/–0.06	ns, min
DY inputs	T_{DYCK}/T_{CKDY}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
DX inputs	T_{DXCK}/T_{CKDX}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
CE input	T_{CECK}/T_{CKCE}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}	0.55/–0.01	0.60/–0.01	0.78/–0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.37	0.40	0.45	ns, min
Minimum Pulse Width, Low	T_{CL}	0.37	0.40	0.45	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.09	1.25	1.40	ns, max
Toggle Frequency (for export control)	F_{TOG}	1350	1200	1050	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Virtex-II Pro Pin Definitions

This section describes the pinouts for Virtex-II Pro devices in the following packages:

- FG256/FGG256, FG456/FGG456, and FG676/FGG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF672, FF896, FF1148, FF1152, FF1517, FF1696, and FF1704: flip-chip fine-pitch BGA of 1.00 mm pitch

All of the devices supported in a particular package are pin-out-compatible and are listed in the same table (one table per package). Pins that are not available for smaller devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards. Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

All Virtex-II Pro pinout tables are available on the distribution CD-ROM, or on the web (at http://www.xilinx.com).

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II Pro pinout tables.

Table 4: **Virtex-II Pro Pin Definitions**

Pin Name	Direction	Description
User I/O Pins:		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins:		
IO_LXXY_#/ZZZ	The *dual-function pins* are labelled "**IO_LXXY_#/ZZZ**", where "**ZZZ**" can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B** These dual functions are defined in the following section:	
"ZZZ" (Dual Function) Definitions:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In SelectMAP mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In SelectMAP mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. These pins can be used to clock the RocketIO transceiver. See the **RocketIO Transceiver User Guide** for design guidelines and BREFCLK-specific pins, by device.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins:(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection. Pin is biased by V_{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used. The mode pins are not to be toggled (changed) while in operation during and after configuration.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock. This pin is 3.3V compatible.
TDI	Input	Boundary Scan Data Input. This pin is 3.3V compatible.
TDO	Output (open-drain)	Boundary Scan Data Output. Pin is open-drain and can be pulled up to 3.3V. It is recommended that the external pull-up be greater than 200Ω. There is no internal pull-up.
TMS	Input	Boundary Scan Mode Select. This pin is 3.3V compatible.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins:		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Connect to V_{CCAUX} or GND if battery not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the RocketIO MGT (2.5V).
AVCCAUXTX#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (2.5V).
BREFCLKN, BREFCLKP(2)	Input	Differential clock input that clocks the RocketIO X MGTs populating the same side of the chip (top or bottom). Can also drive DCMs for RocketIO X MGT use.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
1	IO_L45N_1/VREF_1	C18			
1	IO_L45P_1	D18			
1	IO_L43N_1	E18			
1	IO_L43P_1	F18			
1	IO_L39N_1	G18			
1	IO_L39P_1	H18			
1	IO_L37N_1	A19			
1	IO_L37P_1	B19			
1	IO_L09N_1/VREF_1	E19			
1	IO_L09P_1	F19			
1	IO_L07N_1	G19			
1	IO_L07P_1	H19			
1	IO_L06N_1	C20			
1	IO_L06P_1	D20			
1	IO_L05_1/No_Pair	E20			
1	IO_L03N_1/VREF_1	F20			
1	IO_L03P_1	G20			
1	IO_L02N_1	D21			
1	IO_L02P_1	E21			
1	IO_L01N_1/VRP_1	D22			
1	IO_L01P_1/VRN_1	E22			
2	IO_L01N_2/VRP_2	C25			
2	IO_L01P_2/VRN_2	C26			
2	IO_L02N_2	D25			
2	IO_L02P_2	D26			
2	IO_L03N_2	E23			
2	IO_L03P_2	F22			
2	IO_L04N_2/VREF_2	E25			
2	IO_L04P_2	E26			
2	IO_L06N_2	F21			
2	IO_L06P_2	G21			
2	IO_L24N_2	F23	NC		
2	IO_L24P_2	F24	NC		
2	IO_L31N_2	F25			

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E29				
0	IO_L01P_0/VRN_0	E28				
0	IO_L02N_0	H26				
0	IO_L02P_0	G26				
0	IO_L03N_0	H25				
0	IO_L03P_0/VREF_0	G25				
0	IO_L05_0/No_Pair	J25				
0	IO_L06N_0	K24				
0	IO_L06P_0	J24				
0	IO_L07N_0	F26				
0	IO_L07P_0	E26				
0	IO_L08N_0	D30				
0	IO_L08P_0	D29				
0	IO_L09N_0	K23				
0	IO_L09P_0/VREF_0	J23				
0	IO_L19N_0	F24	NC	NC		
0	IO_L19P_0	E24	NC	NC		
0	IO_L20N_0	D28	NC	NC		
0	IO_L20P_0	C28	NC	NC		
0	IO_L21N_0	H24	NC	NC		
0	IO_L21P_0	G24	NC	NC		
0	IO_L25N_0	G23	NC	NC		
0	IO_L25P_0	F23	NC	NC		
0	IO_L26N_0	E27	NC	NC		
0	IO_L26P_0	D27	NC	NC		
0	IO_L27N_0	K22	NC	NC		
0	IO_L27P_0/VREF_0	J22	NC	NC		
0	IO_L37N_0	H22				
0	IO_L37P_0	G22				
0	IO_L38N_0	D26				
0	IO_L38P_0	C26				
0	IO_L39N_0	K21				
0	IO_L39P_0	J21				
0	IO_L43N_0	F22				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
5	IO_L44N_5	AK22				
5	IO_L44P_5	AJ22				
5	IO_L43N_5	AF21				
5	IO_L43P_5	AE21				
5	IO_L39N_5	AK24				
5	IO_L39P_5	AJ24				
5	IO_L38N_5	AH22				
5	IO_L38P_5	AG22				
5	IO_L37N_5	AF22				
5	IO_L37P_5	AE22				
5	IO_L27N_5/VREF_5	AL25	NC	NC		
5	IO_L27P_5	AK25	NC	NC		
5	IO_L26N_5	AJ23	NC	NC		
5	IO_L26P_5	AH23	NC	NC		
5	IO_L25N_5	AH24	NC	NC		
5	IO_L25P_5	AG24	NC	NC		
5	IO_L21N_5	AM26	NC	NC		
5	IO_L21P_5	AL26	NC	NC		
5	IO_L20N_5	AK26	NC	NC		
5	IO_L20P_5	AJ26	NC	NC		
5	IO_L19N_5	AF23	NC	NC		
5	IO_L19P_5	AE23	NC	NC		
5	IO_L09N_5/VREF_5	AL27				
5	IO_L09P_5	AK27				
5	IO_L08N_5	AH25				
5	IO_L08P_5	AG25				
5	IO_L07N_5/VREF_5	AF24				
5	IO_L07P_5	AE24				
5	IO_L06N_5/VRP_5	AM28				
5	IO_L06P_5/VRN_5	AL28				
5	IO_L05_5/No_Pair	AF25				
5	IO_L03N_5/D4	AK28				
5	IO_L03P_5/D5	AK29				
5	IO_L02N_5/D6	AH26				
5	IO_L02P_5/D7	AG26				
5	IO_L01N_5/RDWR_B	AL29				
5	IO_L01P_5/CS_B	AL30				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L40P_2	K3		
2	IO_L41N_2	R9		
2	IO_L41P_2	P9		
2	IO_L42N_2	K1		
2	IO_L42P_2	K2		
2	IO_L43N_2	L5		
2	IO_L43P_2	L6		
2	IO_L44N_2	P7		
2	IO_L44P_2	P8		
2	IO_L45N_2	L1		
2	IO_L45P_2	L2		
2	IO_L46N_2/VREF_2	M5		
2	IO_L46P_2	M6		
2	IO_L47N_2	R10		
2	IO_L47P_2	R11		
2	IO_L48N_2	M3		
2	IO_L48P_2	M4		
2	IO_L49N_2	M1		
2	IO_L49P_2	M2		
2	IO_L50N_2	R7		
2	IO_L50P_2	T8		
2	IO_L51N_2	P4		
2	IO_L51P_2	N4		
2	IO_L52N_2/VREF_2	N2		
2	IO_L52P_2	N3		
2	IO_L53N_2	T10		
2	IO_L53P_2	T11		
2	IO_L54N_2	P5		
2	IO_L54P_2	P6		
2	IO_L55N_2	R3		
2	IO_L55P_2	P3		
2	IO_L56N_2	T6		
2	IO_L56P_2	T7		
2	IO_L57N_2	P1		
2	IO_L57P_2	P2		
2	IO_L58N_2/VREF_2	R5		
2	IO_L58P_2	R6		
2	IO_L59N_2	U10		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L55N_3	Y1		
3	IO_L55P_3	Y2		
3	IO_L54N_3	AA5		
3	IO_L54P_3	AA6		
3	IO_L53N_3	Y10		
3	IO_L53P_3	Y11		
3	IO_L52N_3	AA4		
3	IO_L52P_3	AB4		
3	IO_L51N_3/VREF_3	AA1		
3	IO_L51P_3	AA2		
3	IO_L50N_3	Y9		
3	IO_L50P_3	AA9		
3	IO_L49N_3	AB6		
3	IO_L49P_3	AB7		
3	IO_L48N_3	AB2		
3	IO_L48P_3	AB3		
3	IO_L47N_3	AA10		
3	IO_L47P_3	AA11		
3	IO_L46N_3	AC5		
3	IO_L46P_3	AC6		
3	IO_L45N_3/VREF_3	AC3		
3	IO_L45P_3	AC4		
3	IO_L44N_3	AA7		
3	IO_L44P_3	AA8		
3	IO_L43N_3	AC1		
3	IO_L43P_3	AC2		
3	IO_L42N_3	AD5		
3	IO_L42P_3	AD6		
3	IO_L41N_3	AB10		
3	IO_L41P_3	AB11		
3	IO_L40N_3	AD3		
3	IO_L40P_3	AE3		
3	IO_L39N_3/VREF_3	AD1		
3	IO_L39P_3	AD2		
3	IO_L38N_3	AB8		
3	IO_L38P_3	AC7		
3	IO_L37N_3	AE5		
3	IO_L37P_3	AE6		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	AVCCAUXTX6	B23		
N/A	VTTXPAD6	B24		
N/A	TXNPAD6	A24		
N/A	TXPPAD6	A23		
N/A	GNDA6	C24		
N/A	RXPPAD6	A22		
N/A	RXNPAD6	A21		
N/A	VTRXPAD6	B22		
N/A	AVCCAUXRX6	B21		
N/A	AVCCAUXTX7	B18		
N/A	VTTXPAD7	B19		
N/A	TXNPAD7	A19		
N/A	TXPPAD7	A18		
N/A	GNDA7	C16		
N/A	RXPPAD7	A17		
N/A	RXNPAD7	A16		
N/A	VTRXPAD7	B17		
N/A	AVCCAUXRX7	B16		
N/A	AVCCAUXTX8	B14		
N/A	VTTXPAD8	B15		
N/A	TXNPAD8	A15		
N/A	TXPPAD8	A14		
N/A	GNDA8	C13		
N/A	RXPPAD8	A13		
N/A	RXNPAD8	A12		
N/A	VTRXPAD8	B13		
N/A	AVCCAUXRX8	B12		
N/A	AVCCAUXTX9	B10		
N/A	VTTXPAD9	B11		
N/A	TXNPAD9	A11		
N/A	TXPPAD9	A10		
N/A	GNDA9	C9		
N/A	RXPPAD9	A9		
N/A	RXNPAD9	A8		
N/A	VTRXPAD9	B9		
N/A	AVCCAUXRX9	B8		
N/A	AVCCAUXTX11	B6		
N/A	VTTXPAD11	B7		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GNDA18	AU16		
N/A	TXPPAD18	AW18		
N/A	TXNPAD18	AW19		
N/A	VTTXPAD18	AV19		
N/A	AVCCAUXTX18	AV18		
N/A	AVCCAUXRX19	AV21		
N/A	VTRXPAD19	AV22		
N/A	RXNPAD19	AW21		
N/A	RXPPAD19	AW22		
N/A	GNDA19	AU24		
N/A	TXPPAD19	AW23		
N/A	TXNPAD19	AW24		
N/A	VTTXPAD19	AV24		
N/A	AVCCAUXTX19	AV23		
N/A	AVCCAUXRX20	AV25		
N/A	VTRXPAD20	AV26		
N/A	RXNPAD20	AW25		
N/A	RXPPAD20	AW26		
N/A	GNDA20	AU27		
N/A	TXPPAD20	AW27		
N/A	TXNPAD20	AW28		
N/A	VTTXPAD20	AV28		
N/A	AVCCAUXTX20	AV27		
N/A	AVCCAUXRX21	AV29		
N/A	VTRXPAD21	AV30		
N/A	RXNPAD21	AW29		
N/A	RXPPAD21	AW30		
N/A	GNDA21	AU31		
N/A	TXPPAD21	AW31		
N/A	TXNPAD21	AW32		
N/A	VTTXPAD21	AV32		
N/A	AVCCAUXTX21	AV31		
N/A	AVCCAUXRX23	AV33		
N/A	VTRXPAD23	AV34		
N/A	RXNPAD23	AW33		
N/A	RXPPAD23	AW34		
N/A	GNDA23	AU34		
N/A	TXPPAD23	AW35		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L37N_5		AU28		
5	IO_L37P_5		AV28		
5	IO_L87N_5/VREF_5		AP28	NC	
5	IO_L87P_5		AR28	NC	
5	IO_L86N_5		AN28	NC	
5	IO_L86P_5		AM28	NC	
5	IO_L85N_5		AV29	NC	
5	IO_L85P_5		AW29	NC	
5	IO_L84N_5		AT29	NC	
5	IO_L84P_5		AU29	NC	
5	IO_L83_5/No_Pair		AR29	NC	
5	IO_L78N_5		AM29	NC	
5	IO_L78P_5		AN29	NC	
5	IO_L36N_5/VREF_5		AL29		
5	IO_L36P_5		AL28		
5	IO_L35N_5		AY30		
5	IO_L35P_5		AW30		
5	IO_L34N_5		AU30		
5	IO_L34P_5		AV30		
5	IO_L30N_5		AR30		
5	IO_L30P_5		AT30		
5	IO_L29N_5		AN30		
5	IO_L29P_5		AP30		
5	IO_L28N_5		AL30		
5	IO_L28P_5		AM30		
5	IO_L27N_5/VREF_5		AV31		
5	IO_L27P_5		AW31		
5	IO_L26N_5		AU31		
5	IO_L26P_5		AT31		
5	IO_L25N_5		AP31		
5	IO_L25P_5		AR31		
5	IO_L21N_5		AM31		
5	IO_L21P_5		AN31		
5	IO_L20N_5		AY32		
5	IO_L20P_5		AY33		
5	IO_L19N_5		AU32		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	VCCO_3		AD14		
3	VCCO_3		AC15		
3	VCCO_3		AC14		
3	VCCO_3		AC8		
3	VCCO_3		AC5		
3	VCCO_3		AB15		
3	VCCO_3		AB14		
4	VCCO_4		AW18		
4	VCCO_4		AT20		
4	VCCO_4		AT15		
4	VCCO_4		AT11		
4	VCCO_4		AP18		
4	VCCO_4		AP14		
4	VCCO_4		AJ21		
4	VCCO_4		AJ20		
4	VCCO_4		AJ19		
4	VCCO_4		AJ18		
4	VCCO_4		AJ17		
4	VCCO_4		AH21		
4	VCCO_4		AH20		
4	VCCO_4		AH19		
4	VCCO_4		AH18		
5	VCCO_5		AW25		
5	VCCO_5		AT32		
5	VCCO_5		AT28		
5	VCCO_5		AT23		
5	VCCO_5		AP29		
5	VCCO_5		AP25		
5	VCCO_5		AJ26		
5	VCCO_5		AJ25		
5	VCCO_5		AJ24		
5	VCCO_5		AJ23		
5	VCCO_5		AJ22		
5	VCCO_5		AH25		
5	VCCO_5		AH24		
5	VCCO_5		AH23		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCINT		U26		
N/A	VCCINT		U17		
N/A	VCCINT		U16		
N/A	VCCINT		T27		
N/A	VCCINT		T26		
N/A	VCCINT		T25		
N/A	VCCINT		T24		
N/A	VCCINT		T23		
N/A	VCCINT		T22		
N/A	VCCINT		T21		
N/A	VCCINT		T20		
N/A	VCCINT		T19		
N/A	VCCINT		T18		
N/A	VCCINT		T17		
N/A	VCCINT		T16		
N/A	VCCINT		R28		
N/A	VCCINT		R27		
N/A	VCCINT		R26		
N/A	VCCINT		R17		
N/A	VCCINT		R16		
N/A	VCCINT		R15		
N/A	VCCINT		P29		
N/A	VCCINT		P28		
N/A	VCCINT		P27		
N/A	VCCINT		P16		
N/A	VCCINT		P15		
N/A	VCCINT		P14		
N/A	VCCINT		N30		
N/A	VCCINT		N13		
N/A	VCCAUX		AB42		
N/A	VCCAUX		AB41		
N/A	VCCAUX		AB2		
N/A	VCCAUX		AB1		
N/A	VCCAUX		AC42		
N/A	VCCAUX		AC1		
N/A	VCCAUX		AM32		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L79P_7	D41	
7	IO_L79N_7	D42	
7	IO_L78P_7	C39	
7	IO_L78N_7	C40	
7	IO_L77P_7	H34	
7	IO_L77N_7	H35	
7	IO_L76P_7	C37	
7	IO_L76N_7/VREF_7	D36	
7	IO_L75P_7	B38	
7	IO_L75N_7	C38	
7	IO_L74P_7	F34	
7	IO_L74N_7	G34	
7	IO_L73P_7	C35	
7	IO_L73N_7	C36	
7	IO_L06P_7	A39	
7	IO_L06N_7	B39	
7	IO_L05P_7	D34	
7	IO_L05N_7	D35	
7	IO_L04P_7	A37	
7	IO_L04N_7/VREF_7	B37	
7	IO_L03P_7	A36	
7	IO_L03N_7	B36	
7	IO_L02P_7	B34	
7	IO_L02N_7	C34	
7	IO_L01P_7/VRN_7	A35	
7	IO_L01N_7/VRP_7	B35	
7	VCCO_7	W39	
7	VCCO_7	P39	
7	VCCO_7	K39	
7	VCCO_7	F39	
7	VCCO_7	D37	
7	VCCO_7	W35	
7	VCCO_7	P35	
7	VCCO_7	K35	
7	VCCO_7	M33	
7	VCCO_7	H33	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	VCCO_3	AF14	
3	VCCO_3	AE14	
3	VCCO_3	AD14	
3	VCCO_3	AC14	
3	VCCO_3	AB14	
3	VCCO_3	AR10	
3	VCCO_3	AL10	
3	VCCO_3	AN8	
3	VCCO_3	AJ8	
3	VCCO_3	AD8	
3	VCCO_3	AW6	
3	VCCO_3	AU4	
3	VCCO_3	AN4	
3	VCCO_3	AJ4	
3	VCCO_3	AD4	
2	VCCO_2	AA15	
2	VCCO_2	Y15	
2	VCCO_2	W15	
2	VCCO_2	V15	
2	VCCO_2	U15	
2	VCCO_2	T15	
2	VCCO_2	AA14	
2	VCCO_2	Y14	
2	VCCO_2	W14	
2	VCCO_2	V14	
2	VCCO_2	U14	
2	VCCO_2	T14	
2	VCCO_2	R14	
2	VCCO_2	M10	
2	VCCO_2	H10	
2	VCCO_2	W8	
2	VCCO_2	P8	
2	VCCO_2	K8	
2	VCCO_2	D6	
2	VCCO_2	W4	
2	VCCO_2	P4	
2	VCCO_2	K4	