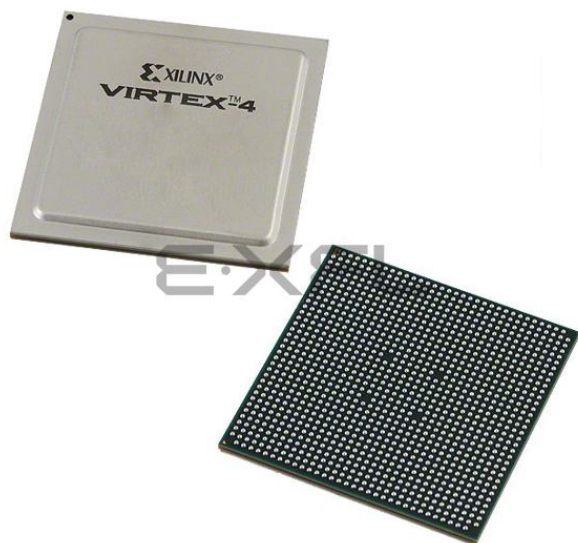




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

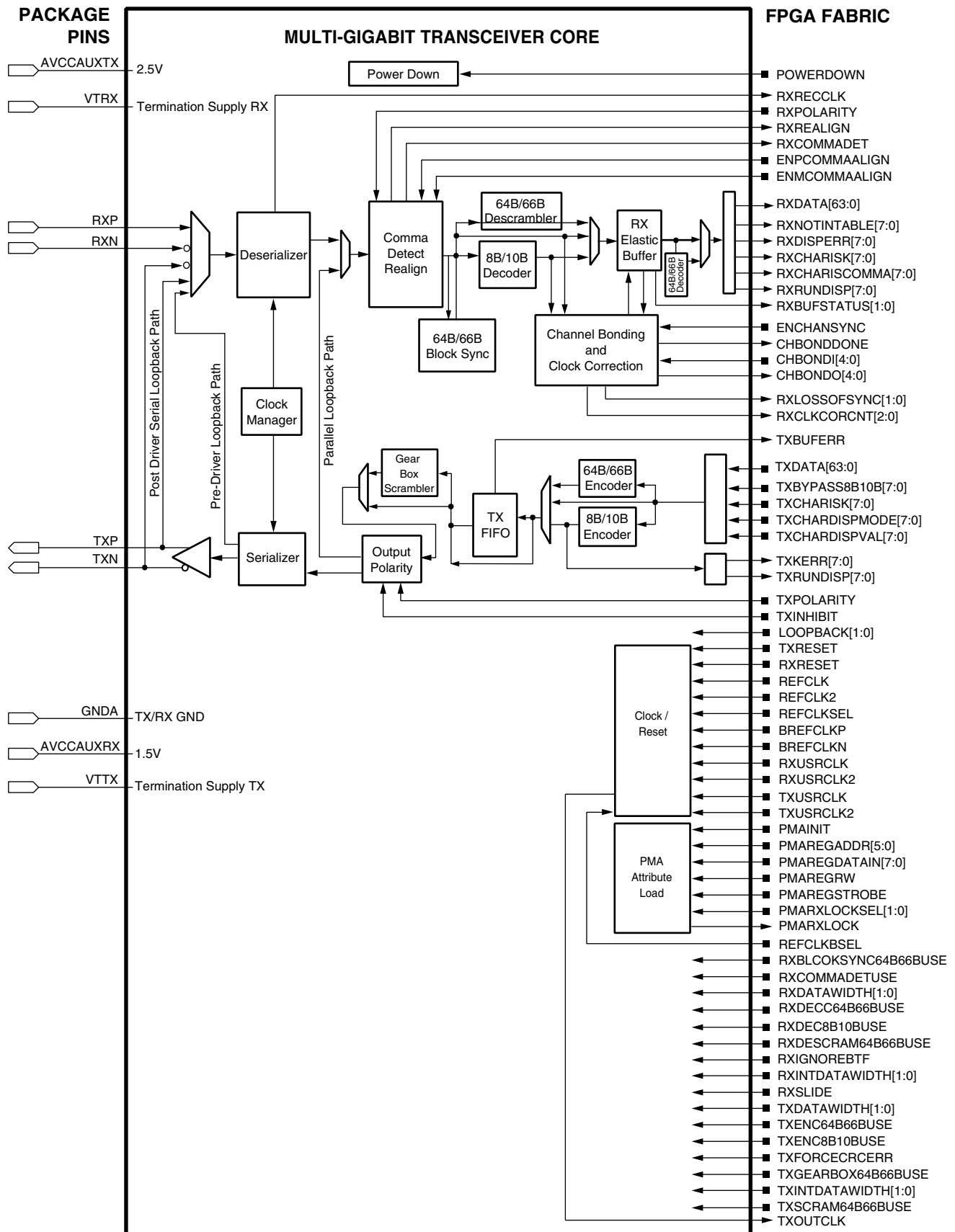
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	804
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6ff1148c



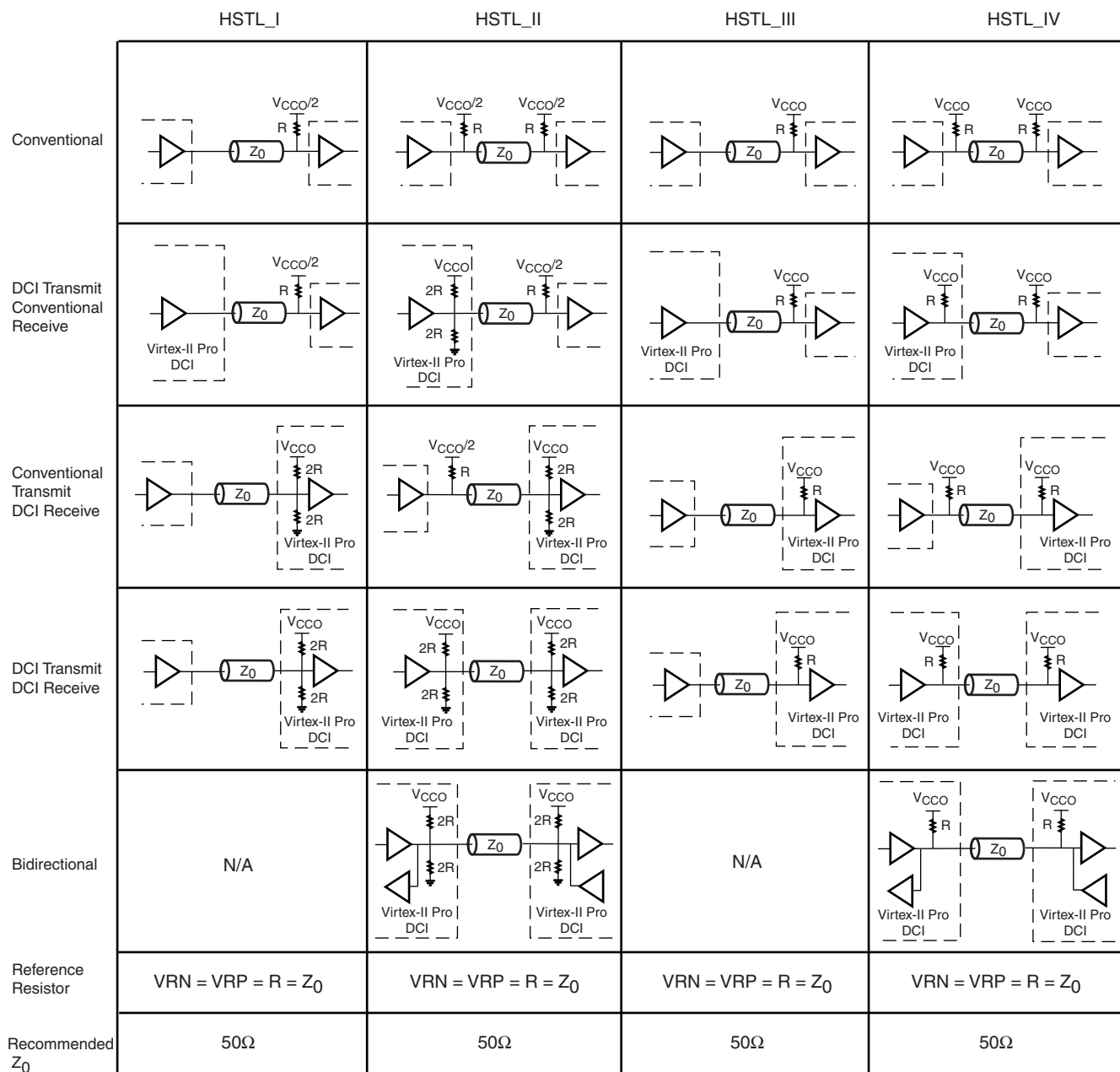
DS083-2_37_050704

Figure 4: RocketIO X Transceiver Block Diagram

Table 15: SelectIO-Ultra Differential Buffers With On-Chip Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).



DS083-2_65a_082102

Figure 28: HSTL DCI Usage Examples

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

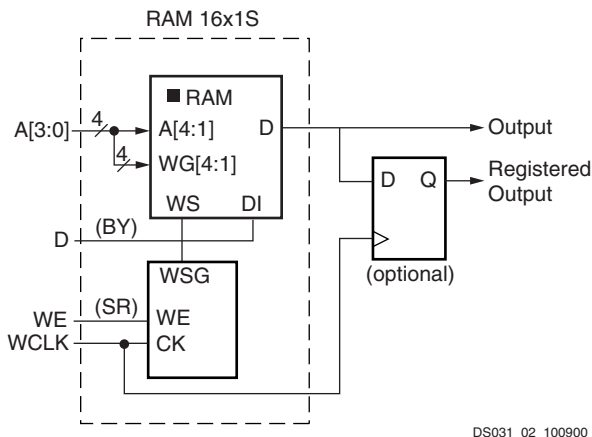


Figure 36: Distributed SelectRAM+ (RAM16x1S)

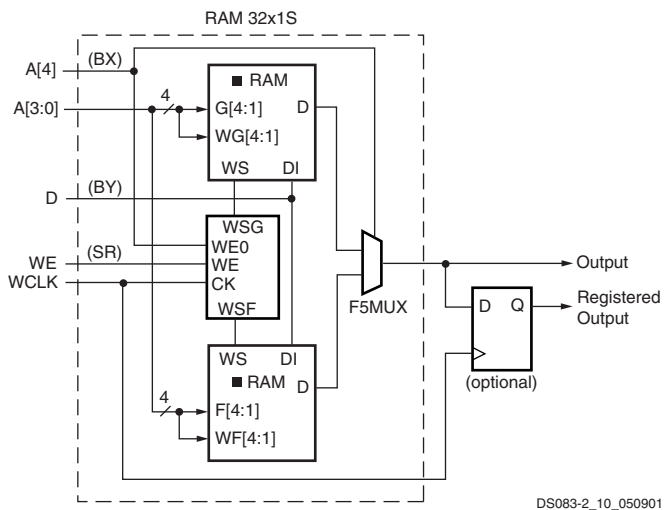


Figure 37: Single-Port Distributed SelectRAM+ (RAM32x1S)

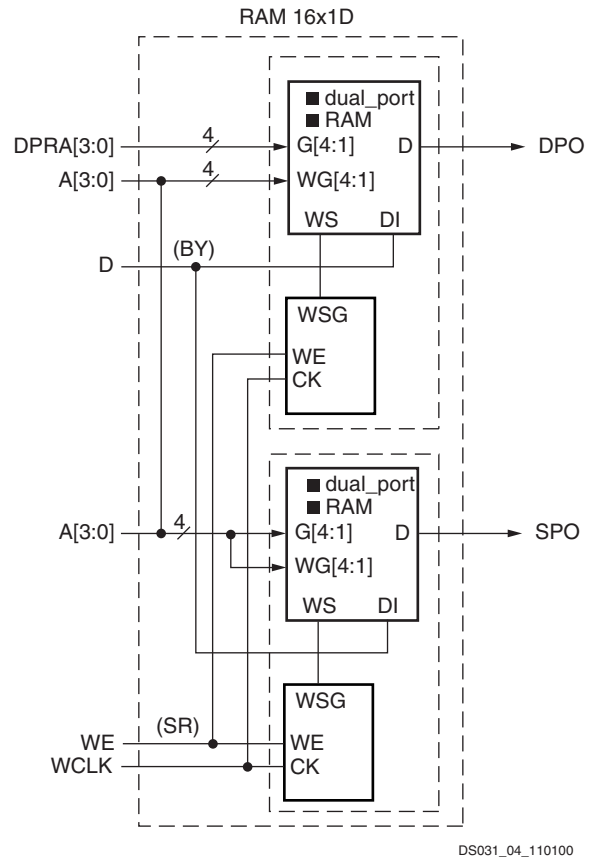


Figure 38: Dual-Port Distributed SelectRAM+ (RAM16x1D)

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

Table 17: ROM Configuration

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011

Product Specification

Virtex-II Pro⁽¹⁾ Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade

commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: Absolute Maximum Ratings

Symbol	Description ⁽¹⁾	Virtex-II Pro X	Virtex-II Pro	Units
V _{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.6		V
V _{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0		V
V _{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75		V
V _{BATT}	Key memory battery backup supply	–0.5 to 4.05		V
V _{REF}	Input reference voltage	–0.3 to 3.75		V
V _{IN}	3.3V I/O input voltage relative to GND (user and dedicated I/Os)	–0.3 to 4.05 ⁽³⁾		V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.5 to V _{CCO} + 0.5		V
V _{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)	–0.3 to 4.05 ⁽³⁾		V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.5 to V _{CCO} + 0.5		V
AVCCAUXRX	Receive auxiliary supply voltage relative to GNDA (analog ground)	–0.5 to 2.0	–0.5 to 3.0	V
AVCCAUTX	Transmit auxiliary supply voltage relative to GNDA (analog ground)	–0.5 to 3.0	–0.5 to 3.0	V
V _{TRX}	Terminal receive supply voltage relative to GND	–0.5 to 3.0	–0.5 to 3.0	V
V _{TTX}	Terminal transmit supply voltage relative to GND	–0.5 to 1.6	–0.5 to 3.0	V
T _{STG}	Storage temperature (ambient)	–65 to +150		°C
T _{SOL}	Maximum soldering temperature ⁽²⁾	All regular FG/FF flip-chip packages		+220
		Pb-free FGG256 wire-bond package		N/A
		Pb-free FGG456 and FGG676 wire-bond packages		N/A
T _J	Maximum junction temperature ⁽²⁾	+125		°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- For soldering guidelines and thermal considerations, see the [Device Packaging and Thermal Characteristics Guide](#) information on the Xilinx website.
- 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to [XAPP659](#) for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Date	Version	Revision
12/03/02	2.5	Updated parametric information in: Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from $-0.5V$ to $-0.3V$ for 3.3V. Table 2: Add footnote (2) regarding V_{CCAUX} voltage droop. Renumbered other notes. Table 12: Add waveform diagrams (Figure 1 and Figure 2) illustrating DV_{OUT} (single-ended) and DV_{PPOUT} (differential). Table 23: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct T_{RCLK} and T_{FCLK} values and unit of measurement. Table 60: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL.
01/20/03	2.6	Updated parametric information in: Table 12: Correct DV_{IN} Min (200 mV to 175 mV) and DV_{IN} Max (1000 mV to 2000 mV). Table 23: Correct T_{RCLK}/T_{FCLK} Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max T_{GJT} parameter. Table 59: Correct hyperlink in footnote (1) to point directly to Answer Record 13645. - Move clock parameters from Table 18, Table 19, Table 20, and Table 21 to Table 16.
03/24/03	2.7	- Added/updated timing parameters from speedsfile v1.76. Table 2: Delete first table footnote and renumber all others. Table 3: Add "sample-tested" to I_L. Remove "Device" column, unnecessary. Table 8: Update V_{OCM} (Typ) to 1.250V. Table 10: Update LVPECL_25 DC parameters. Table 23: Update F_{GCLK} frequency ranges. Break out T_{GJT} by operating speed. Table 27: Update F_{GTx} frequency ranges. Correct T_{DJ} to 0.17 UI, T_{RJ} to 0.18 UI. Table 39: Update V_{REF} (Typ) for HSTL Class I/II from 1.08V to 0.90V. Table 43, Table 44: Correct parameter name "CE input (WS)" to "SR input". Table 64: Break out T_{DCD_CLK0} by device type.
05/27/03	2.8	- Updated time and frequency parameters as per speedsfile v1.78. Table 3: Added values for I_{REF}, I_L, I_{RPU}, I_{RPD} - Corrected I_{CCINTQ} (Table 4) and $I_{CCINTMIN}$ (Table 5) for XC2VP20 to 600 mA. Table 4: Updated/Added Typ and Max quiescent current values for XC2VP7 and XC2VP20. Added footnote specifying parameters are for Commercial Grade parts. Table 5: Added footnote specifying parameters are for Commercial Grade parts. Table 6: Corrected V_{IH} (Max) for LVTTL and LVCMOS33 standards from 3.6V to 3.45V. Changed V_{IL} (Min) for all standards to $-0.2V$. Corrected V_{IL} (Max) for LVCMOS15 and LVCMOS18 from 20% V_{CC0} to 30% V_{CC0}. Table 10: Corrected LVPECL_25 Min and Max values for V_{IH} and V_{IL}. Added explanatory text above table. Table 13 and Table 14 (pin-pin and reg-reg performance): Changed device specified from XC2VP7FF672-6 to XC2VP20FF1152-6. Table 15: Updated to show devices XC2VP7 and XC2VP20 as Preliminary for the -6 speed grade and Production for the -5 speed grade. - Removed former Table 32, Standard Capacitive Loads. Table 52: Updated T_{TAPCK} from 4.0 ns to 5.5 ns. Table 59: Modified footnote referenced at CLKFX/CLKFX180 to point to the online Jitter Calculator. - Added Figure 6 and accompanying procedure for measuring standard adjustments.
05/27/03 (cont'd)	2.8 (cont'd)	Table 1: Footnote (2) rewritten to specify "one or more banks." Table 57: Some DCM parameters were erroneously missing from v2.8 (single-module version) due to a document compilation error. The concatenated full data sheet version was not affected. These parameters have been restored.

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VTTXPAD4	B4			
N/A	TXNPAD4	A4			
N/A	TXPPAD4	A5			
N/A	GND4	C6			
N/A	RXPPAD4	A6			
N/A	RXNPAD4	A7			
N/A	VTRXPAD4	B6			
N/A	AVCCAUXRX4	B7			
N/A	AVCCAUXTX6	B10			
N/A	VTTXPAD6	B9			
N/A	TXNPAD6	A9			
N/A	TXPPAD6	A10			
N/A	GND6	C11			
N/A	RXPPAD6	A11			
N/A	RXNPAD6	A12			
N/A	VTRXPAD6	B11			
N/A	AVCCAUXRX6	B12			
N/A	AVCCAUXTX7	B16			
N/A	VTTXPAD7	B15			
N/A	TXNPAD7	A15			
N/A	TXPPAD7	A16			
N/A	GND7	C16			
N/A	RXPPAD7	A17			
N/A	RXNPAD7	A18			
N/A	VTRXPAD7	B17			
N/A	AVCCAUXRX7	B18			
N/A	AVCCAUXTX9	B21			
N/A	VTTXPAD9	B20			
N/A	TXNPAD9	A20			
N/A	TXPPAD9	A21			
N/A	GND9	C21			
N/A	RXPPAD9	A22			
N/A	RXNPAD9	A23			
N/A	VTRXPAD9	B22			
N/A	AVCCAUXRX9	B23			

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L57P_3		Y1			
3	IO_L56N_3		U7			
3	IO_L56P_3		U8			
3	IO_L55N_3		V5			
3	IO_L55P_3		V6			
3	IO_L54N_3		Y2			
3	IO_L54P_3		AA2			
3	IO_L53N_3		V7			
3	IO_L53P_3		V8			
3	IO_L52N_3		W3			
3	IO_L52P_3		W4			
3	IO_L51N_3/VREF_3		AA1			
3	IO_L51P_3		AB1			
3	IO_L50N_3		W5			
3	IO_L50P_3		W6			
3	IO_L49N_3		Y4			
3	IO_L49P_3		Y5			
3	IO_L48N_3		AA3			
3	IO_L48P_3		AA4			
3	IO_L47N_3		W7			
3	IO_L47P_3		W8			
3	IO_L46N_3		AB3			
3	IO_L46P_3		AB4			
3	IO_L45N_3/VREF_3		AB2			
3	IO_L45P_3		AC2			
3	IO_L44N_3		AA5			
3	IO_L44P_3		AA6			
3	IO_L43N_3		AC3			
3	IO_L43P_3		AC4			
3	IO_L42N_3		AD1	NC		
3	IO_L42P_3		AD2	NC		
3	IO_L41N_3		Y7	NC		
3	IO_L41P_3		Y8	NC		
3	IO_L40N_3		AB5	NC		
3	IO_L40P_3		AB6	NC		
3	IO_L39N_3/VREF_3		AE1	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
5	IO_L48N_5		AH20	NC		
5	IO_L48P_5		AH21	NC		
5	IO_L47N_5		AE19	NC		
5	IO_L47P_5		AE20	NC		
5	IO_L46N_5		AD18	NC		
5	IO_L46P_5		AC18	NC		
5	IO_L45N_5/VREF_5		AJ22			
5	IO_L45P_5		AH22			
5	IO_L44N_5		AE21			
5	IO_L44P_5		AE22			
5	IO_L43N_5		AD19			
5	IO_L43P_5		AC19			
5	IO_L39N_5		AG21			
5	IO_L39P_5		AF21			
5	IO_L38N_5		AF22			
5	IO_L38P_5		AF23			
5	IO_L37N_5		AD20			
5	IO_L37P_5		AC20			
5	IO_L09N_5/VREF_5		AK23			
5	IO_L09P_5		AJ23			
5	IO_L08N_5		AE23			
5	IO_L08P_5		AE24			
5	IO_L07N_5/VREF_5		AD21			
5	IO_L07P_5		AC21			
5	IO_L06N_5/VRP_5		AH23			
5	IO_L06P_5/VRN_5		AG23			
5	IO_L05_5/No_Pair		AD23			
5	IO_L03N_5/D4		AH24			
5	IO_L03P_5/D5		AG24			
5	IO_L02N_5/D6		AD22			
5	IO_L02P_5/D7		AC22			
5	IO_L01N_5/RDWR_B		AF24			
5	IO_L01P_5/CS_B		AG25			
6	IO_L01P_6/VRN_6		AK28			
6	IO_L01N_6/VRP_6		AJ28			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
5	IO_L44N_5	AK22				
5	IO_L44P_5	AJ22				
5	IO_L43N_5	AF21				
5	IO_L43P_5	AE21				
5	IO_L39N_5	AK24				
5	IO_L39P_5	AJ24				
5	IO_L38N_5	AH22				
5	IO_L38P_5	AG22				
5	IO_L37N_5	AF22				
5	IO_L37P_5	AE22				
5	IO_L27N_5/VREF_5	AL25	NC	NC		
5	IO_L27P_5	AK25	NC	NC		
5	IO_L26N_5	AJ23	NC	NC		
5	IO_L26P_5	AH23	NC	NC		
5	IO_L25N_5	AH24	NC	NC		
5	IO_L25P_5	AG24	NC	NC		
5	IO_L21N_5	AM26	NC	NC		
5	IO_L21P_5	AL26	NC	NC		
5	IO_L20N_5	AK26	NC	NC		
5	IO_L20P_5	AJ26	NC	NC		
5	IO_L19N_5	AF23	NC	NC		
5	IO_L19P_5	AE23	NC	NC		
5	IO_L09N_5/VREF_5	AL27				
5	IO_L09P_5	AK27				
5	IO_L08N_5	AH25				
5	IO_L08P_5	AG25				
5	IO_L07N_5/VREF_5	AF24				
5	IO_L07P_5	AE24				
5	IO_L06N_5/VRP_5	AM28				
5	IO_L06P_5/VRN_5	AL28				
5	IO_L05_5/No_Pair	AF25				
5	IO_L03N_5/D4	AK28				
5	IO_L03P_5/D5	AK29				
5	IO_L02N_5/D6	AH26				
5	IO_L02P_5/D7	AG26				
5	IO_L01N_5/RDWR_B	AL29				
5	IO_L01P_5/CS_B	AL30				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	VCCO_1	L15				
1	VCCO_1	M13				
1	VCCO_1	M14				
1	VCCO_1	M15				
1	VCCO_1	M16				
1	VCCO_1	M17				
2	VCCO_2	F3				
2	VCCO_2	K6				
2	VCCO_2	M11				
2	VCCO_2	N11				
2	VCCO_2	N12				
2	VCCO_2	P11				
2	VCCO_2	P12				
2	VCCO_2	R5				
2	VCCO_2	R11				
2	VCCO_2	R12				
2	VCCO_2	T12				
2	VCCO_2	U12				
3	VCCO_3	V12				
3	VCCO_3	W12				
3	VCCO_3	Y5				
3	VCCO_3	Y11				
3	VCCO_3	Y12				
3	VCCO_3	AA11				
3	VCCO_3	AA12				
3	VCCO_3	AB11				
3	VCCO_3	AB12				
3	VCCO_3	AC11				
3	VCCO_3	AE6				
3	VCCO_3	AJ3				
4	VCCO_4	AC13				
4	VCCO_4	AC14				
4	VCCO_4	AC15				
4	VCCO_4	AC16				
4	VCCO_4	AC17				
4	VCCO_4	AD12				
4	VCCO_4	AD13				
4	VCCO_4	AD14				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	V19				
N/A	GND	V20				
N/A	GND	V21				
N/A	GND	W1				
N/A	GND	W14				
N/A	GND	W15				
N/A	GND	W16				
N/A	GND	W17				
N/A	GND	W18				
N/A	GND	W19				
N/A	GND	W20				
N/A	GND	W21				
N/A	GND	W34				
N/A	GND	Y8				
N/A	GND	Y14				
N/A	GND	Y15				
N/A	GND	Y16				
N/A	GND	Y17				
N/A	GND	Y18				
N/A	GND	Y19				
N/A	GND	Y20				
N/A	GND	Y21				
N/A	GND	Y27				
N/A	GND	AA14				
N/A	GND	AA15				
N/A	GND	AA16				
N/A	GND	AA17				
N/A	GND	AA18				
N/A	GND	AA19				
N/A	GND	AA20				
N/A	GND	AA21				
N/A	GND	AC5				
N/A	GND	AC8				
N/A	GND	AC27				
N/A	GND	AC30				
N/A	GND	AE3				
N/A	GND	AE32				
N/A	GND	H23				

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L64N_1	E18		
1	IO_L64P_1	D18		
1	IO_L60N_1	G18		
1	IO_L60P_1	F18		
1	IO_L59N_1	L18		
1	IO_L59P_1	K18		
1	IO_L58N_1	J18		
1	IO_L58P_1	H18		
1	IO_L57N_1/VREF_1	D17		
1	IO_L57P_1	C17		
1	IO_L56N_1	N18		
1	IO_L56P_1	M18		
1	IO_L55N_1	E17		
1	IO_L55P_1	E16		
1	IO_L54N_1	G17		
1	IO_L54P_1	F16		
1	IO_L53_1/No_Pair	J17		
1	IO_L50_1/No_Pair	H17		
1	IO_L49N_1	J16		
1	IO_L49P_1	H16		
1	IO_L48N_1	D15		
1	IO_L48P_1	C15		
1	IO_L47N_1	L17		
1	IO_L47P_1	K16		
1	IO_L46N_1	F15		
1	IO_L46P_1	E15		
1	IO_L45N_1/VREF_1	H15		
1	IO_L45P_1	G15		
1	IO_L44N_1	N17		
1	IO_L44P_1	M17		
1	IO_L43N_1	D14		
1	IO_L43P_1	C14		
1	IO_L39N_1	F14		
1	IO_L39P_1	E14		
1	IO_L38N_1	M16		
1	IO_L38P_1	M15		
1	IO_L37N_1	H14		
1	IO_L37P_1	G14		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L09P_3	AM3		
3	IO_L08N_3	AK8		
3	IO_L08P_3	AK9		
3	IO_L07N_3	AN6		
3	IO_L07P_3	AN7		
3	IO_L84N_3	AN3	NC	
3	IO_L84P_3	AN4	NC	
3	IO_L82N_3	AN1	NC	
3	IO_L82P_3	AN2	NC	
3	IO_L81N_3/VREF_3	AN5	NC	
3	IO_L81P_3	AP5	NC	
3	IO_L79N_3	AP3	NC	
3	IO_L79P_3	AP4	NC	
3	IO_L78N_3	AP1	NC	
3	IO_L78P_3	AP2	NC	
3	IO_L76N_3	AR2	NC	
3	IO_L76P_3	AR3	NC	
3	IO_L75N_3/VREF_3	AT1	NC	
3	IO_L75P_3	AT2	NC	
3	IO_L73N_3	AT5	NC	
3	IO_L73P_3	AU5	NC	
3	IO_L06N_3	AR6		
3	IO_L06P_3	AT6		
3	IO_L05N_3	AL9		
3	IO_L05P_3	AM8		
3	IO_L04N_3	AP7		
3	IO_L04P_3	AR7		
3	IO_L03N_3/VREF_3	AM9		
3	IO_L03P_3	AN9		
3	IO_L02N_3	AR8		
3	IO_L02P_3	AT8		
3	IO_L01N_3/VRP_3	AT7		
3	IO_L01P_3/VRN_3	AU7		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AT9		
4	IO_L01P_4/INIT_B	AR9		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AK11		
4	IO_L02P_4/D1	AK12		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L57N_5/VREF_5	AT23		
5	IO_L57P_5	AU23		
5	IO_L56N_5	AJ22		
5	IO_L56P_5	AK22		
5	IO_L55N_5	AN23		
5	IO_L55P_5	AP24		
5	IO_L54N_5	AL23		
5	IO_L54P_5	AM23		
5	IO_L53_5/No_Pair	AH23		
5	IO_L50_5/No_Pair	AG23		
5	IO_L49N_5	AR24		
5	IO_L49P_5	AR25		
5	IO_L48N_5	AL24		
5	IO_L48P_5	AM24		
5	IO_L47N_5	AH22		
5	IO_L47P_5	AJ23		
5	IO_L46N_5	AT25		
5	IO_L46P_5	AU25		
5	IO_L45N_5/VREF_5	AN25		
5	IO_L45P_5	AP25		
5	IO_L44N_5	AH24		
5	IO_L44P_5	AH25		
5	IO_L43N_5	AL25		
5	IO_L43P_5	AM25		
5	IO_L39N_5	AT26		
5	IO_L39P_5	AU26		
5	IO_L38N_5	AK24		
5	IO_L38P_5	AK25		
5	IO_L37N_5	AP26		
5	IO_L37P_5	AR26		
5	IO_L36N_5/VREF_5	AM26	NC	
5	IO_L36P_5	AN26	NC	
5	IO_L35N_5	AJ25	NC	
5	IO_L35P_5	AJ26	NC	
5	IO_L34N_5	AR27	NC	
5	IO_L34P_5	AT27	NC	
5	IO_L30N_5	AN27	NC	
5	IO_L30P_5	AP28	NC	

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD21		BB31		
N/A	GNDA21		AY31		
N/A	TXPPAD21		BB32		
N/A	TXNPAD21		BB33		
N/A	VTTXPAD21		BA33		
N/A	AVCCAUXTX21		BA32		
N/A	AVCCAUXRX22		BA34		
N/A	VTRXPAD22		BA35		
N/A	RXNPAD22		BB34		
N/A	RXPPAD22		BB35		
N/A	GNDA22		AY35		
N/A	TXPPAD22		BB36		
N/A	TXNPAD22		BB37		
N/A	VTTXPAD22		BA37		
N/A	AVCCAUXTX22		BA36		
N/A	AVCCAUXRX23		BA38		
N/A	VTRXPAD23		BA39		
N/A	RXNPAD23		BB38		
N/A	RXPPAD23		BB39		
N/A	GNDA23		AY39		
N/A	TXPPAD23		BB40		
N/A	TXNPAD23		BB41		
N/A	VTTXPAD23		BA41		
N/A	AVCCAUXTX23		BA40		
N/A	VCCINT		AB27		
N/A	VCCINT		AB16		
N/A	VCCINT		AC27		
N/A	VCCINT		AC16		
N/A	VCCINT		AD27		
N/A	VCCINT		AD16		
N/A	VCCINT		AE27		
N/A	VCCINT		AE16		
N/A	VCCINT		AF27		
N/A	VCCINT		AF26		
N/A	VCCINT		AF17		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L38P_3	AE9	
3	IO_L37N_3	AH3	
3	IO_L37P_3	AJ3	
3	IO_L36N_3	AJ1	
3	IO_L36P_3	AJ2	
3	IO_L35N_3	AE6	
3	IO_L35P_3	AE7	
3	IO_L34N_3	AK6	
3	IO_L34P_3	AK7	
3	IO_L33N_3/VREF_3	AK3	
3	IO_L33P_3	AK4	
3	IO_L32N_3	AE12	
3	IO_L32P_3	AF12	
3	IO_L31N_3	AL5	
3	IO_L31P_3	AL6	
3	IO_L30N_3	AL3	
3	IO_L30P_3	AL4	
3	IO_L29N_3	AF10	
3	IO_L29P_3	AF11	
3	IO_L28N_3	AK2	
3	IO_L28P_3	AL2	
3	IO_L27N_3/VREF_3	AL7	
3	IO_L27P_3	AM6	
3	IO_L26N_3	AF7	
3	IO_L26P_3	AF8	
3	IO_L25N_3	AM4	
3	IO_L25P_3	AM5	
3	IO_L24N_3	AM1	
3	IO_L24P_3	AM2	
3	IO_L23N_3	AG10	
3	IO_L23P_3	AG11	
3	IO_L22N_3	AM7	
3	IO_L22P_3	AN7	
3	IO_L21N_3/VREF_3	AN5	
3	IO_L21P_3	AN6	
3	IO_L20N_3	AG8	
3	IO_L20P_3	AG9	