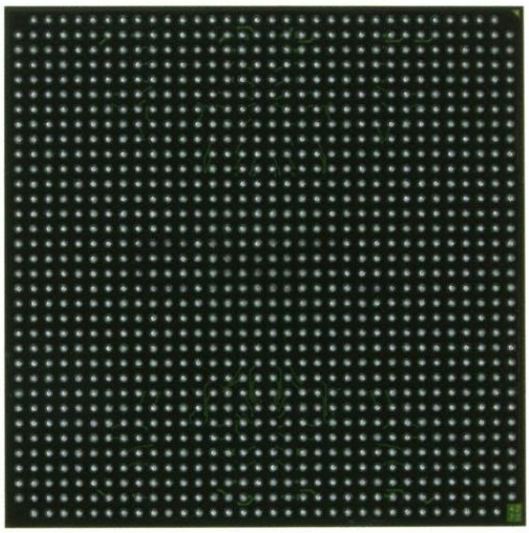

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6ff1152i

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 13 shows the initial situation in the FPGA's receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

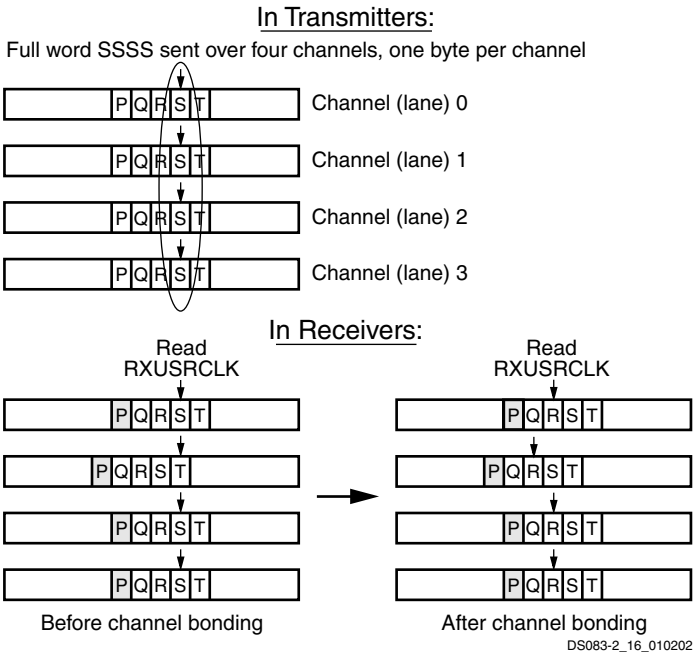

Figure 13: **Channel Bonding (Alignment)**

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 13, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bonding character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 13. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

RocketIO Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports 16 transceiver primitives, as shown in Table 6.

Each of the primitives in Table 6 defines default values for the configuration attributes, allowing some number of them to be modified by the user. Refer to the ***RocketIO Transceiver User Guide*** for more details.

Table 6: **Supported RocketIO MGT Protocol Primitives**

GT_CUSTOM	Fully customizable by user
GT_FIBRE_CHAN_1	Fibre Channel, 1-byte data path
GT_FIBRE_CHAN_2	Fibre Channel, 2-byte data path
GT_FIBRE_CHAN_4	Fibre Channel, 4-byte data path
GT_ETHERNET_1	Gigabit Ethernet, 1-byte data path
GT_ETHERNET_2	Gigabit Ethernet, 2-byte data path
GT_ETHERNET_4	Gigabit Ethernet, 4-byte data path
GT_XAUI_1	10-gigabit Ethernet, 1-byte data path
GT_XAUI_2	10-gigabit Ethernet, 2-byte data path
GT_XAUI_4	10-gigabit Ethernet, 4-byte data path
GT_INFINIBAND_1	Infiniband, 1-byte data path
GT_INFINIBAND_2	Infiniband, 2-byte data path
GT_INFINIBAND_4	Infiniband, 4-byte data path
GT_AURORA_1(1)	1-byte data path
GT_AURORA_2(1)	2-byte data path
GT_AURORA_4(1)	4-byte data path

Notes:
1. For more information on the Aurora protocol, visit http://www.xilinx.com.

Other RocketIO Features and Notes

CRC

The RocketIO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, FibreChannel, and Gigabit Ethernet.

On the transmitter side, the CRC logic recognizes where the CRC bytes should be inserted and replaces four placeholder bytes at the tail of a data packet with the computed CRC. For Gigabit Ethernet and FibreChannel, transmitter

memory protection. Working with appropriate system-level software, the MMU provides the following functions:

- Translation of the 4 GB effective address space into physical addresses
- Independent enabling of instruction and data translation/protection
- Page-level access control using the translation mechanism
- Software control of page replacement strategy
- Additional control over protection using zones
- Storage attributes for cache policy and speculative memory access control

The MMU can be disabled under software control. If the MMU is not used, the PPC405 core provides other storage control mechanisms.

Translation Look-Aside Buffer (TLB)

The Translation Look-Aside Buffer (TLB) is the hardware resource that controls translation and protection. It consists of 64 entries, each specifying a page to be translated. The TLB is fully associative; a given page entry can be placed anywhere in the TLB. The translation function of the MMU occurs pre-cache. Cache tags and indexing use physical addresses.

Software manages the establishment and replacement of TLB entries. This gives system software significant flexibility in implementing a custom page replacement strategy. For example, to reduce TLB thrashing or translation delays, software can reserve several TLB entries in the TLB for globally accessible static mappings. The instruction set provides several instructions used to manage TLB entries. These instructions are privileged and require the software to be executing in supervisor state. Additional TLB instructions are provided to move TLB entry fields to and from GPRs.

The MMU divides logical storage into pages. Eight page sizes (1 KB, 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB) are simultaneously supported, such that, at any given time, the TLB can contain entries for any combination of page sizes. In order for a logical to physical translation to exist, a valid entry for the page containing the logical address must be in the TLB. Addresses for which no TLB entry exists cause TLB-Miss exceptions.

To improve performance, four instruction-side and eight data-side TLB entries are kept in shadow arrays. The shadow arrays allow single-cycle address translation and also help to avoid TLB contention between load/store and instruction fetch operations. Hardware manages the replacement and invalidation of shadow-TLB entries; no system software action is required.

Memory Protection

When address translation is enabled, the translation mechanism provides a basic level of protection.

The Zone Protection Register (ZPR) enables the system software to override the TLB access controls. For example, the ZPR provides a way to deny read access to application programs. The ZPR can be used to classify storage by type; access by type can be changed without manipulating individual TLB entries.

The PowerPC Architecture provides WIU0GE (write-back / write-through, cacheability, user-defined 0, guarded, endian) storage attributes that control memory accesses, using bits in the TLB or, when address translation is disabled, storage attribute control registers.

When address translation is enabled, storage attribute control bits in the TLB control the storage attributes associated with the current page. When address translation is disabled, bits in each storage attribute control register control the storage attributes associated with storage regions. Each storage attribute control register contains 32 fields. Each field sets the associated storage attribute for a 128 MB memory region.

Timers

The embedded PPC405 core contains a 64-bit time base and three timers, as shown in Figure 17:

- Programmable Interval Timer (PIT)
- Fixed Interval Timer (FIT)
- Watchdog Timer (WDT)

The time base counter increments either by an internal signal equal to the CPU clock rate or by a separate external timer clock signal. No interrupts are generated when the time base rolls over. The three timers are synchronous with the time base.

The PIT is a 32-bit register that decrements at the same rate as the time base is incremented. The user loads the PIT register with a value to create the desired delay. When the register reaches zero, the timer stops decrementing and generates a PIT interrupt. Optionally, the PIT can be programmed to auto-reload the last value written to the PIT register, after which the PIT continues to decrement.

The FIT generates periodic interrupts based on one of four selectable bits in the time base. When the selected bit changes from 0 to 1, the PPC405 core generates a FIT interrupt.

The WDT provides a periodic critical-class interrupt based on a selected bit in the time base. This interrupt can be used for system error recovery in the event of software or system lockups. Users may select one of four time periods for the interval and the type of reset generated if the WDT expires twice without an intervening clear from software. If enabled, the watchdog timer generates a reset unless an exception handler updates the WDT status bit before the timer has completed two of the selected timer intervals.

Table 26: **RocketIO X Transmitter Switching Characteristics**(1)

Description	Symbol	Conditions	BREFCLK Frequency	Min	Typ	Max	Units
Serial data rate	F_{GTX}			2.488		6.25	Gb/s
Serial data output total jitter (p-p)(3)	T_{TJ}	2.488 Gb/s			0.15	0.20	UI(2)
		3.125 Gb/s			0.14	0.19	UI
		4.25 Gb/s			0.39	0.48	UI
		6.25 Gb/s			0.42	0.54	UI
Serial data output deterministic jitter (p-p)(3)	T_{DJ}	2.488 Gb/s	155.52 MHz		0.03	0.17	UI
		3.125 Gb/s	156.25 MHz		0.03	0.17	UI
		4.25 Gb/s	212.5 MHz		0.14	0.26	UI
		6.25 Gb/s	312.5 MHz		0.17	0.35	UI
Serial data output random jitter (p-p)(3,4)	T_{RJ}	2.488 Gb/s	155.52 MHz		0.12	0.18	UI
		3.125 Gb/s	156.25 MHz		0.12	0.20	UI
		4.25 Gb/s	212.5 MHz		0.25	0.39	UI
		6.25 Gb/s	312.5 MHz		0.25	0.39	UI
TX rise time	T_{RTX}	20% – 80% @ 2.500 Gb/s			60		ps
TX fall time	T_{FTX}				60		ps
Transmit latency(5)	T_{TXLAT}				14	19	TXUSRCLK cycles
TXUSRCLK duty cycle	T_{TXDC}			45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}			45	50	55	%

Notes:
1. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.
2. UI = Unit Interval
3. Total Jitter $T_{TJ} = T_{DJ} + T_{RJ}$
4. T_{RJ} specifications are *wideband* and include low-frequency jitter components (also referred to as *wander*).T_{RJ} specified is peak-to-peak, estimated at BER=10^{-12} using the Bathtub Method.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO X Transceiver User Guide*** for more information on calculating latency.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

Table 37: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.58	1.68	1.85	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.65	1.82	1.99	ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}	1.23	1.35	1.51	ns, max
T input to valid data on Pad	T_{IOTP}	1.51	1.63	1.78	ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$	1.08	1.22	1.36	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.56	1.69	1.85	ns, max
GTS to Pad high-impedance(2)	T_{GTS}	4.11	4.73	5.20	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.59	1.76	1.93	ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}	1.39	1.55	1.73	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.67	1.82	2.00	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
Set/Reset Delays					
Minimum Pulse Width, SR inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
SR input to Pad (asynchronous)	T_{IOSRP}	2.33	2.56	2.83	ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}	1.97	2.16	2.41	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.24	2.44	2.69	ns, max
GSR to Pad	T_{IOGSRQ}	5.87	6.75	7.43	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 7; corresponding timing characteristics are listed in Table 49.

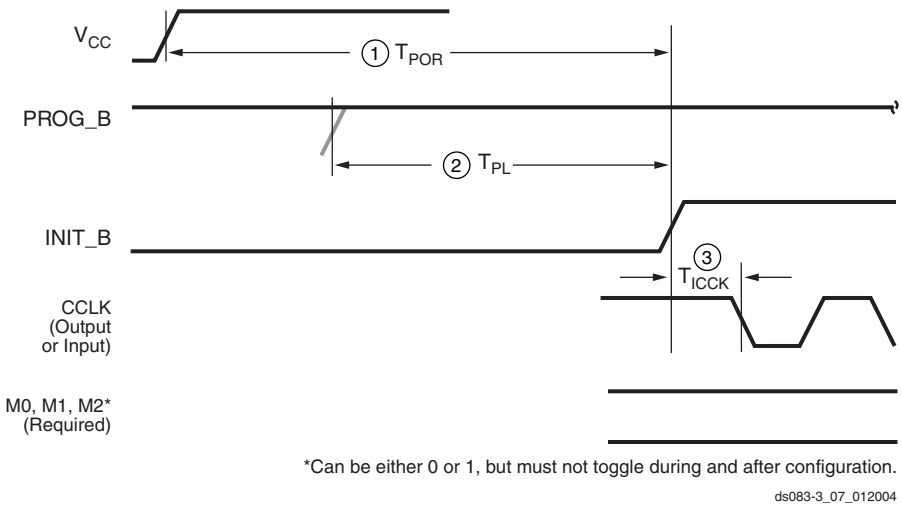

Figure 7: **Configuration Power-Up Timing**

Table 49: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.25	µs, min
			4.00	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information

DS083 (v5.0) June 21, 2011 **Product Specification**

This document provides Virtex™-II Pro Device/Package Combinations, Maximum I/Os, and Virtex-II Pro Pin Definitions, followed by pinout tables, for these packages:

- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- FF672 Flip-Chip Fine-Pitch BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1148 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- FF1704 Flip-Chip Fine-Pitch BGA Package
- FF1696 Flip-Chip Fine-Pitch BGA Package

For device pinout diagrams and layout guidelines, refer to the **Virtex-II Pro Platform FPGA User Guide**. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Pro Device/Package Combinations and Maximum I/Os(1)

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)

Table 1: **Wire-Bond Packages Information**

Package(1)	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676
Pitch (mm)	1.00	1.00	1.00
Size (mm)	17 x 17	23 x 23	26 x 26
Maximum I/Os	140	248	412

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	27 x 27	31 x 31	35 x 35	35 x 35	40 x 40	42.5 x 42.5	42.5 x 42.5
Maximum I/Os	396	556	644	812	964	1040	1200

Table 3 shows the number of available I/Os, the number of RocketIO™ (or RocketIO X) multi-gigabit transceiver (MGT) pins, and the number of differential I/O pairs for each Virtex-II Pro device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), the nine (per transceiver) RocketIO MGT pins (TXP, TXN, RXP, RXN, AVCCAUXTX, AVCCAUXRX, VTTX, VTRX, and GNDA), and for Virtex-II Pro X devices only, the two BREFCLKN/ BREFCLKP differential clock input pairs (four pins). The Virtex-II Pro X devices are highlighted in bold type.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 5, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	IO_L85N_7	G2
7	IO_L06P_7	G3
7	IO_L06N_7	G4
7	IO_L04P_7	F1
7	IO_L04N_7/VREF_7	F2
7	IO_L03P_7	F3
7	IO_L03N_7	F4
7	IO_L02P_7	F5
7	IO_L02N_7	E4
7	IO_L01P_7/VRN_7	E2
7	IO_L01N_7/VRP_7	E3
0	VCCO_0	F8
0	VCCO_0	F7
0	VCCO_0	E8
1	VCCO_1	F9
1	VCCO_1	F10
1	VCCO_1	E9
2	VCCO_2	H12
2	VCCO_2	H11
2	VCCO_2	G11
3	VCCO_3	K11
3	VCCO_3	J12
3	VCCO_3	J11
4	VCCO_4	M9
4	VCCO_4	L9
4	VCCO_4	L10
5	VCCO_5	M8
5	VCCO_5	L8
5	VCCO_5	L7
6	VCCO_6	K6
6	VCCO_6	J6
6	VCCO_6	J5
7	VCCO_7	H6
7	VCCO_7	H5

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/BUSY/DOUT(1)	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0/DIN(1)	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L49N_3	T24			
3	IO_L49P_3	U24			
3	IO_L48N_3	U23			
3	IO_L48P_3	U22			
3	IO_L47N_3	T19			
3	IO_L47P_3	U19			
3	IO_L45N_3/VREF_3	V26			
3	IO_L45P_3	V25			
3	IO_L43N_3	V24			
3	IO_L43P_3	V23			
3	IO_L42N_3	V22			
3	IO_L42P_3	V21			
3	IO_L41N_3	V20			
3	IO_L41P_3	V19			
3	IO_L39N_3/VREF_3	W26			
3	IO_L39P_3	W25			
3	IO_L37N_3	W21			
3	IO_L37P_3	W20			
3	IO_L36N_3	Y26			
3	IO_L36P_3	Y25			
3	IO_L35N_3	Y24			
3	IO_L35P_3	Y23			
3	IO_L33N_3/VREF_3	W22			
3	IO_L33P_3	Y22			
3	IO_L31N_3	AA26			
3	IO_L31P_3	AA25			
3	IO_L24N_3	AA24	NC		
3	IO_L24P_3	AA23	NC		
3	IO_L23N_3	Y21	NC		
3	IO_L23P_3	AA21	NC		
3	IO_L06N_3	AB26			
3	IO_L06P_3	AB25			
3	IO_L05N_3	AA22			
3	IO_L05P_3	AB23			
3	IO_L03N_3/VREF_3	AC26			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L52P_7	M7			
7	IO_L52N_7/VREF_7	L7			
7	IO_L50P_7	K1			
7	IO_L50N_7	K2			
7	IO_L49P_7	L3			
7	IO_L49N_7	K3			
7	IO_L48P_7	K4			
7	IO_L48N_7	K5			
7	IO_L46P_7	L8			
7	IO_L46N_7/VREF_7	K8			
7	IO_L44P_7	J1			
7	IO_L44N_7	J2			
7	IO_L43P_7	J3			
7	IO_L43N_7	J4			
7	IO_L42P_7	J5			
7	IO_L42N_7	J6			
7	IO_L40P_7	J7			
7	IO_L40N_7/VREF_7	J8			
7	IO_L38P_7	H1			
7	IO_L38N_7	H2			
7	IO_L37P_7	H6			
7	IO_L37N_7	H7			
7	IO_L36P_7	G1			
7	IO_L36N_7	G2			
7	IO_L34P_7	G3			
7	IO_L34N_7/VREF_7	G4			
7	IO_L32P_7	H5			
7	IO_L32N_7	G5			
7	IO_L31P_7	F1			
7	IO_L31N_7	F2			
7	IO_L24P_7	F3	NC		
7	IO_L24N_7	F4	NC		
7	IO_L06P_7	G6			
7	IO_L06N_7	F6			
7	IO_L04P_7	E1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L01N_0/VRP_0		E25			
0	IO_L01P_0/VRN_0		E24			
0	IO_L02N_0		F24			
0	IO_L02P_0		F23			
0	IO_L03N_0		E23			
0	IO_L03P_0/VREF_0		E22			
0	IO_L05_0/No_Pair		G23			
0	IO_L06N_0		H22			
0	IO_L06P_0		G22			
0	IO_L07N_0		F22			
0	IO_L07P_0		F21			
0	IO_L08N_0		D24			
0	IO_L08P_0		C24			
0	IO_L09N_0		H21			
0	IO_L09P_0/VREF_0		G21			
0	IO_L37N_0		E21			
0	IO_L37P_0		D21			
0	IO_L38N_0		D23			
0	IO_L38P_0		C23			
0	IO_L39N_0		H20			
0	IO_L39P_0		G20			
0	IO_L43N_0		E20			
0	IO_L43P_0		D20			
0	IO_L44N_0		B23			
0	IO_L44P_0		A23			
0	IO_L45N_0		H19			
0	IO_L45P_0/VREF_0		G19			
0	IO_L46N_0		E19	NC		
0	IO_L46P_0		E18	NC		
0	IO_L47N_0		C22	NC		
0	IO_L47P_0		B22	NC		
0	IO_L48N_0		F20	NC		
0	IO_L48P_0		F19	NC		
0	IO_L49N_0		G17	NC		
0	IO_L49P_0		F17	NC		
0	IO_L50_0/No_Pair		B21	NC		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L24N_7	L37		
7	IO_L23P_7	P31		
7	IO_L23N_7	P32		
7	IO_L22P_7	L34		
7	IO_L22N_7/VREF_7	L35		
7	IO_L21P_7	L32		
7	IO_L21N_7	L33		
7	IO_L20P_7	N29		
7	IO_L20N_7	M29		
7	IO_L19P_7	K38		
7	IO_L19N_7	K39		
7	IO_L18P_7	J37		
7	IO_L18N_7	K37		
7	IO_L17P_7	N30		
7	IO_L17N_7	P30		
7	IO_L16P_7	K35		
7	IO_L16N_7/VREF_7	K36		
7	IO_L15P_7	K34		
7	IO_L15N_7	K33		
7	IO_L14P_7	N31		
7	IO_L14N_7	M32		
7	IO_L13P_7	J38		
7	IO_L13N_7	J39		
7	IO_L12P_7	J35		
7	IO_L12N_7	H36		
7	IO_L11P_7	M30		
7	IO_L11N_7	L31		
7	IO_L10P_7	J33		
7	IO_L10N_7/VREF_7	J34		
7	IO_L09P_7	H37		
7	IO_L09N_7	H38		
7	IO_L08P_7	K31		
7	IO_L08N_7	K32		
7	IO_L07P_7	H33		
7	IO_L07N_7	H34		
7	IO_L84P_7	G38	NC	
7	IO_L84N_7	G39	NC	
7	IO_L82P_7	G36	NC	

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L53N_3		AE10		
3	IO_L53P_3		AE11		
3	IO_L52N_3		AE1		
3	IO_L52P_3		AE2		
3	IO_L51N_3/VREF_3		AE4		
3	IO_L51P_3		AE5		
3	IO_L50N_3		AF11		
3	IO_L50P_3		AE12		
3	IO_L49N_3		AE7		
3	IO_L49P_3		AE8		
3	IO_L48N_3		AF1		
3	IO_L48P_3		AF2		
3	IO_L47N_3		AG12		
3	IO_L47P_3		AF12		
3	IO_L46N_3		AF3		
3	IO_L46P_3		AF4		
3	IO_L45N_3/VREF_3		AF5		
3	IO_L45P_3		AF6		
3	IO_L44N_3		AF7		
3	IO_L44P_3		AF8		
3	IO_L43N_3		AF9		
3	IO_L43P_3		AF10		
3	IO_L42N_3		AG2		
3	IO_L42P_3		AG3		
3	IO_L41N_3		AG10		
3	IO_L41P_3		AG11		
3	IO_L40N_3		AG4		
3	IO_L40P_3		AG5		
3	IO_L39N_3/VREF_3		AG6		
3	IO_L39P_3		AG7		
3	IO_L38N_3		AG8		
3	IO_L38P_3		AH8		
3	IO_L37N_3		AH1		
3	IO_L37P_3		AH2		
3	IO_L36N_3		AH3		
3	IO_L36P_3		AJ3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L19P_5		AV32		
5	IO_L09N_5/VREF_5		AP32		
5	IO_L09P_5		AR32		
5	IO_L08N_5		AW33		
5	IO_L08P_5		AV33		
5	IO_L07N_5/VREF_5		AT33		
5	IO_L07P_5		AU33		
5	IO_L06N_5/VRP_5		AP33		
5	IO_L06P_5/VRN_5		AR33		
5	IO_L05_5/No_Pair		AN32		
5	IO_L03N_5/D4		AW34		
5	IO_L03P_5/D5		AY34		
5	IO_L02N_5/D6		AV34		
5	IO_L02P_5/D7		AU34		
5	IO_L01N_5/RDWR_B		AR34		
5	IO_L01P_5/CS_B		AT34		
6	IO_L01P_6/VRN_6		AW37		
6	IO_L01N_6/VRP_6		AV37		
6	IO_L02P_6		AW36		
6	IO_L02N_6		AV36		
6	IO_L03P_6		AY37		
6	IO_L03N_6/VREF_6		AY38		
6	IO_L04P_6		AU36		
6	IO_L04N_6		AT37		
6	IO_L05P_6		AU35		
6	IO_L05N_6		AT35		
6	IO_L06P_6		AW41		
6	IO_L06N_6		AW42		
6	IO_L73P_6		AV41		
6	IO_L73N_6		AV42		
6	IO_L74P_6		AW40		
6	IO_L74N_6		AV40		
6	IO_L75P_6		AU39		
6	IO_L75N_6/VREF_6		AU40		
6	IO_L76P_6		AU41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L45P_7		U39		
7	IO_L45N_7		U40		
7	IO_L44P_7		U33		
7	IO_L44N_7		U34		
7	IO_L43P_7		U37		
7	IO_L43N_7		U38		
7	IO_L42P_7		U35		
7	IO_L42N_7		U36		
7	IO_L41P_7		T32		
7	IO_L41N_7		T33		
7	IO_L40P_7		T40		
7	IO_L40N_7/VREF_7		T41		
7	IO_L39P_7		T38		
7	IO_L39N_7		T39		
7	IO_L38P_7		R35		
7	IO_L38N_7		T35		
7	IO_L37P_7		T36		
7	IO_L37N_7		T37		
7	IO_L36P_7		R31		
7	IO_L36N_7		R32		
7	IO_L35P_7		R41		
7	IO_L35N_7		R42		
7	IO_L34P_7		R40		
7	IO_L34N_7/VREF_7		P40		
7	IO_L33P_7		R37		
7	IO_L33N_7		R38		
7	IO_L32P_7		R33		
7	IO_L32N_7		R34		
7	IO_L31P_7		P41		
7	IO_L31N_7		P42		
7	IO_L30P_7		P37		
7	IO_L30N_7		P38		
7	IO_L29P_7		P31		
7	IO_L29N_7		P32		
7	IO_L28P_7		P35		
7	IO_L28N_7/VREF_7		P36		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L10N_5	AW27	NC
5	IO_L10P_5	AW26	NC
5	IO_L45N_5/VREF_5	AN27	
5	IO_L45P_5	AP27	
5	IO_L44N_5	AU27	
5	IO_L44P_5	AV27	
5	IO_L43N_5	AR27	
5	IO_L43P_5	AR26	
5	IO_L39N_5	AL27	
5	IO_L39P_5	AM27	
5	IO_L38N_5	BA28	
5	IO_L38P_5	BB28	
5	IO_L37N_5	AY28	
5	IO_L37P_5	AY27	
5	IO_L87N_5/VREF_5	AN28	
5	IO_L87P_5	AP28	
5	IO_L86N_5	AU28	
5	IO_L86P_5	AV28	
5	IO_L85N_5	AT28	
5	IO_L85P_5	AT27	
5	IO_L84N_5	AL28	
5	IO_L84P_5	AM28	
5	IO_L83_5/No_Pair	BA29	
5	IO_L80_5/No_Pair	BB29	
5	IO_L79N_5	AY29	
5	IO_L79P_5	AW28	
5	IO_L78N_5	AN29	
5	IO_L78P_5	AP29	
5	IO_L77N_5	AU29	
5	IO_L77P_5	AV29	
5	IO_L76N_5	AT29	
5	IO_L76P_5	AR28	
5	IO_L36N_5/VREF_5	AL29	
5	IO_L36P_5	AM29	
5	IO_L35N_5	AY30	
5	IO_L35P_5	BA30	
5	IO_L34N_5	AT30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	E13	
N/A	GND	A13	
N/A	GND	AD12	
N/A	GND	W12	
N/A	GND	BB9	
N/A	GND	AV9	
N/A	GND	AP9	
N/A	GND	AK9	
N/A	GND	AF9	
N/A	GND	AC9	
N/A	GND	Y9	
N/A	GND	U9	
N/A	GND	N9	
N/A	GND	J9	
N/A	GND	E9	
N/A	GND	A9	
N/A	GND	BB5	
N/A	GND	AV5	
N/A	GND	AP5	
N/A	GND	AK5	
N/A	GND	AF5	
N/A	GND	AC5	
N/A	GND	Y5	
N/A	GND	U5	
N/A	GND	N5	
N/A	GND	J5	
N/A	GND	E5	
N/A	GND	A5	
N/A	GND	BA3	
N/A	GND	B3	
N/A	GND	BA2	
N/A	GND	AY2	
N/A	GND	C2	
N/A	GND	B2	
N/A	GND	AV1	
N/A	GND	AP1	
N/A	GND	AK1	