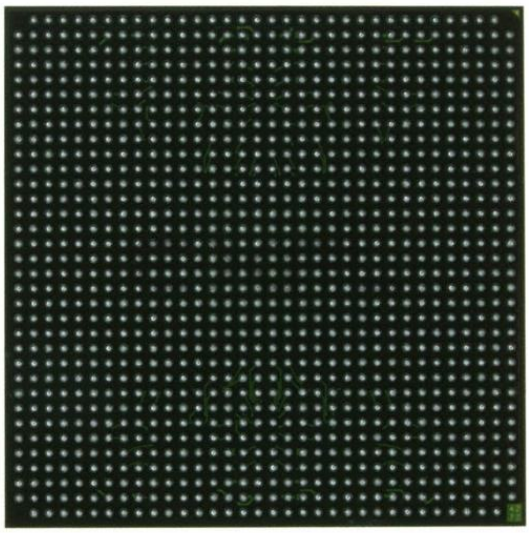

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6ffg1152c

- Single-cycle and multi-cycle mode option for I-side and D-side interfaces
- Single cycle = one CPU clock cycle; multi-cycle = minimum of two and maximum of eight CPU clock cycles
- FPGA configurable DCR addresses within DSOCM and ISOCM.
- Independent 16 MB logical memory space available within PPC405 memory map for each of the DSOCM and ISOCM. The number of block RAMs in the device might limit the maximum amount of OCM supported.
- Maximum of 64K and 128K bytes addressable from DSOCM and ISOCM interfaces, respectively, using address outputs from OCM directly without additional decoding logic.

Data-Side OCM (DSOCM)

- 32-bit Data Read bus and 32-bit Data Write bus
- Byte write access to DSBRAM support
- Second port of dual port DSBRAM is available to read/write from an FPGA interface
- 22-bit address to DSBRAM port
- 8-bit DCR Registers: DSCNTL, DSARC
- Three alternatives to write into DSBRAM: BRAM initialization, CPU, FPGA H/W using second port

Instruction-Side OCM (ISOCM)

The ISOCM interface contains a 64-bit read only port, for instruction fetches, and a 32-bit write only port, to initialize or test the ISBRAM. When implementing the read only port, the user must deassert the write port inputs. The preferred method of initializing the ISBRAM is through the configuration bitstream.

- 64-bit Data Read Only bus (two instructions per cycle)
- 32-bit Data Write Only bus (through DCR)
- Separate 21-bit address to ISBRAM
- 8-bit DCR Registers: ISCNTL, ISARC
- 32-bit DCR Registers: ISINIT, ISFILL
- Two alternatives to write into ISBRAM: BRAM initialization, DCR and write instruction

Clock/Control Interface Logic

The clock/control interface logic provides proper initialization and connections for PPC405 clock/power management, resets, PLB cycle control, and OCM interfaces. It also couples user signals between the FPGA fabric and the embedded PPC405 CPU core.

The processor clock connectivity is similar to CLB clock pins. It can connect either to global clock nets or general routing resources. Therefore the processor clock source can come from DCM, CLB, or user package pin.

CPU-FPGA Interfaces

All Processor Block user pins link up with the general FPGA routing resources through the CPU-FPGA interface. Therefore processor signals have the same routability as other non-Processor Block user signals. Longlines and hex lines travel across the Processor Block both vertically and horizontally, allowing signals to route through the Processor Block.

Processor Local Bus (PLB) Interfaces

The PPC405 core accesses high-speed system resources through PLB interfaces on the instruction and data cache controllers. The PLB interfaces provide separate 32-bit address/64-bit data buses for the instruction and data sides.

The cache controllers are both PLB masters. PLB arbiters are implemented in the FPGA fabric and are available as soft IP cores.

Device Control Register (DCR) Bus Interface

The device control register (DCR) bus has 10 bits of address space for components external to the PPC405 core. Using the DCR bus to manage status and configuration registers reduces PLB traffic and improves system integrity. System resources on the DCR bus are protected or isolated from wayward code since the DCR bus is not part of the system memory map.

External Interrupt Controller (EIC) Interface

Two level-sensitive user interrupt pins (critical and non-critical) are available. They can be either driven by user defined logic or Xilinx soft interrupt controller IP core outside the Processor Block.

Clock/Power Management (CPM) Interface

The CPM interface supports several methods of clock distribution and power management. Three modes of operation that reduce power consumption below the normal operational level are available.

Reset Interface

There are three user reset input pins (core, chip, and system) and three user reset output pins for different levels of reset, if required.

Debug Interface

Debugging interfaces on the embedded PPC405 core, consisting of the JTAG and Trace ports, offer access to resources internal to the core and assist in software development. The JTAG port provides basic JTAG chip testing functionality as well as the ability for external debug tools to gain control of the processor for debug purposes. The Trace port furnishes programmers with a mechanism for acquiring instruction execution traces.

The JTAG port is compatible with IEEE Std 1149.1, which defines a test access port (TAP) and Boundary-Scan architecture. Extensions to the JTAG interface provide debuggers with processor control that includes stopping, starting, and stepping the PPC405 core. These extensions are compliant with the IEEE 1149.1 specifications for vendor-specific extensions.

Multiplexers

Virtex-II Pro function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II Pro slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 41. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Pro Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

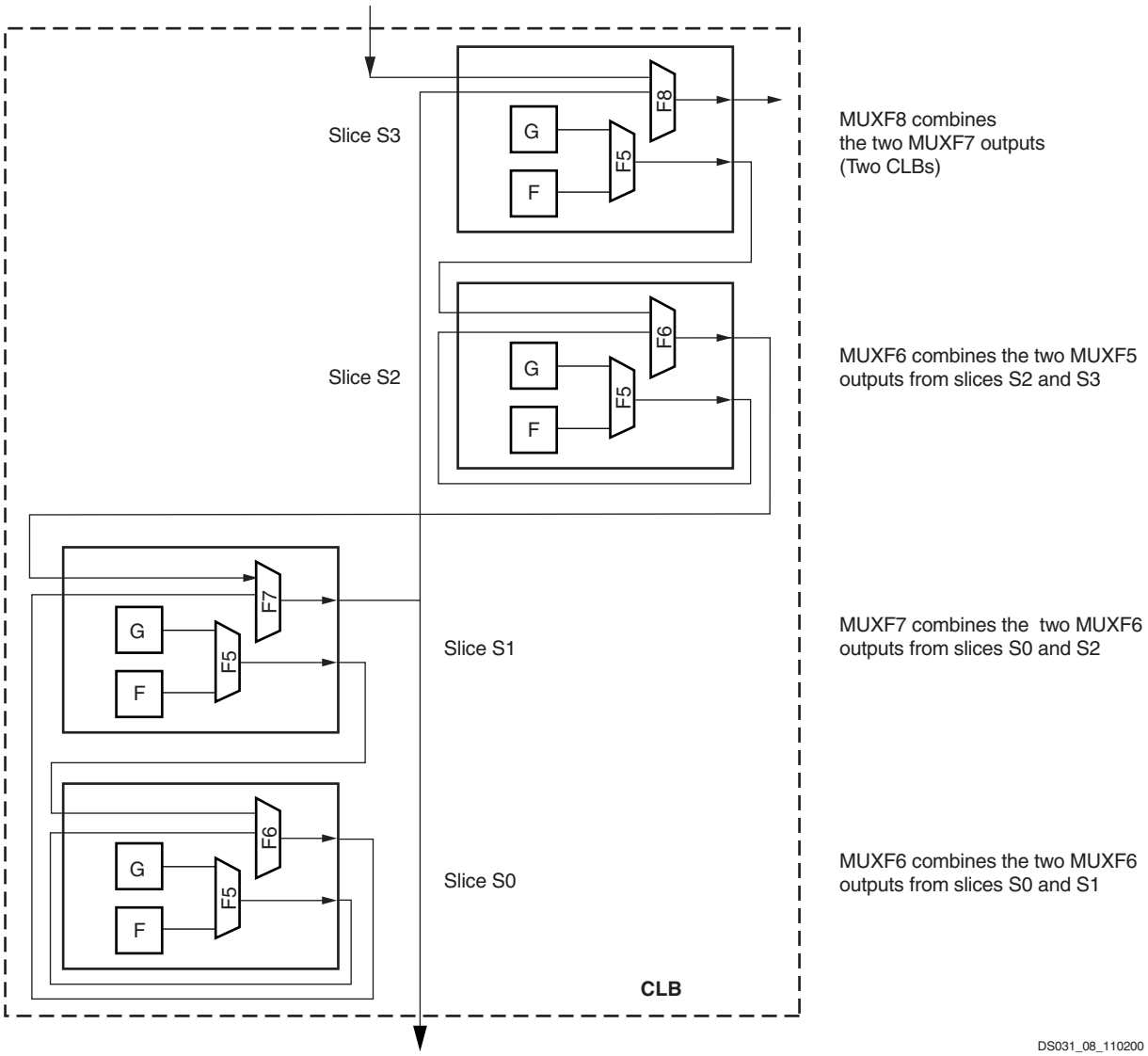


Figure 41: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II Pro CLB has two separate carry chains, as shown in the Figure 42.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II Pro device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 34) improves the efficiency of multiplier implementation.

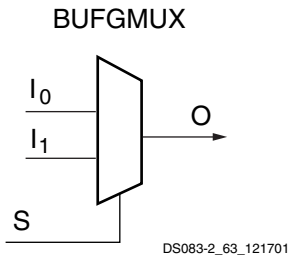


Figure 60: **Virtex-II Pro BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II Pro devices have 16 global clock multiplexer buffers.

Figure 61 shows a switchover from I0 to I1.

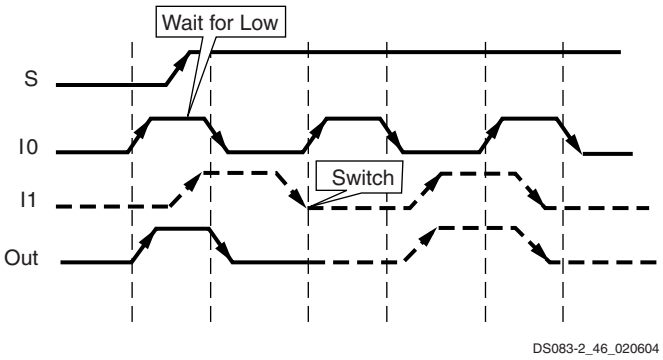


Figure 61: **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II Pro devices. There are more than 72 local clocks in the Virtex-II Pro family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II Pro FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II Pro devices.

Digital Clock Manager (DCM)

The Virtex-II Pro DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 62). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

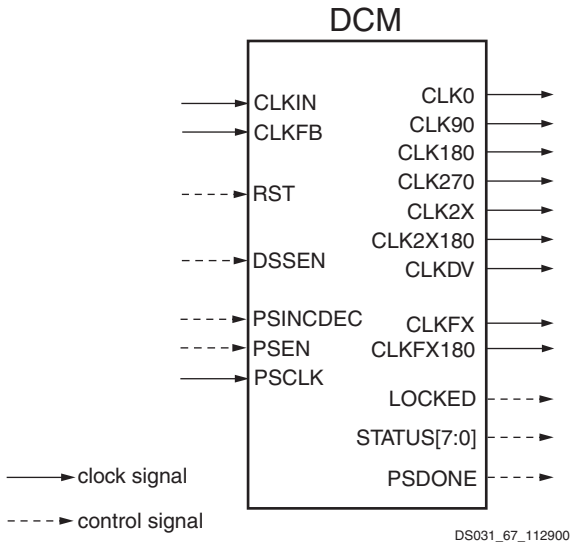


Figure 62: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II Pro configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

LVDS DC Specifications (LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.602	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.898			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	454	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100	350	600	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100		1000	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	V_{CCO} = 2.375V		V_{CCO} = 2.5V		V_{CCO} = 2.625V		Units
	Min	Max	Min	Max	Min	Max	
V_{OH}	1.35	1.495	1.475	1.62	1.6	1.745	V
V_{OL}	0.565	0.755	0.69	0.88	0.815	1.005	V
V_{IH}	0.8	2.0	0.8	2.0	0.8	2.0	V
V_{IL}	0.5	1.7	0.5	1.7	0.5	1.7	V
Differential Input Voltage	0.100	1.5	0.100	1.5	0.100	1.5	V

CLB Distributed RAM Switching Characteristics

Table 43: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.25	1.38	1.54	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.57	1.75	1.95	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.52	1.68	1.88	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.38/–0.07	0.41/–0.07	0.46/–0.08	ns, min
F/G address inputs	T_{AS}/T_{AH}	0.42/ 0.00	0.47/ 0.00	0.52/ 0.00	ns, min
SR input	T_{WES}/T_{WEH}	0.22/ 0.04	0.24/ 0.05	0.26/ 0.05	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.63	0.72	0.79	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.25	1.44	1.58	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 44: **CLB Shift Register Switching Characteristics**

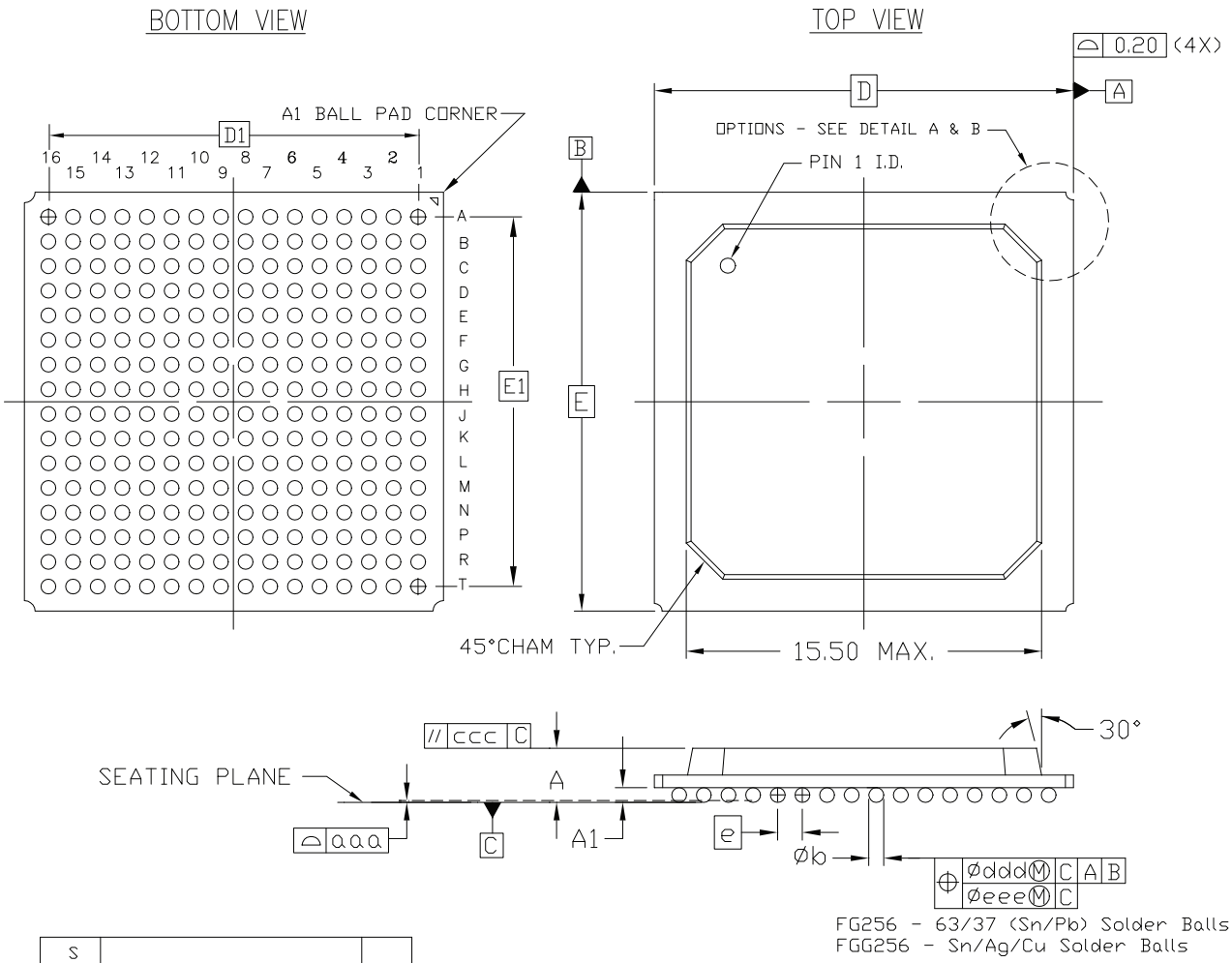
Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.78	3.12	3.49	ns, max
Clock CLK to X/Y outputs	T_{REG32}	3.10	3.49	3.90	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.84	3.18	3.55	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.55	2.88	3.21	ns, max
Clock CLK to Shiftout	T_{CKSH}	2.50	2.83	3.15	ns, max
Clock CLK to F5 output	T_{REGF5}	3.05	3.42	3.83	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.70/–0.16	0.77/–0.18	0.98/–0.21	ns, min
SR input	T_{WSS}/T_{WSH}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{SRPL}	0.63	0.72	0.79	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

Figure 1: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
1	IO_L45N_1/VREF_1	C18			
1	IO_L45P_1	D18			
1	IO_L43N_1	E18			
1	IO_L43P_1	F18			
1	IO_L39N_1	G18			
1	IO_L39P_1	H18			
1	IO_L37N_1	A19			
1	IO_L37P_1	B19			
1	IO_L09N_1/VREF_1	E19			
1	IO_L09P_1	F19			
1	IO_L07N_1	G19			
1	IO_L07P_1	H19			
1	IO_L06N_1	C20			
1	IO_L06P_1	D20			
1	IO_L05_1/No_Pair	E20			
1	IO_L03N_1/VREF_1	F20			
1	IO_L03P_1	G20			
1	IO_L02N_1	D21			
1	IO_L02P_1	E21			
1	IO_L01N_1/VRP_1	D22			
1	IO_L01P_1/VRN_1	E22			
2	IO_L01N_2/VRP_2	C25			
2	IO_L01P_2/VRN_2	C26			
2	IO_L02N_2	D25			
2	IO_L02P_2	D26			
2	IO_L03N_2	E23			
2	IO_L03P_2	F22			
2	IO_L04N_2/VREF_2	E25			
2	IO_L04P_2	E26			
2	IO_L06N_2	F21			
2	IO_L06P_2	G21			
2	IO_L24N_2	F23	NC		
2	IO_L24P_2	F24	NC		
2	IO_L31N_2	F25			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
5	IO_L44N_5	AK22				
5	IO_L44P_5	AJ22				
5	IO_L43N_5	AF21				
5	IO_L43P_5	AE21				
5	IO_L39N_5	AK24				
5	IO_L39P_5	AJ24				
5	IO_L38N_5	AH22				
5	IO_L38P_5	AG22				
5	IO_L37N_5	AF22				
5	IO_L37P_5	AE22				
5	IO_L27N_5/VREF_5	AL25	NC	NC		
5	IO_L27P_5	AK25	NC	NC		
5	IO_L26N_5	AJ23	NC	NC		
5	IO_L26P_5	AH23	NC	NC		
5	IO_L25N_5	AH24	NC	NC		
5	IO_L25P_5	AG24	NC	NC		
5	IO_L21N_5	AM26	NC	NC		
5	IO_L21P_5	AL26	NC	NC		
5	IO_L20N_5	AK26	NC	NC		
5	IO_L20P_5	AJ26	NC	NC		
5	IO_L19N_5	AF23	NC	NC		
5	IO_L19P_5	AE23	NC	NC		
5	IO_L09N_5/VREF_5	AL27				
5	IO_L09P_5	AK27				
5	IO_L08N_5	AH25				
5	IO_L08P_5	AG25				
5	IO_L07N_5/VREF_5	AF24				
5	IO_L07P_5	AE24				
5	IO_L06N_5/VRP_5	AM28				
5	IO_L06P_5/VRN_5	AL28				
5	IO_L05_5/No_Pair	AF25				
5	IO_L03N_5/D4	AK28				
5	IO_L03P_5/D5	AK29				
5	IO_L02N_5/D6	AH26				
5	IO_L02P_5/D7	AG26				
5	IO_L01N_5/RDWR_B	AL29				
5	IO_L01P_5/CS_B	AL30				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	TXNPAD11	A7		
N/A	TXPPAD11	A6		
N/A	GNDA11	C6		
N/A	RXPPAD11	A5		
N/A	RXNPAD11	A4		
N/A	VTRXPAD11	B5		
N/A	AVCCAUXRX11	B4		
N/A	AVCCAUXRX14	AV4		
N/A	VTRXPAD14	AV5		
N/A	RXNPAD14	AW4		
N/A	RXPPAD14	AW5		
N/A	GNDA14	AU6		
N/A	TXPPAD14	AW6		
N/A	TXNPAD14	AW7		
N/A	VTTXPAD14	AV7		
N/A	AVCCAUXTX14	AV6		
N/A	AVCCAUXRX16	AV8		
N/A	VTRXPAD16	AV9		
N/A	RXNPAD16	AW8		
N/A	RXPPAD16	AW9		
N/A	GNDA16	AU9		
N/A	TXPPAD16	AW10		
N/A	TXNPAD16	AW11		
N/A	VTTXPAD16	AV11		
N/A	AVCCAUXTX16	AV10		
N/A	AVCCAUXRX17	AV12		
N/A	VTRXPAD17	AV13		
N/A	RXNPAD17	AW12		
N/A	RXPPAD17	AW13		
N/A	GNDA17	AU13		
N/A	TXPPAD17	AW14		
N/A	TXNPAD17	AW15		
N/A	VTTXPAD17	AV15		
N/A	AVCCAUXTX17	AV14		
N/A	AVCCAUXRX18	AV16		
N/A	VTRXPAD18	AV17		
N/A	RXNPAD18	AW16		
N/A	RXPPAD18	AW17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L77N_3		AT3		
3	IO_L77P_3		AT4		
3	IO_L76N_3		AU1		
3	IO_L76P_3		AU2		
3	IO_L75N_3/VREF_3		AU3		
3	IO_L75P_3		AU4		
3	IO_L74N_3		AV3		
3	IO_L74P_3		AW3		
3	IO_L73N_3		AV1		
3	IO_L73P_3		AV2		
3	IO_L06N_3		AW1		
3	IO_L06P_3		AW2		
3	IO_L05N_3		AT8		
3	IO_L05P_3		AU8		
3	IO_L04N_3		AT6		
3	IO_L04P_3		AU7		
3	IO_L03N_3/VREF_3		AY5		
3	IO_L03P_3		AY6		
3	IO_L02N_3		AV7		
3	IO_L02P_3		AW7		
3	IO_L01N_3/VRP_3		AV6		
3	IO_L01P_3/VRN_3		AW6		
4	IO_L01N_4/BUSY/DOUT(1)		AT9		
4	IO_L01P_4/INIT_B		AR9		
4	IO_L02N_4/D0/DIN(1)		AU9		
4	IO_L02P_4/D1		AV9		
4	IO_L03N_4/D2		AY9		
4	IO_L03P_4/D3		AW9		
4	IO_L05_4/No_Pair		AN11		
4	IO_L06N_4/VRP_4		AR10		
4	IO_L06P_4/VRN_4		AP10		
4	IO_L07N_4		AU10		
4	IO_L07P_4/VREF_4		AT10		
4	IO_L08N_4		AV10		
4	IO_L08P_4		AW10		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L09N_4		AR11		
4	IO_L09P_4/VREF_4		AP11		
4	IO_L19N_4		AV11		
4	IO_L19P_4		AU11		
4	IO_L20N_4		AY10		
4	IO_L20P_4		AY11		
4	IO_L21N_4		AN12		
4	IO_L21P_4		AM12		
4	IO_L25N_4		AR12		
4	IO_L25P_4		AP12		
4	IO_L26N_4		AT12		
4	IO_L26P_4		AU12		
4	IO_L27N_4		AW12		
4	IO_L27P_4/VREF_4		AV12		
4	IO_L28N_4		AM13		
4	IO_L28P_4		AL13		
4	IO_L29N_4		AP13		
4	IO_L29P_4		AN13		
4	IO_L30N_4		AT13		
4	IO_L30P_4		AR13		
4	IO_L34N_4		AV13		
4	IO_L34P_4		AU13		
4	IO_L35N_4		AW13		
4	IO_L35P_4		AY13		
4	IO_L36N_4		AL15		
4	IO_L36P_4/VREF_4		AL14		
4	IO_L78N_4		AN14	NC	
4	IO_L78P_4		AM14	NC	
4	IO_L83_4/No_Pair		AR14	NC	
4	IO_L84N_4		AU14	NC	
4	IO_L84P_4		AT14	NC	
4	IO_L85N_4		AW14	NC	
4	IO_L85P_4		AV14	NC	
4	IO_L86N_4		AM15	NC	
4	IO_L86P_4		AN15	NC	
4	IO_L87N_4		AR15	NC	

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	VCCO_3		AD14		
3	VCCO_3		AC15		
3	VCCO_3		AC14		
3	VCCO_3		AC8		
3	VCCO_3		AC5		
3	VCCO_3		AB15		
3	VCCO_3		AB14		
4	VCCO_4		AW18		
4	VCCO_4		AT20		
4	VCCO_4		AT15		
4	VCCO_4		AT11		
4	VCCO_4		AP18		
4	VCCO_4		AP14		
4	VCCO_4		AJ21		
4	VCCO_4		AJ20		
4	VCCO_4		AJ19		
4	VCCO_4		AJ18		
4	VCCO_4		AJ17		
4	VCCO_4		AH21		
4	VCCO_4		AH20		
4	VCCO_4		AH19		
4	VCCO_4		AH18		
5	VCCO_5		AW25		
5	VCCO_5		AT32		
5	VCCO_5		AT28		
5	VCCO_5		AT23		
5	VCCO_5		AP29		
5	VCCO_5		AP25		
5	VCCO_5		AJ26		
5	VCCO_5		AJ25		
5	VCCO_5		AJ24		
5	VCCO_5		AJ23		
5	VCCO_5		AJ22		
5	VCCO_5		AH25		
5	VCCO_5		AH24		
5	VCCO_5		AH23		

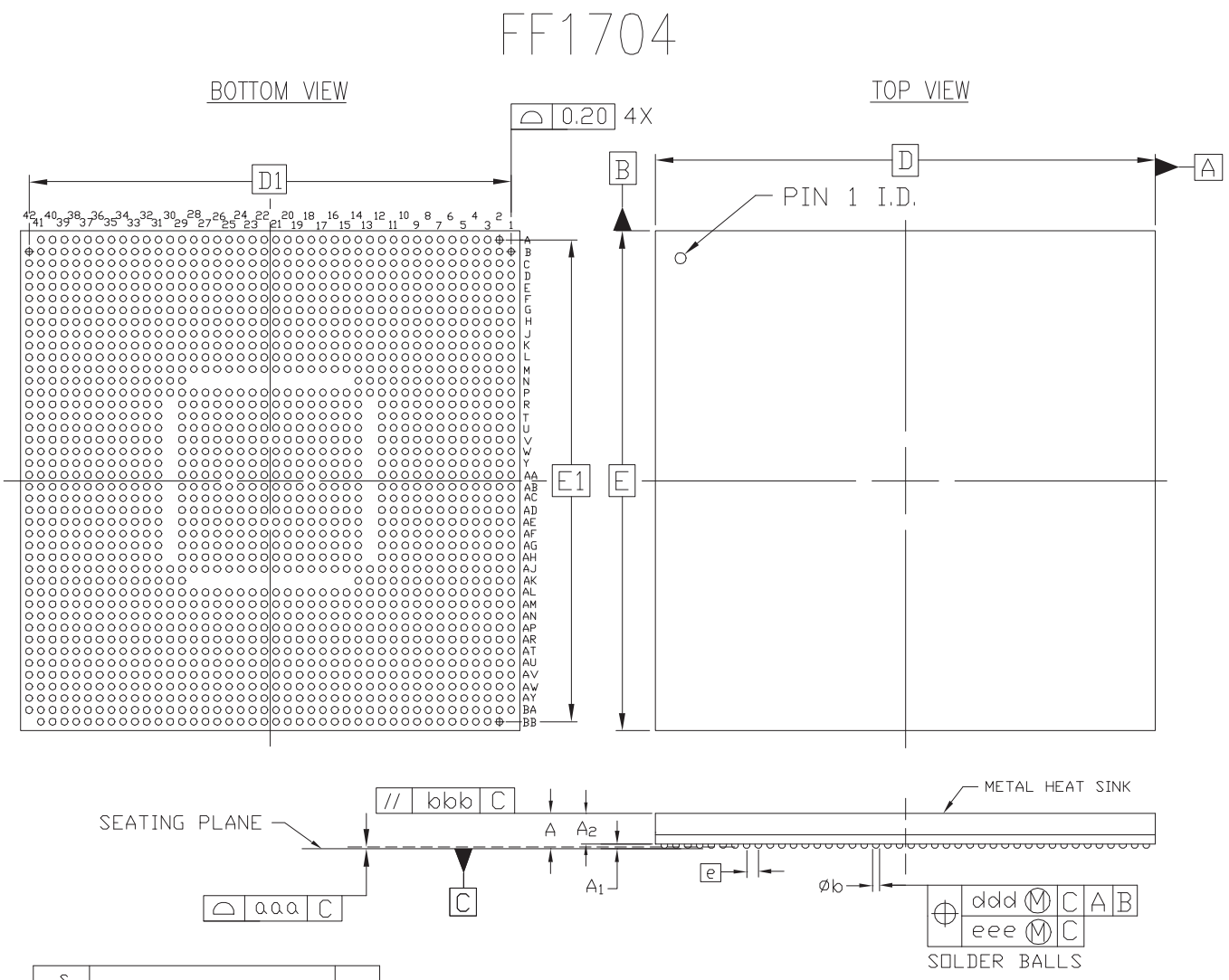
Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AE19		
N/A	GND		AE18		
N/A	GND		AE17		
N/A	GND		AE9		
N/A	GND		AE6		
N/A	GND		AF25		
N/A	GND		AF24		
N/A	GND		AF23		
N/A	GND		AF22		
N/A	GND		AF21		
N/A	GND		AF20		
N/A	GND		AF19		
N/A	GND		AF18		
N/A	GND		AG42		
N/A	GND		AG1		
N/A	GND		AH39		
N/A	GND		AH36		
N/A	GND		AH7		
N/A	GND		AH4		
N/A	GND		AL42		
N/A	GND		AL1		
N/A	GND		AM22		
N/A	GND		AM21		
N/A	GND		AN39		
N/A	GND		AN4		
N/A	GND		AP34		
N/A	GND		AP9		
N/A	GND		AR42		
N/A	GND		AR35		
N/A	GND		AR22		
N/A	GND		AR21		
N/A	GND		AR8		
N/A	GND		AR1		
N/A	GND		AT36		
N/A	GND		AT7		
N/A	GND		AU37		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AU25		
N/A	GND		AU18		
N/A	GND		AU6		
N/A	GND		AV38		
N/A	GND		AV22		
N/A	GND		AV21		
N/A	GND		AV5		
N/A	GND		AW39		
N/A	GND		AW32		
N/A	GND		AW28		
N/A	GND		AW15		
N/A	GND		AW11		
N/A	GND		AW4		
N/A	GND		AY42		
N/A	GND		AY41		
N/A	GND		AY40		
N/A	GND		AY3		
N/A	GND		AY2		
N/A	GND		AY1		
N/A	GND		BA42		
N/A	GND		BA1		
N/A	GND		AA38		
N/A	GND		AA35		
N/A	GND		AA32		
N/A	GND		AA26		
N/A	GND		AA25		
N/A	GND		AA24		
N/A	GND		AA23		
N/A	GND		AA22		
N/A	GND		AA21		
N/A	GND		AA20		
N/A	GND		AA19		
N/A	GND		AA18		
N/A	GND		AA17		
N/A	GND		AA11		
N/A	GND		AA8		

FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	
A_1	0.40	0.50	0.60	
A_2			2.85	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

Figure 9: **FF1704 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L67P_0	J22	
0	IO_L68N_0	K23	
0	IO_L68P_0	L23	
0	IO_L69N_0	F22	
0	IO_L69P_0/VREF_0	G22	
0	IO_L73N_0	D22	
0	IO_L73P_0	E22	
0	IO_L74N_0/GCLK7P	K22	
0	IO_L74P_0/GCLK6S	L22	
0	IO_L75N_0/GCLK5P	B22	
0	IO_L75P_0/GCLK4S	C22	
1	IO_L75N_1/GCLK3P	C21	
1	IO_L75P_1/GCLK2S	B21	
1	IO_L74N_1/GCLK1P	L21	
1	IO_L74P_1/GCLK0S	K21	
1	IO_L73N_1	E21	
1	IO_L73P_1	D21	
1	IO_L69N_1/VREF_1	G21	
1	IO_L69P_1	F21	
1	IO_L68N_1	L20	
1	IO_L68P_1	K20	
1	IO_L67N_1	J21	
1	IO_L67P_1	H21	
1	IO_L66N_1/VREF_1	C20	
1	IO_L66P_1	B20	
1	IO_L65N_1	M20	
1	IO_L65P_1	M21	
1	IO_L64N_1	G20	
1	IO_L64P_1	F20	
1	IO_L60N_1	B19	
1	IO_L60P_1	A19	
1	IO_L59N_1	K19	
1	IO_L59P_1	J19	
1	IO_L58N_1	D19	
1	IO_L58P_1	D20	
1	IO_L57N_1/VREF_1	F19	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	AG26	
N/A	VCCINT	AF26	
N/A	VCCINT	U26	
N/A	VCCINT	T26	
N/A	VCCINT	R26	
N/A	VCCINT	AG25	
N/A	VCCINT	T25	
N/A	VCCINT	AG24	
N/A	VCCINT	T24	
N/A	VCCINT	AG23	
N/A	VCCINT	T23	
N/A	VCCINT	AG22	
N/A	VCCINT	T22	
N/A	VCCINT	AG21	
N/A	VCCINT	T21	
N/A	VCCINT	AG20	
N/A	VCCINT	T20	
N/A	VCCINT	AG19	
N/A	VCCINT	T19	
N/A	VCCINT	AG18	
N/A	VCCINT	T18	
N/A	VCCINT	AH17	
N/A	VCCINT	AG17	
N/A	VCCINT	AF17	
N/A	VCCINT	U17	
N/A	VCCINT	T17	
N/A	VCCINT	R17	
N/A	VCCINT	AJ16	
N/A	VCCINT	AH16	
N/A	VCCINT	AG16	
N/A	VCCINT	AF16	
N/A	VCCINT	AE16	
N/A	VCCINT	AD16	
N/A	VCCINT	AC16	
N/A	VCCINT	AB16	
N/A	VCCINT	AA16	
N/A	VCCINT	Y16	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	W16	
N/A	VCCINT	V16	
N/A	VCCINT	U16	
N/A	VCCINT	T16	
N/A	VCCINT	R16	
N/A	VCCINT	P16	
N/A	VCCINT	AJ15	
N/A	VCCINT	AH15	
N/A	VCCINT	R15	
N/A	VCCINT	P15	
N/A	VCCINT	AJ14	
N/A	VCCINT	P14	
N/A	VCCINT	AK13	
N/A	VCCINT	N13	
N/A	VCCAUX	BA42	
N/A	VCCAUX	AY42	
N/A	VCCAUX	AL42	
N/A	VCCAUX	AB42	
N/A	VCCAUX	AA42	
N/A	VCCAUX	M42	
N/A	VCCAUX	C42	
N/A	VCCAUX	B42	
N/A	VCCAUX	BB41	
N/A	VCCAUX	A41	
N/A	VCCAUX	BB40	
N/A	VCCAUX	A40	
N/A	VCCAUX	BB31	
N/A	VCCAUX	A31	
N/A	VCCAUX	BB22	
N/A	VCCAUX	A22	
N/A	VCCAUX	BB21	
N/A	VCCAUX	A21	
N/A	VCCAUX	BB12	
N/A	VCCAUX	A12	
N/A	VCCAUX	BB3	
N/A	VCCAUX	A3	
N/A	VCCAUX	BB2	