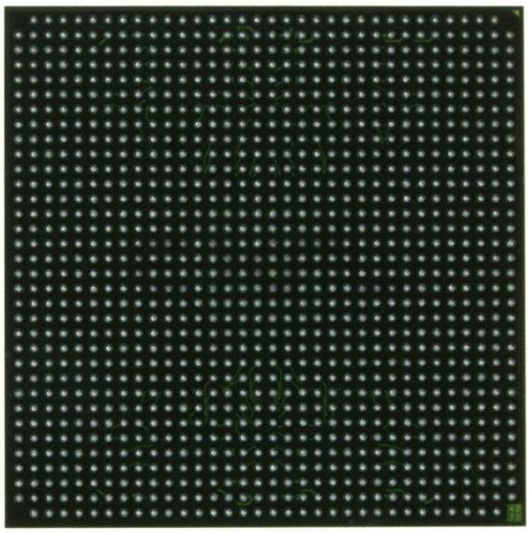
AMD Xilinx - XC2VP40-6FFG1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6ffg1152i

Other RocketIO X Features and Notes

Loopback

In order to facilitate testing without having the need to either apply patterns or measure data at GHz rates, four programmable loop-back features are available.

The first option, serial loopback, is available in two modes: *pre-driver* and *post-driver*.

- The pre-driver mode loops back to the receiver without going through the output driver. In this mode, TXP and TXN are not driven and therefore need not be terminated.
- The post-driver mode is the same as the RocketIO loopback. In this mode, TXP and TXN are driven and must be properly terminated.

The third option, parallel loopback, checks the digital circuitry. When parallel loopback is enabled, the serial loopback path is disabled. However, the transmitter outputs remain active, and data can be transmitted. If TXINHIBIT is asserted, TXP is forced to 0 until TXINHIBIT is de-asserted.

The fourth option, repeater loopback, allows received data to be transmitted without going through the FPGA fabric.

Reset

The receiver and transmitter have their own synchronous reset inputs. The transmitter reset, TXRESET, recenters the transmission FIFO and resets all transmitter registers and the encoder. The receiver reset, RXRESET, recenters the receiver elastic buffer and resets all receiver registers and the decoder. When the signals TXRESET or RXRESET are asserted High, the PCS is in reset. After TXRESET or RXRESET are deasserted, the PCS takes five clocks to come out of reset for each clock domain.

The PMA configuration vector is not affected during this reset, so the PMA speed, filter settings, and so on, all remain the same. Also, the PMA internal pipeline is not affected and continues to operate in normal fashion.

Power

The transceiver voltage regulator circuits must not be shared with any other supplies (including FPGA supplies V_{CCINT}, V_{CCO}, V_{CCAUX}, and V_{REF}). Voltage regulators can be shared among transceiver power supplies of the same voltage, but each supply pin must still have its own separate passive filtering network.

All RocketIO transceivers in the FPGA, whether instantiated in the design or not, must be connected to power and ground. Unused transceivers can be powered by any 1.5V or 2.5V source, and passive filtering is not required.

The Power Down feature is controlled by the transceiver's POWERDOWN input pin. Any given transceiver that is not instantiated in the design is automatically set to the POWERDOWN state by the Xilinx ISE development software. The Power Down pin on the FPGA package has no effect on the MGT.

- Single-cycle and multi-cycle mode option for I-side and D-side interfaces
- Single cycle = one CPU clock cycle; multi-cycle = minimum of two and maximum of eight CPU clock cycles
- FPGA configurable DCR addresses within DSOCM and ISOCM.
- Independent 16 MB logical memory space available within PPC405 memory map for each of the DSOCM and ISOCM. The number of block RAMs in the device might limit the maximum amount of OCM supported.
- Maximum of 64K and 128K bytes addressable from DSOCM and ISOCM interfaces, respectively, using address outputs from OCM directly without additional decoding logic.

Data-Side OCM (DSOCM)

- 32-bit Data Read bus and 32-bit Data Write bus
- Byte write access to DSBRAM support
- Second port of dual port DSBRAM is available to read/write from an FPGA interface
- 22-bit address to DSBRAM port
- 8-bit DCR Registers: DSCNTL, DSARC
- Three alternatives to write into DSBRAM: BRAM initialization, CPU, FPGA H/W using second port

Instruction-Side OCM (ISOCM)

The ISOCM interface contains a 64-bit read only port, for instruction fetches, and a 32-bit write only port, to initialize or test the ISBRAM. When implementing the read only port, the user must deassert the write port inputs. The preferred method of initializing the ISBRAM is through the configuration bitstream.

- 64-bit Data Read Only bus (two instructions per cycle)
- 32-bit Data Write Only bus (through DCR)
- Separate 21-bit address to ISBRAM
- 8-bit DCR Registers: ISCNTL, ISARC
- 32-bit DCR Registers: ISINIT, ISFILL
- Two alternatives to write into ISBRAM: BRAM initialization, DCR and write instruction

Clock/Control Interface Logic

The clock/control interface logic provides proper initialization and connections for PPC405 clock/power management, resets, PLB cycle control, and OCM interfaces. It also couples user signals between the FPGA fabric and the embedded PPC405 CPU core.

The processor clock connectivity is similar to CLB clock pins. It can connect either to global clock nets or general routing resources. Therefore the processor clock source can come from DCM, CLB, or user package pin.

CPU-FPGA Interfaces

All Processor Block user pins link up with the general FPGA routing resources through the CPU-FPGA interface. Therefore processor signals have the same routability as other non-Processor Block user signals. Longlines and hex lines travel across the Processor Block both vertically and horizontally, allowing signals to route through the Processor Block.

Processor Local Bus (PLB) Interfaces

The PPC405 core accesses high-speed system resources through PLB interfaces on the instruction and data cache controllers. The PLB interfaces provide separate 32-bit address/64-bit data buses for the instruction and data sides.

The cache controllers are both PLB masters. PLB arbiters are implemented in the FPGA fabric and are available as soft IP cores.

Device Control Register (DCR) Bus Interface

The device control register (DCR) bus has 10 bits of address space for components external to the PPC405 core. Using the DCR bus to manage status and configuration registers reduces PLB traffic and improves system integrity. System resources on the DCR bus are protected or isolated from wayward code since the DCR bus is not part of the system memory map.

External Interrupt Controller (EIC) Interface

Two level-sensitive user interrupt pins (critical and non-critical) are available. They can be either driven by user defined logic or Xilinx soft interrupt controller IP core outside the Processor Block.

Clock/Power Management (CPM) Interface

The CPM interface supports several methods of clock distribution and power management. Three modes of operation that reduce power consumption below the normal operational level are available.

Reset Interface

There are three user reset input pins (core, chip, and system) and three user reset output pins for different levels of reset, if required.

Debug Interface

Debugging interfaces on the embedded PPC405 core, consisting of the JTAG and Trace ports, offer access to resources internal to the core and assist in software development. The JTAG port provides basic JTAG chip testing functionality as well as the ability for external debug tools to gain control of the processor for debug purposes. The Trace port furnishes programmers with a mechanism for acquiring instruction execution traces.

The JTAG port is compatible with IEEE Std 1149.1, which defines a test access port (TAP) and Boundary-Scan architecture. Extensions to the JTAG interface provide debuggers with processor control that includes stopping, starting, and stepping the PPC405 core. These extensions are compliant with the IEEE 1149.1 specifications for vendor-specific extensions.

Clock Distribution Switching Characteristics

Table 41: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Global Clock Buffer I input to O output	T_{GIO}	0.05	0.057	0.064	ns, max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.49/–0.10	0.54/–0.12	0.60/–0.13	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 34 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 42: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.28	0.32	0.36	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.59	0.65	0.73	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.63	0.70	0.79	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.29	0.32	0.36	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}	0.29	0.32	0.36	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}	0.29	0.32	0.36	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.11	0.13	0.14	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.23	0.24	0.27	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.37	0.38	0.42	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.57	0.64	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.21/–0.04	0.24/–0.05	0.27/–0.06	ns, min
DY inputs	T_{DYCK}/T_{CKDY}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
DX inputs	T_{DXCK}/T_{CKDX}	0.00/ 0.12	0.00/ 0.14	0.00/ 0.15	ns, min
CE input	T_{CECK}/T_{CKCE}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}	0.55/–0.01	0.60/–0.01	0.78/–0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.37	0.40	0.45	ns, min
Minimum Pulse Width, Low	T_{CL}	0.37	0.40	0.45	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.09	1.25	1.40	ns, max
Toggle Frequency (for export control)	F_{TOG}	1350	1200	1050	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 56: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2	1.80/–0.44	1.85/–0.41	1.96/–0.43	ns
		XC2VP4	1.82/–0.53	1.83/–0.31	1.90/–0.29	ns
		XC2VP7	1.80/–0.34	1.81/–0.24	1.88/–0.19	ns
		XC2VP20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VPX20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VP30	1.75/–0.22	1.92/–0.26	1.99/–0.23	ns
		XC2VP40	2.25/–0.54	2.40/–0.56	2.49/–0.54	ns
		XC2VP50	2.93/–1.02	2.98/–0.93	3.00/–0.83	ns
		XC2VP70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VPX70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VP100	N/A	5.58/–2.35	5.60/–2.35	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 5, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L55N_0	G12			
0	IO_L55P_0	F12			
0	IO_L57N_0	E12			
0	IO_L57P_0/VREF_0	F13			
0	IO_L67N_0	D12			
0	IO_L67P_0	C12			
0	IO_L69N_0	J13			
0	IO_L69P_0/VREF_0	H13			
0	IO_L74N_0/GCLK7P	E13			
0	IO_L74P_0/GCLK6S	D13			
0	IO_L75N_0/GCLK5P	C13			
0	IO_L75P_0/GCLK4S	B13			
1	IO_L75N_1/GCLK3P	B14			
1	IO_L75P_1/GCLK2S	C14			
1	IO_L74N_1/GCLK1P	D14			
1	IO_L74P_1/GCLK0S	E14			
1	IO_L69N_1/VREF_1	H14			
1	IO_L69P_1	J14			
1	IO_L67N_1	C15			
1	IO_L67P_1	D15			
1	IO_L57N_1/VREF_1	F14			
1	IO_L57P_1	E15			
1	IO_L55N_1	F15			
1	IO_L55P_1	G15			
1	IO_L54N_1	H15			
1	IO_L54P_1	J15			
1	IO_L53_1/No_Pair	F16			
1	IO_L50_1/No_Pair	G16			
1	IO_L49N_1	C17			
1	IO_L49P_1	D17			
1	IO_L48N_1	E16			
1	IO_L48P_1	E17			
1	IO_L46N_1	H16			
1	IO_L46P_1	H17			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	AVCCAUXRX21	AE7			
N/A	VTRXPAD21	AE6			
N/A	RXNPAD21	AF7			
N/A	RXPPAD21	AF6			
N/A	GNDA21	AD6			
N/A	TXPPAD21	AF5			
N/A	TXNPAD21	AF4			
N/A	VTTXPAD21	AE4			
N/A	AVCCAUXTX21	AE5			
N/A	M2	AD4			
N/A	M0	AF3			
N/A	M1	AE3			
N/A	TDI	D3			
N/A	VCCINT	G10			
N/A	VCCINT	G13			
N/A	VCCINT	G14			
N/A	VCCINT	G17			
N/A	VCCINT	J9			
N/A	VCCINT	J18			
N/A	VCCINT	K7			
N/A	VCCINT	K10			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K17			
N/A	VCCINT	K20			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	N7			
N/A	VCCINT	N20			
N/A	VCCINT	P7			
N/A	VCCINT	P20			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U7			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L87N_7	M25			
7	IO_L86P_7	M24			
7	IO_L86N_7	M23			
7	IO_L85P_7	M22			
7	IO_L85N_7	M21			
7	IO_L60P_7	N19	NC		
7	IO_L60N_7	M19	NC		
7	IO_L59P_7	L26	NC		
7	IO_L59N_7	L25	NC		
7	IO_L58P_7	L24	NC		
7	IO_L58N_7/VREF_7	L23	NC		
7	IO_L57P_7	L22	NC		
7	IO_L57N_7	L21	NC		
7	IO_L56P_7	M20	NC		
7	IO_L56N_7	L20	NC		
7	IO_L55P_7	L19	NC		
7	IO_L55N_7	K20	NC		
7	IO_L54P_7	K26	NC		
7	IO_L54N_7	J26	NC		
7	IO_L53P_7	K24	NC		
7	IO_L53N_7	K23	NC		
7	IO_L52P_7	K22	NC		
7	IO_L52N_7/VREF_7	K21	NC		
7	IO_L51P_7	J25	NC		
7	IO_L51N_7	J24	NC		
7	IO_L50P_7	J23	NC		
7	IO_L50N_7	J22	NC		
7	IO_L49P_7	J21	NC		
7	IO_L49N_7	J20	NC		
7	IO_L48P_7	H26	NC		
7	IO_L48N_7	H25	NC		
7	IO_L47P_7	H24	NC		
7	IO_L47N_7	H23	NC		
7	IO_L46P_7	H22	NC		
7	IO_L46N_7/VREF_7	H21	NC		
7	IO_L45P_7	G26	NC		
7	IO_L45N_7	F26	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L59N_2		P8			
2	IO_L59P_2		P7			
2	IO_L60N_2		N4			
2	IO_L60P_2		N3			
2	IO_L85N_2		P3			
2	IO_L85P_2		P2			
2	IO_L86N_2		R8			
2	IO_L86P_2		R7			
2	IO_L87N_2		P5			
2	IO_L87P_2		P4			
2	IO_L88N_2/VREF_2		R2			
2	IO_L88P_2		T2			
2	IO_L89N_2		R6			
2	IO_L89P_2		R5			
2	IO_L90N_2		R4			
2	IO_L90P_2		R3			
3	IO_L90N_3		U1			
3	IO_L90P_3		V1			
3	IO_L89N_3		T5			
3	IO_L89P_3		T6			
3	IO_L88N_3		T3			
3	IO_L88P_3		T4			
3	IO_L87N_3/VREF_3		U2			
3	IO_L87P_3		U3			
3	IO_L86N_3		T7			
3	IO_L86P_3		T8			
3	IO_L85N_3		U4			
3	IO_L85P_3		U5			
3	IO_L60N_3		V2			
3	IO_L60P_3		W2			
3	IO_L59N_3		T9			
3	IO_L59P_3		U9			
3	IO_L58N_3		V3			
3	IO_L58P_3		V4			
3	IO_L57N_3/VREF_3		W1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		C14			
N/A	GND		C3			
N/A	GND		B29			
N/A	GND		B2			
N/A	GND		A22			
N/A	GND		A9			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
5	IO_L44N_5	AK22				
5	IO_L44P_5	AJ22				
5	IO_L43N_5	AF21				
5	IO_L43P_5	AE21				
5	IO_L39N_5	AK24				
5	IO_L39P_5	AJ24				
5	IO_L38N_5	AH22				
5	IO_L38P_5	AG22				
5	IO_L37N_5	AF22				
5	IO_L37P_5	AE22				
5	IO_L27N_5/VREF_5	AL25	NC	NC		
5	IO_L27P_5	AK25	NC	NC		
5	IO_L26N_5	AJ23	NC	NC		
5	IO_L26P_5	AH23	NC	NC		
5	IO_L25N_5	AH24	NC	NC		
5	IO_L25P_5	AG24	NC	NC		
5	IO_L21N_5	AM26	NC	NC		
5	IO_L21P_5	AL26	NC	NC		
5	IO_L20N_5	AK26	NC	NC		
5	IO_L20P_5	AJ26	NC	NC		
5	IO_L19N_5	AF23	NC	NC		
5	IO_L19P_5	AE23	NC	NC		
5	IO_L09N_5/VREF_5	AL27				
5	IO_L09P_5	AK27				
5	IO_L08N_5	AH25				
5	IO_L08P_5	AG25				
5	IO_L07N_5/VREF_5	AF24				
5	IO_L07P_5	AE24				
5	IO_L06N_5/VRP_5	AM28				
5	IO_L06P_5/VRN_5	AL28				
5	IO_L05_5/No_Pair	AF25				
5	IO_L03N_5/D4	AK28				
5	IO_L03P_5/D5	AK29				
5	IO_L02N_5/D6	AH26				
5	IO_L02P_5/D7	AG26				
5	IO_L01N_5/RDWR_B	AL29				
5	IO_L01P_5/CS_B	AL30				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L55N_3	Y1		
3	IO_L55P_3	Y2		
3	IO_L54N_3	AA5		
3	IO_L54P_3	AA6		
3	IO_L53N_3	Y10		
3	IO_L53P_3	Y11		
3	IO_L52N_3	AA4		
3	IO_L52P_3	AB4		
3	IO_L51N_3/VREF_3	AA1		
3	IO_L51P_3	AA2		
3	IO_L50N_3	Y9		
3	IO_L50P_3	AA9		
3	IO_L49N_3	AB6		
3	IO_L49P_3	AB7		
3	IO_L48N_3	AB2		
3	IO_L48P_3	AB3		
3	IO_L47N_3	AA10		
3	IO_L47P_3	AA11		
3	IO_L46N_3	AC5		
3	IO_L46P_3	AC6		
3	IO_L45N_3/VREF_3	AC3		
3	IO_L45P_3	AC4		
3	IO_L44N_3	AA7		
3	IO_L44P_3	AA8		
3	IO_L43N_3	AC1		
3	IO_L43P_3	AC2		
3	IO_L42N_3	AD5		
3	IO_L42P_3	AD6		
3	IO_L41N_3	AB10		
3	IO_L41P_3	AB11		
3	IO_L40N_3	AD3		
3	IO_L40P_3	AE3		
3	IO_L39N_3/VREF_3	AD1		
3	IO_L39P_3	AD2		
3	IO_L38N_3	AB8		
3	IO_L38P_3	AC7		
3	IO_L37N_3	AE5		
3	IO_L37P_3	AE6		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L17N_3	AH9		
3	IO_L17P_3	AJ9		
3	IO_L16N_3	AK7		
3	IO_L16P_3	AL7		
3	IO_L15N_3/VREF_3	AK4		
3	IO_L15P_3	AL4		
3	IO_L14N_3	AJ7		
3	IO_L14P_3	AJ8		
3	IO_L13N_3	AK3		
3	IO_L13P_3	AL3		
3	IO_L12N_3	AL5		
3	IO_L12P_3	AL6		
3	IO_L11N_3	AK8		
3	IO_L11P_3	AL8		
3	IO_L10N_3	AL1		
3	IO_L10P_3	AL2		
3	IO_L09N_3/VREF_3	AM6		
3	IO_L09P_3	AM7		
3	IO_L08N_3	AL9		
3	IO_L08P_3	AM9		
3	IO_L07N_3	AM5		
3	IO_L07P_3	AN5		
3	IO_L06N_3	AM1		
3	IO_L06P_3	AM2		
3	IO_L05N_3	AN8		
3	IO_L05P_3	AN9		
3	IO_L04N_3	AN6		
3	IO_L04P_3	AP6		
3	IO_L03N_3/VREF_3	AN4		
3	IO_L03P_3	AP4		
3	IO_L02N_3	AN7		
3	IO_L02P_3	AP7		
3	IO_L01N_3/VRP_3	AN3		
3	IO_L01P_3/VRN_3	AP3		
4	IO_L01N_4/BUSY/DOUT(1)	AK10		
4	IO_L01P_4/INIT_B	AJ10		
4	IO_L02N_4/D0/DIN(1)	AF11		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	VCCO_4	AP17		
4	VCCO_4	AK17		
4	VCCO_4	AF17		
4	VCCO_4	AG16		
4	VCCO_4	AF16		
4	VCCO_4	AG15		
4	VCCO_4	AF15		
4	VCCO_4	AG14		
4	VCCO_4	AP13		
4	VCCO_4	AK13		
3	VCCO_3	AE14		
3	VCCO_3	AD14		
3	VCCO_3	AC14		
3	VCCO_3	AB14		
3	VCCO_3	AA14		
3	VCCO_3	Y14		
3	VCCO_3	AF13		
3	VCCO_3	AG12		
3	VCCO_3	AC11		
3	VCCO_3	AP8		
3	VCCO_3	AL8		
3	VCCO_3	AG8		
3	VCCO_3	AC7		
3	VCCO_3	AR4		
3	VCCO_3	AL4		
3	VCCO_3	AG4		
3	VCCO_3	AC3		
3	VCCO_3	AR1		
2	VCCO_2	W14		
2	VCCO_2	V14		
2	VCCO_2	U14		
2	VCCO_2	T14		
2	VCCO_2	R14		
2	VCCO_2	P13		
2	VCCO_2	N12		
2	VCCO_2	U11		
2	VCCO_2	N8		
2	VCCO_2	J8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L76N_6		AU42		
6	IO_L77P_6		AT39		
6	IO_L77N_6		AT40		
6	IO_L78P_6		AT41		
6	IO_L78N_6		AT42		
6	IO_L79P_6		AR38		
6	IO_L79N_6		AR39		
6	IO_L80P_6		AR37		
6	IO_L80N_6		AT38		
6	IO_L81P_6		AR40		
6	IO_L81N_6/VREF_6		AR41		
6	IO_L82P_6		AP36		
6	IO_L82N_6		AP37		
6	IO_L83P_6		AP35		
6	IO_L83N_6		AR36		
6	IO_L84P_6		AP38		
6	IO_L84N_6		AP39		
6	IO_L07P_6		AP41		
6	IO_L07N_6		AP42		
6	IO_L08P_6		AN35		
6	IO_L08N_6		AN36		
6	IO_L09P_6		AN37		
6	IO_L09N_6/VREF_6		AN38		
6	IO_L10P_6		AN41		
6	IO_L10N_6		AN42		
6	IO_L11P_6		AM33		
6	IO_L11N_6		AN34		
6	IO_L12P_6		AM36		
6	IO_L12N_6		AM37		
6	IO_L13P_6		AM38		
6	IO_L13N_6		AM39		
6	IO_L14P_6		AM34		
6	IO_L14N_6		AM35		
6	IO_L15P_6		AN40		
6	IO_L15N_6/VREF_6		AM40		
6	IO_L16P_6		AM41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L38P_3	AE9	
3	IO_L37N_3	AH3	
3	IO_L37P_3	AJ3	
3	IO_L36N_3	AJ1	
3	IO_L36P_3	AJ2	
3	IO_L35N_3	AE6	
3	IO_L35P_3	AE7	
3	IO_L34N_3	AK6	
3	IO_L34P_3	AK7	
3	IO_L33N_3/VREF_3	AK3	
3	IO_L33P_3	AK4	
3	IO_L32N_3	AE12	
3	IO_L32P_3	AF12	
3	IO_L31N_3	AL5	
3	IO_L31P_3	AL6	
3	IO_L30N_3	AL3	
3	IO_L30P_3	AL4	
3	IO_L29N_3	AF10	
3	IO_L29P_3	AF11	
3	IO_L28N_3	AK2	
3	IO_L28P_3	AL2	
3	IO_L27N_3/VREF_3	AL7	
3	IO_L27P_3	AM6	
3	IO_L26N_3	AF7	
3	IO_L26P_3	AF8	
3	IO_L25N_3	AM4	
3	IO_L25P_3	AM5	
3	IO_L24N_3	AM1	
3	IO_L24P_3	AM2	
3	IO_L23N_3	AG10	
3	IO_L23P_3	AG11	
3	IO_L22N_3	AM7	
3	IO_L22P_3	AN7	
3	IO_L21N_3/VREF_3	AN5	
3	IO_L21P_3	AN6	
3	IO_L20N_3	AG8	
3	IO_L20P_3	AG9	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L02P_6	BA34	
6	IO_L02N_6	AY34	
6	IO_L03P_6	BB37	
6	IO_L03N_6/VREF_6	BA37	
6	IO_L04P_6	BB36	
6	IO_L04N_6	BA36	
6	IO_L05P_6	AW34	
6	IO_L05N_6	AW35	
6	IO_L06P_6	BB35	
6	IO_L06N_6	BA35	
6	IO_L73P_6	BA38	
6	IO_L73N_6	AY38	
6	IO_L74P_6	AU34	
6	IO_L74N_6	AT34	
6	IO_L75P_6	AY39	
6	IO_L75N_6/VREF_6	AY40	
6	IO_L76P_6	AY37	
6	IO_L76N_6	AW36	
6	IO_L77P_6	AR34	
6	IO_L77N_6	AR35	
6	IO_L78P_6	AY35	
6	IO_L78N_6	AY36	
6	IO_L79P_6	AW41	
6	IO_L79N_6	AW42	
6	IO_L80P_6	AP35	
6	IO_L80N_6	AN34	
6	IO_L81P_6	AW40	
6	IO_L81N_6/VREF_6	AV40	
6	IO_L82P_6	AW39	
6	IO_L82N_6	AV39	
6	IO_L83P_6	AM34	
6	IO_L83N_6	AM35	
6	IO_L84P_6	AW38	
6	IO_L84N_6	AV37	
6	IO_L61P_6	AV41	
6	IO_L61N_6	AU40	
6	IO_L62P_6	AL34	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	