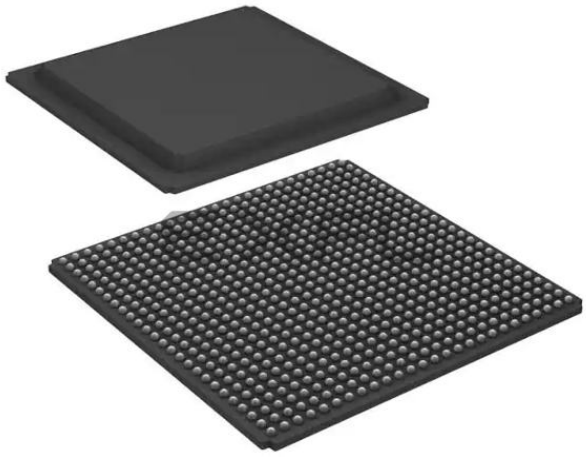

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6fg676c

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II Pro XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 26.

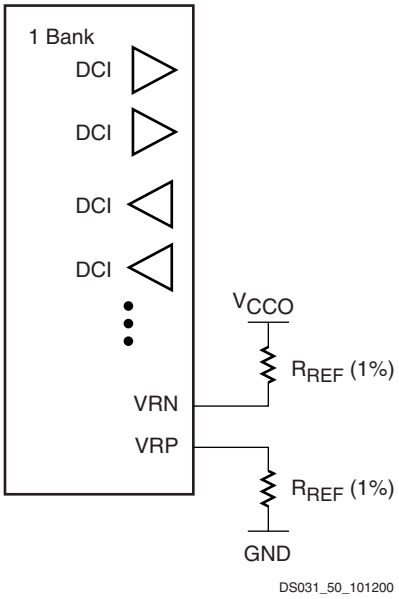


Figure 26: **DCI in a Virtex-II Pro Bank**

When used with a terminated I/O standard, the value of the resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (20Ω to 100Ω). For all series and parallel terminations listed in Table 13 and Table 14, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II Pro input buffers also support LVDCI and LVDCI_DV2.

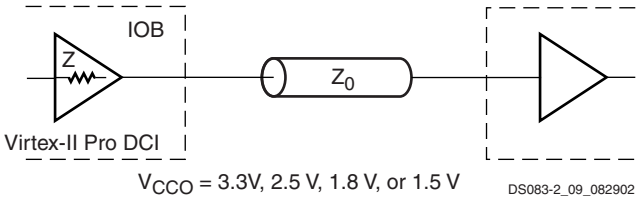


Figure 27: **Internal Series Termination**

Table 13: **SelectIO-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3V	LVDCI_33	N/A
2.5V	LVDCI_25	LVDCI_DV2_25
1.8V	LVDCI_18	LVDCI_DV2_18
1.5V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Terminations (Parallel)

DCI also provides on-chip termination for SSTL2, SSTL18, HSTL (Class I, II, III, or IV), LVDS_25, LVDSEXT_25, and GTL/GTLP receivers or transmitters on bidirectional lines. Table 14 and Table 15 list the on-chip parallel terminations available in Virtex-II Pro devices. V_{CCO} must be set according to Table 10. There is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 14: **SelectIO-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL Class I, 2.5V	SSTL2_I	SSTL2_I_DCI(1)
SSTL Class II, 2.5V	SSTL2_II	SSTL2_II_DCI(1)
SSTL Class I, 1.8V	SSTL18_I	SSTL18_I_DCI
SSTL Class II, 1.8V	SSTL18_II	SSTL18_II_DCI
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class I, 1.8V	HSTL_I_18	HSTL_I_DCI_18
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class II, 1.8V	HSTL_II_18	HSTL_II_DCI_18
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class III, 1.8V	HSTL_III_18	HSTL_III_DCI_18
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
HSTL Class IV, 1.8V	HSTL_IV_18	HSTL_IV_DCI_18
GTL	GTL	GTL_DCI
GTL Plus	GTLP	GTLP_DCI

Notes:
1. SSTL compatible.

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

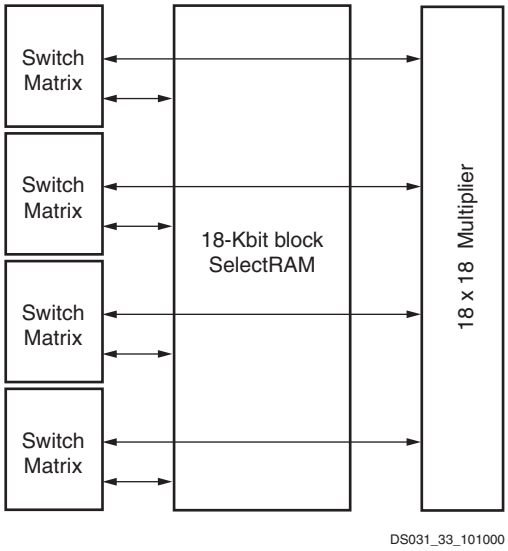


Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

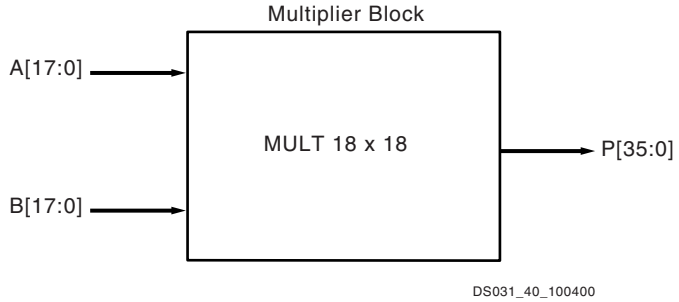


Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Grade	Virtex-II Pro X		Virtex-II Pro		Units
			Min	Max	Min	Max	
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.425	1.575	1.425	1.575	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.425	1.575	1.425	1.575	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	2.375	2.625	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	2.375	2.625	2.375	2.625	V
V_{CCO}(2,3)	Supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.2	3.45(5)	1.2	3.45(5)	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.2	3.45(5)	1.2	3.45(5)	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	GND – 0.2	3.45(5)	GND – 0.2	3.45(5)	V
	3.3V supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	GND – 0.2	3.45(5)	GND – 0.2	3.45(5)	V
	2.5V and below supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	GND – 0.2	V_{CCO} + 0.2	GND – 0.2	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	GND – 0.2	V_{CCO} + 0.2	GND – 0.2	V_{CCO} + 0.2	V
V_{BATT}(4)	Battery voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.0	3.6	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.0	3.6	1.0	3.6	V
AVCCAUXRX(6)	Auxilliary receive supply voltage relative to GNDA	Comm.	1.425(7)	1.575(7)	2.375	2.625	V
		Indus.	1.425(7)	1.575(7)	2.375	2.625	V
AVCCAUXTX(6)	Auxilliary transmit supply voltage relative to GNDA	Comm.	2.375	2.625	2.375	2.625	V
		Indus.	2.375	2.625	2.375	2.625	V
V_{TRX}	Terminal receive supply voltage relative to GND	Comm.	0	2.625	1.6	2.625	V
		Indus.	0	2.625	1.6	2.625	V
V_{TTX}	Terminal transmit supply voltage relative to GND	Comm.	1.425	1.575	1.6	2.625	V
		Indus.	1.425	1.575	1.6	2.625	V

Notes:
1. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. For 3.3V I/O operation, refer to **XAPP659**, available on the Xilinx website at **www.xilinx.com**.
4. If battery is not used, connect V_{BATT} to GND or V_{CCAUX}.
5. For PCI and PCI-X, refer to **XAPP653**, available on the Xilinx website at **www.xilinx.com**.
6. **IMPORTANT!** The RocketIO transceivers have certain power guidelines that must be met, even if unused in the design. Please refer to the section entitled “Powering the RocketIO Transceivers” in the ***RocketIO Transceiver User Guide*** or ***RocketIO X Transceiver User Guide*** for more details.
7. For non-8B/10B-encoded data, the specification for AVCCAUXRX is 1.8V ±5% (1.71 – 1.89V).

RocketIO Switching Characteristics

Table 22: **RocketIO X Reference Clock Switching Characteristics**

			All Speed Grades			
Description	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Reference Clock frequency range(1)	F_{GCLK}		62.5		425	MHz
Reference Clock frequency tolerance	F_{GTOL}				±350	ppm
Reference Clock rise time	T_{RCLK}	20% – 80%		75		ps
Reference Clock fall time	T_{FCLK}	20% – 80%		75		ps
Reference Clock duty cycle	T_{DCREF}		45	50	55	%
Reference Clock total jitter, peak-peak	T_{GJTT}	3.125 Gb/s – 6.25 Gb/s			30	ps
		2.488 Gb/s – 3.125 Gb/s			40	ps
Clock recovery frequency acquisition time, from Power-up to High state of PMARXLOCK	T_{LOCK}			100		µs
Clock recovery phase acquisition time, from Data to High state of PMARXLOCK	T_{PHASE}			40	60	µs

Notes:
1. BREFCLK should be used for all serial bit rates up to the maximum shown.

Table 23: **RocketIO Reference Clock Switching Characteristics**

			All Speed Grades			
Description	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Reference Clock frequency range(1)	F_{GCLK}	Full rate operation	50		156.25	MHz
		Half rate operation(2) (2X oversampling)	60		100	MHz
Reference Clock frequency tolerance	F_{GTOL}				±100	ppm
Reference Clock rise time	T_{RCLK}	20% – 80%		600	1000	ps
Reference Clock fall time	T_{FCLK}	20% – 80%		600	1000	ps
Reference Clock duty cycle	T_{DCREF}		45	50	55	%
Reference Clock total jitter, peak-peak(3)	T_{GJTT}	2.501 Gb/s – 3.125 Gb/s			40	ps
		1.061 Gb/s – 2.5 Gb/s			50	ps
		< 1.06 Gb/s			120	ps
Clock recovery frequency acquisition time	T_{LOCK}				10	µs
Clock recovery phase acquisition time	T_{PHASE}			960		bits(4)

Notes:
1. BREFCLK/BREFCLK2 can be used for all serial bit rates up to the maximum shown. REFCLK/REFCLK2 can be used for serial bit rates up to 2.5 Gb/s (REFCLK = 125 MHz). All other parameters apply equally to REFCLK, REFCLK2, BREFCLK, and BREFCLK2 except as noted.
2. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
3. Measured at the package pin. For reference clock frequencies equal to or above 125 MHz, BREFCLK/BREFCLK2 must be used.
4. 8B/10B-type bitstream.

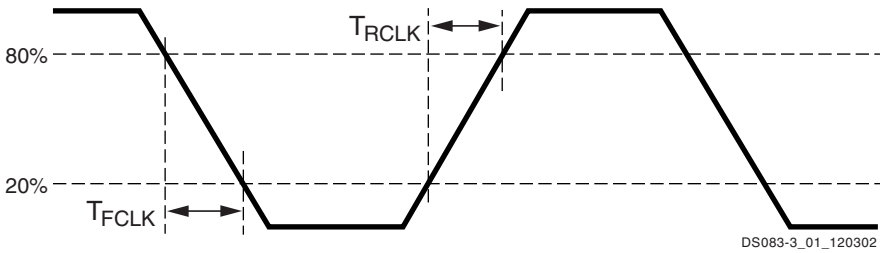


Figure 3: **Reference Clock Timing Parameters**

Table 34: **RocketIO TXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (TXUSRCLK2)					
CONFIGENABLE control input	$T_{GCCK\_}CFGEN/T_{GCKC\_}CFGEN$	0.35/ 0.10	0.35/ 0.10	0.39/ 0.11	ns, min
TXBYPASS8B10B control inputs	$T_{GCCK\_}TBYP/T_{GCKC\_}TBYP$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
TXFORCECRCERR control input	$T_{GCCK\_}TCRCE/T_{GCKC\_}TCRCE$	0.39/ 0.12	0.44/ 0.14	0.49/ 0.15	ns, min
TXPOLARITY control input	$T_{GCCK\_}TPOL/T_{GCKC\_}TPOL$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
TXINHIBIT control inputs	$T_{GCCK\_}TINH/T_{GCKC\_}TINH$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
LOOPBACK control inputs	$T_{GCCK\_}LBK/T_{GCKC\_}LBK$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
TXRESET control input	$T_{GCCK\_}TRST/T_{GCKC\_}TRST$	0.02/ 0.10	0.02/ 0.10	0.02/ 0.11	ns, min
TXCHARISK control inputs	$T_{GCCK\_}TKCH/T_{GCKC\_}TKCH$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
TXCHARDISPMODE control inputs	$T_{GCCK\_}TCDM/T_{GCKC\_}TCDM$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
TXCHARDISPVAL control inputs	$T_{GCCK\_}TCDV/T_{GCKC\_}TCDV$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
CONFIGIN data input	$T_{GDCK\_}CFGIN/T_{GCKD\_}CFGIN$	0.35/ 0.10	0.35/ 0.10	0.39/ 0.11	ns, min
TXDATA data inputs	$T_{GDCK\_}TDAT/T_{GCKD\_}TDAT$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
Clock to Out					
TXBUFERR status output	$T_{GCKST\_}TBERR$	0.54	0.54	0.60	ns, max
TXKERR status outputs	$T_{GCKST\_}TKERR$	0.41	0.41	0.46	ns, max
TXRUNDISP status outputs	$T_{GCKST\_}TRDIS$	0.41	0.41	0.46	ns, max
CONFIGOUT data output	$T_{GCKDO\_}CFGOUT$	0.25	0.25	0.28	ns, max
Clock					
TXUSRCLK2 minimum pulse width, High	$T_{GPWH\_}TX2$	1.42	1.42	2.25	ns, min
TXUSRCLK2 minimum pulse width, Low	$T_{GPWL\_}TX2$	1.42	1.42	2.25	ns, min

Date	Version	Revision
09/15/05	4.4	• Table 2: Added Footnote (7) to AVCCAUXRX for RocketIO X (1.8V for all non-8B/10B-encoded data). • Table 3: - Power dissipation for 10.3125 Gb/s deleted. - Max $I_{CCAUXTX}$ and $I_{CCAUXRX}$ specifications added for Virtex-II Pro. • Table 11: Added specification for minimum p-p differential input voltage. • Table 22: - F_{GCLK}: Changed high end of range to 425 MHz. - T_{GJTT}: Changed measurement units to picoseconds and added maximum specifications for two bit rate ranges. - T_{LOCK}: Changed measurement units to microseconds and adderd typical specification. - T_{PHASE}: Changed measurement units to microseconds and adderd typical and maximum specifications. • Table 24: - All parameters: Deleted specifications for 10.3125 Gb/s. - T_{RJTOL}: Added typical specifications. - T_{JTOL}, T_{SJTOL}, and T_{DDJTOL}: Added typical and maximum specifications. • Table 26: Restructured table. Total Jitter parameter added. All jitter parameters respecified. • Table 28: Restructured table and added new specifications.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Table 15: Removed -7 designations for XC2VPX20 and XC2VPX70 devices.
03/05/07	4.6	*No changes in Module 3 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Changed I_{TRX} typical value in Table 3.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

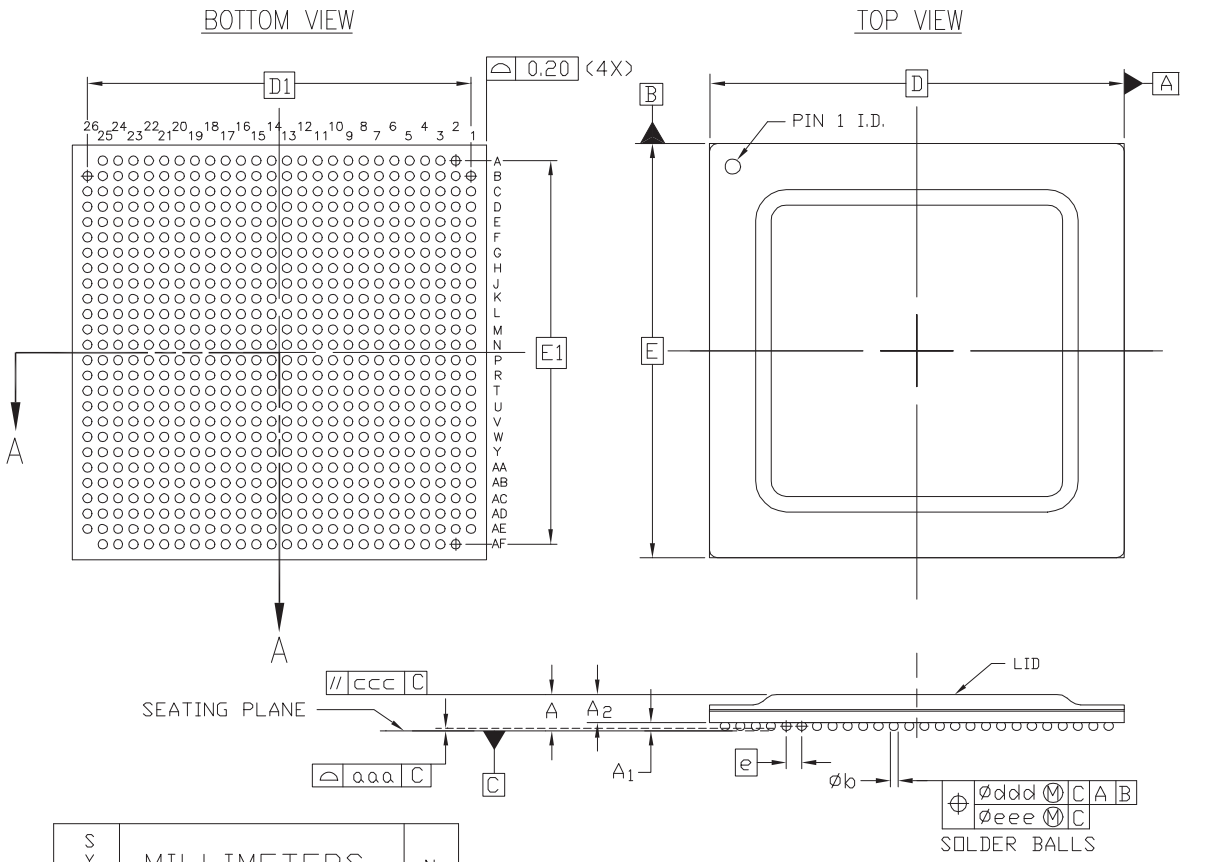
Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/BUSY/DOUT(1)	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0/DIN(1)	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L48N_3	W1	NC		
3	IO_L48P_3	W2	NC		
3	IO_L47N_3	W3	NC		
3	IO_L47P_3	W4	NC		
3	IO_L46N_3	W5	NC		
3	IO_L46P_3	W6	NC		
3	IO_L45N_3/VREF_3	Y1	NC		
3	IO_L45P_3	AA1	NC		
3	IO_L44N_3	Y3	NC		
3	IO_L44P_3	Y4	NC		
3	IO_L43N_3	Y5	NC		
3	IO_L43P_3	Y6	NC		
3	IO_L42N_3	AA2	NC	NC	NC
3	IO_L42P_3	AA3	NC	NC	NC
3	IO_L41N_3	AA4	NC	NC	NC
3	IO_L41P_3	AA5	NC	NC	NC
3	IO_L39N_3/VREF_3	AB1	NC	NC	NC
3	IO_L39P_3	AB2	NC	NC	NC
3	IO_L06N_3	AB3			
3	IO_L06P_3	AB4			
3	IO_L05N_3	AC1			
3	IO_L05P_3	AC2			
3	IO_L04N_3	AD1			
3	IO_L04P_3	AD2			
3	IO_L03N_3/VREF_3	AE1			
3	IO_L03P_3	AF2			
3	IO_L02N_3	AC3			
3	IO_L02P_3	AD4			
3	IO_L01N_3/VRP_3	AE3			
3	IO_L01P_3/VRN_3	AF3			
4	IO_L01N_4/BUSY/DOUT(1)	AC6			
4	IO_L01P_4/INIT_B	AD6			
4	IO_L02N_4/D0/DIN(1)	AB7			
4	IO_L02P_4/D1	AC7			
4	IO_L03N_4/D2	AA7			
4	IO_L03P_4/D3	AA8			

FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		2.45	2.65	
A_1	0.40	0.50	0.60	
A_2			2.15	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

Figure 4: **FF672 Flip-Chip Fine-Pitch BGA Package Specifications**

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 9, XC2VP7, XC2VP20, and XC2VP30 Virtex-II Pro devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	IO_L54N_1		G13	NC		
1	IO_L54P_1		H13	NC		
1	IO_L53_1/No_Pair		A10	NC		
1	IO_L50_1/No_Pair		B10	NC		
1	IO_L49N_1		F14	NC		
1	IO_L49P_1		G14	NC		
1	IO_L48N_1		F12	NC		
1	IO_L48P_1		F11	NC		
1	IO_L47N_1		B9	NC		
1	IO_L47P_1		C9	NC		
1	IO_L46N_1		E13	NC		
1	IO_L46P_1		E12	NC		
1	IO_L45N_1/VREF_1		G12			
1	IO_L45P_1		H12			
1	IO_L44N_1		A8			
1	IO_L44P_1		B8			
1	IO_L43N_1		D11			
1	IO_L43P_1		E11			
1	IO_L39N_1		G11			
1	IO_L39P_1		H11			
1	IO_L38N_1		C8			
1	IO_L38P_1		D8			
1	IO_L37N_1		D10			
1	IO_L37P_1		E10			
1	IO_L09N_1/VREF_1		G10			
1	IO_L09P_1		H10			
1	IO_L08N_1		C7			
1	IO_L08P_1		D7			
1	IO_L07N_1		F10			
1	IO_L07P_1		F9			
1	IO_L06N_1		G9			
1	IO_L06P_1		H9			
1	IO_L05_1/No_Pair		G8			
1	IO_L03N_1/VREF_1		E9			
1	IO_L03P_1		E8			
1	IO_L02N_1		F8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L02P_6		AH26			
6	IO_L02N_6		AG26			
6	IO_L03P_6		AH29			
6	IO_L03N_6/VREF_6		AH30			
6	IO_L04P_6		AH27			
6	IO_L04N_6		AG28			
6	IO_L05P_6		AD25			
6	IO_L05N_6		AD26			
6	IO_L06P_6		AG29			
6	IO_L06N_6		AG30			
6	IO_L31P_6		AF25	NC		
6	IO_L31N_6		AE26	NC		
6	IO_L32P_6		AB23	NC		
6	IO_L32N_6		AB24	NC		
6	IO_L33P_6		AE27	NC		
6	IO_L33N_6/VREF_6		AE28	NC		
6	IO_L34P_6		AF27	NC		
6	IO_L34N_6		AF28	NC		
6	IO_L35P_6		AC25	NC		
6	IO_L35N_6		AC26	NC		
6	IO_L36P_6		AF29	NC		
6	IO_L36N_6		AF30	NC		
6	IO_L37P_6		AD27	NC		
6	IO_L37N_6		AD28	NC		
6	IO_L38P_6		AA23	NC		
6	IO_L38N_6		AA24	NC		
6	IO_L39P_6		AE29	NC		
6	IO_L39N_6/VREF_6		AE30	NC		
6	IO_L40P_6		AB25	NC		
6	IO_L40N_6		AB26	NC		
6	IO_L41P_6		Y23	NC		
6	IO_L41N_6		Y24	NC		
6	IO_L42P_6		AD29	NC		
6	IO_L42N_6		AD30	NC		
6	IO_L43P_6		AC27			
6	IO_L43N_6		AC28			

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L40P_2	K3		
2	IO_L41N_2	R9		
2	IO_L41P_2	P9		
2	IO_L42N_2	K1		
2	IO_L42P_2	K2		
2	IO_L43N_2	L5		
2	IO_L43P_2	L6		
2	IO_L44N_2	P7		
2	IO_L44P_2	P8		
2	IO_L45N_2	L1		
2	IO_L45P_2	L2		
2	IO_L46N_2/VREF_2	M5		
2	IO_L46P_2	M6		
2	IO_L47N_2	R10		
2	IO_L47P_2	R11		
2	IO_L48N_2	M3		
2	IO_L48P_2	M4		
2	IO_L49N_2	M1		
2	IO_L49P_2	M2		
2	IO_L50N_2	R7		
2	IO_L50P_2	T8		
2	IO_L51N_2	P4		
2	IO_L51P_2	N4		
2	IO_L52N_2/VREF_2	N2		
2	IO_L52P_2	N3		
2	IO_L53N_2	T10		
2	IO_L53P_2	T11		
2	IO_L54N_2	P5		
2	IO_L54P_2	P6		
2	IO_L55N_2	R3		
2	IO_L55P_2	P3		
2	IO_L56N_2	T6		
2	IO_L56P_2	T7		
2	IO_L57N_2	P1		
2	IO_L57P_2	P2		
2	IO_L58N_2/VREF_2	R5		
2	IO_L58P_2	R6		
2	IO_L59N_2	U10		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	VCCO_1	H15		
1	VCCO_1	D15		
1	VCCO_1	M14		
1	VCCO_1	M13		
1	VCCO_1	L12		
1	VCCO_1	H11		
1	VCCO_1	D11		
0	VCCO_0	H24		
0	VCCO_0	D24		
0	VCCO_0	L23		
0	VCCO_0	M22		
0	VCCO_0	M21		
0	VCCO_0	M20		
0	VCCO_0	H20		
0	VCCO_0	D20		
0	VCCO_0	M19		
0	VCCO_0	M18		
N/A	CCLK	AG9		
N/A	PROG_B	G26		
N/A	DONE	AF10		
N/A	M0	AG25		
N/A	M1	AG26		
N/A	M2	AF25		
N/A	TCK	G9		
N/A	TDI	F26		
N/A	TDO	F9		
N/A	TMS	H10		
N/A	PWRDWN_B	AG10		
N/A	HSWAP_EN	H25		
N/A	RSVD	H9		
N/A	VBATT	J10		
N/A	DXP	J25		
N/A	DXN	H26		
N/A	VCCINT	AD24		
N/A	VCCINT	L24		
N/A	VCCINT	AC23		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L26P_2		N12		
2	IO_L27N_2		P9		
2	IO_L27P_2		P10		
2	IO_L28N_2/VREF_2		P7		
2	IO_L28P_2		P8		
2	IO_L29N_2		P11		
2	IO_L29P_2		P12		
2	IO_L30N_2		P5		
2	IO_L30P_2		P6		
2	IO_L31N_2		P1		
2	IO_L31P_2		P2		
2	IO_L32N_2		R9		
2	IO_L32P_2		R10		
2	IO_L33N_2		R5		
2	IO_L33P_2		R6		
2	IO_L34N_2/VREF_2		P3		
2	IO_L34P_2		R3		
2	IO_L35N_2		R1		
2	IO_L35P_2		R2		
2	IO_L36N_2		R11		
2	IO_L36P_2		R12		
2	IO_L37N_2		T6		
2	IO_L37P_2		T7		
2	IO_L38N_2		T8		
2	IO_L38P_2		R8		
2	IO_L39N_2		T4		
2	IO_L39P_2		T5		
2	IO_L40N_2/VREF_2		T2		
2	IO_L40P_2		T3		
2	IO_L41N_2		T10		
2	IO_L41P_2		T11		
2	IO_L42N_2		U7		
2	IO_L42P_2		U8		
2	IO_L43N_2		U5		
2	IO_L43P_2		U6		
2	IO_L44N_2		U9		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L44P_2		U10		
2	IO_L45N_2		U3		
2	IO_L45P_2		U4		
2	IO_L46N_2/VREF_2		U1		
2	IO_L46P_2		U2		
2	IO_L47N_2		T12		
2	IO_L47P_2		U12		
2	IO_L48N_2		V10		
2	IO_L48P_2		V11		
2	IO_L49N_2		V7		
2	IO_L49P_2		V8		
2	IO_L50N_2		U11		
2	IO_L50P_2		V12		
2	IO_L51N_2		V4		
2	IO_L51P_2		V5		
2	IO_L52N_2/VREF_2		V1		
2	IO_L52P_2		V2		
2	IO_L53N_2		W9		
2	IO_L53P_2		W10		
2	IO_L54N_2		W7		
2	IO_L54P_2		W8		
2	IO_L55N_2		W5		
2	IO_L55P_2		W6		
2	IO_L56N_2		W11		
2	IO_L56P_2		W12		
2	IO_L57N_2		W3		
2	IO_L57P_2		W4		
2	IO_L58N_2/VREF_2		W1		
2	IO_L58P_2		W2		
2	IO_L59N_2		Y9		
2	IO_L59P_2		Y10		
2	IO_L60N_2		Y6		
2	IO_L60P_2		Y7		
2	IO_L85N_2		Y3		
2	IO_L85P_2		Y4		
2	IO_L86N_2		Y11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L37N_5		AU28		
5	IO_L37P_5		AV28		
5	IO_L87N_5/VREF_5		AP28	NC	
5	IO_L87P_5		AR28	NC	
5	IO_L86N_5		AN28	NC	
5	IO_L86P_5		AM28	NC	
5	IO_L85N_5		AV29	NC	
5	IO_L85P_5		AW29	NC	
5	IO_L84N_5		AT29	NC	
5	IO_L84P_5		AU29	NC	
5	IO_L83_5/No_Pair		AR29	NC	
5	IO_L78N_5		AM29	NC	
5	IO_L78P_5		AN29	NC	
5	IO_L36N_5/VREF_5		AL29		
5	IO_L36P_5		AL28		
5	IO_L35N_5		AY30		
5	IO_L35P_5		AW30		
5	IO_L34N_5		AU30		
5	IO_L34P_5		AV30		
5	IO_L30N_5		AR30		
5	IO_L30P_5		AT30		
5	IO_L29N_5		AN30		
5	IO_L29P_5		AP30		
5	IO_L28N_5		AL30		
5	IO_L28P_5		AM30		
5	IO_L27N_5/VREF_5		AV31		
5	IO_L27P_5		AW31		
5	IO_L26N_5		AU31		
5	IO_L26P_5		AT31		
5	IO_L25N_5		AP31		
5	IO_L25P_5		AR31		
5	IO_L21N_5		AM31		
5	IO_L21P_5		AN31		
5	IO_L20N_5		AY32		
5	IO_L20P_5		AY33		
5	IO_L19N_5		AU32		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCINT		U26		
N/A	VCCINT		U17		
N/A	VCCINT		U16		
N/A	VCCINT		T27		
N/A	VCCINT		T26		
N/A	VCCINT		T25		
N/A	VCCINT		T24		
N/A	VCCINT		T23		
N/A	VCCINT		T22		
N/A	VCCINT		T21		
N/A	VCCINT		T20		
N/A	VCCINT		T19		
N/A	VCCINT		T18		
N/A	VCCINT		T17		
N/A	VCCINT		T16		
N/A	VCCINT		R28		
N/A	VCCINT		R27		
N/A	VCCINT		R26		
N/A	VCCINT		R17		
N/A	VCCINT		R16		
N/A	VCCINT		R15		
N/A	VCCINT		P29		
N/A	VCCINT		P28		
N/A	VCCINT		P27		
N/A	VCCINT		P16		
N/A	VCCINT		P15		
N/A	VCCINT		P14		
N/A	VCCINT		N30		
N/A	VCCINT		N13		
N/A	VCCAUX		AB42		
N/A	VCCAUX		AB41		
N/A	VCCAUX		AB2		
N/A	VCCAUX		AB1		
N/A	VCCAUX		AC42		
N/A	VCCAUX		AC1		
N/A	VCCAUX		AM32		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	