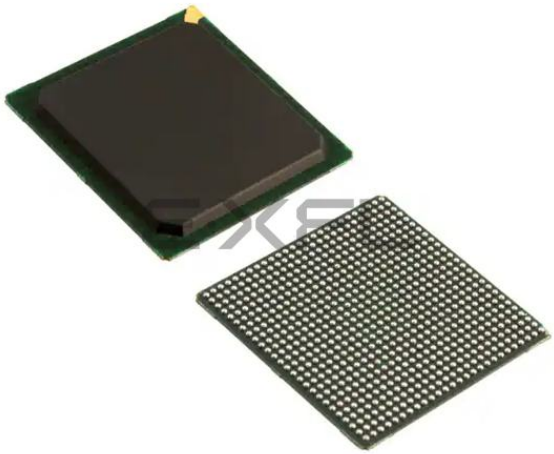

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-6fgg676i

Virtex-II Pro / Virtex-II Pro X Device/Package Combinations and Maximum I/Os

Offerings include ball grid array (BGA) packages with 1.0 mm pitch. In addition to traditional wire-bond interconnect (FG/FGG packages), flip-chip interconnect (FF packages) is used in some of the BGA offerings. Flip-chip interconnect construction supports more I/Os than are possible in wire-bond versions of similar packages, providing a high pin count and excellent power dissipation.

The device/package combination table (Table 3) details the maximum number of user I/Os and RocketIO / RocketIO X MGTs for each device and package using wire-bond or flip-chip technology.

The FF1148 and FF1696 packages have no RocketIO transceivers bonded out. Extra SelectIO-Ultra resources occupy available pins in these packages, resulting in a higher user I/O count. These packages are available for the XC2VP40, XC2VP50, and XC2VP100 devices only.

The I/Os per package count includes all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), VBATT, and the RocketIO / RocketIO X transceiver pins.

Table 3: **Virtex-II Pro Device/Package Combinations and Maximum Number of Available I/Os**

Package(1)	FG256/ FGG256	FG456/ FGG456	FG676	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**
Size (mm)	**17 x 17**	**23 x 23**	**26 x 26**	**27 x 27**	**31 x 31**	**35 x 35**	**35 x 35**	**40 x 40**	**42.5 x 42.5**	**42.5 x 42.5**
XC2VP2	140 / 4	156 / 4		204 / 4						
XC2VP4	140 / 4	248 / 4		348 / 4						
XC2VP7		248 / 8		396 / 8	396 / 8					
XC2VP20			404 / 8		556 / 8	564 / 8				
XC2VPX20					552 / 8(2)					
XC2VP30			416 / 8		556 / 8	644 / 8				
XC2VP40			416 / 8			692 / 12	804 / 0(3)			
XC2VP50						692 / 16	812 / 0(3)	852 / 16		
XC2VP70								964 / 16	996 / 20	
XC2VPX70									992 / 20(2)	
XC2VP100									1,040 / 20	1,164 / 0(3)

Notes:
1. Wirebond packages FG256, FG456, and FG676 are also available in Pb-free versions FGG256, FGG456, and FGG676. See Virtex-II Pro Ordering Examples for details on how to order.
2. Virtex-II Pro X device is equipped with RocketIO X transceiver cores.
3. The RocketIO transceivers in devices in the FF1148 and FF1696 packages are not bonded out to the package pins.

Maximum Performance

Maximum performance of the RocketIO / RocketIO X transceiver and the PowerPC processor block varies, depending on package style and speed grade. See Table 4 for details. Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics contains the rest of the FPGA fabric performance parameters.

Table 4: **Maximum RocketIO / RocketIO X Transceiver and Processor Block Performance**

Device	Speed Grade			Units
	-7(1)	-6	-5	
RocketIO X Transceiver FlipChip (FF)	N/A	6.25(3)	4.25(3)	Gb/s
RocketIO Transceiver FlipChip (FF)	3.125	3.125	2.0	Gb/s
RocketIO Transceiver Wirebond (FG)	2.5	2.5	2.0	Gb/s
PowerPC Processor Block	400(2)	350(2)	300	MHz

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1 to identify dual-processor devices.
3. XC2VPX70 is only available at fixed 4.25 Gb/s baud rate.

Each block SelectRAM+ cell is a fully synchronous memory, as illustrated in Figure 48. The two ports have independent inputs and outputs and are independently clocked.

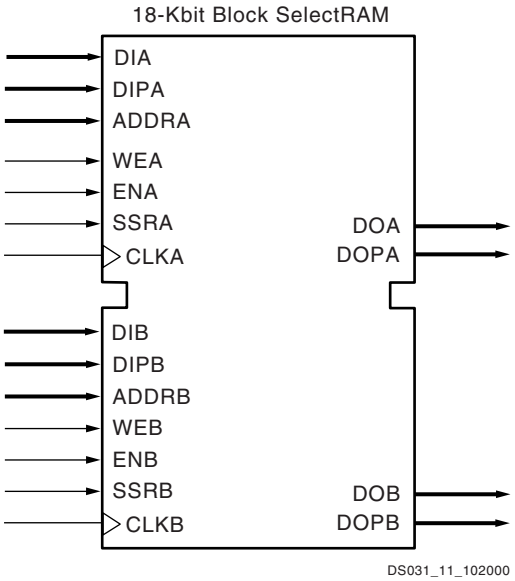

Figure 48: **18 Kb Block SelectRAM+ in Dual-Port Mode**

Port Aspect Ratios

Table 23 shows the depth and the width aspect ratios for the 18 Kb block SelectRAM+ resource. Virtex-II Pro block SelectRAM+ also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM+, and multipliers.

Table 23: **18 Kb Block SelectRAM+ Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II Pro block SelectRAM+ read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **WRITE_FIRST**

   The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO, as shown in Figure 49.

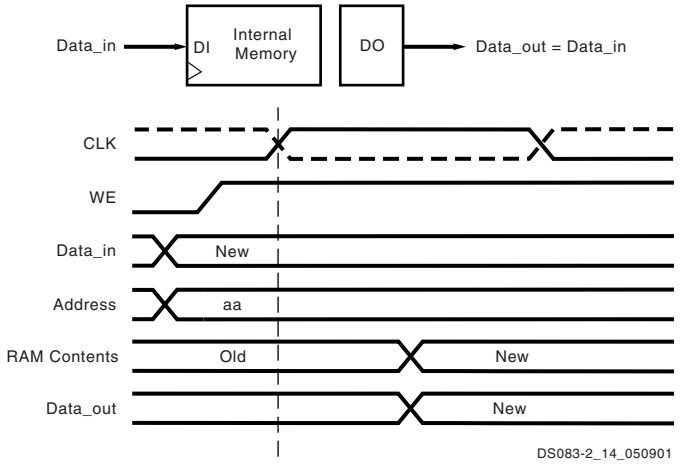

Figure 49: **WRITE_FIRST Mode**

2. **READ_FIRST**

The READ_FIRST option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 50.

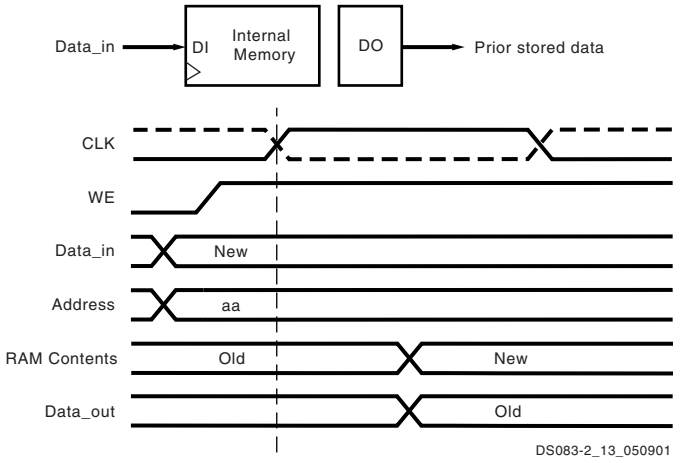

Figure 50: **READ_FIRST Mode**

Table 46: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	1.86/ 0.00	2.06/ 0.00	2.31/ 0.00	ns, max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.23/ 0.00	0.25/ 0.00	0.28/ 0.00	ns, max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.21/–0.09	0.24/–0.09	0.26/–0.10	ns, max
Clock to Output Pin					
Clock to Pin35	T_{MULTCK_P35}	2.45	2.92	3.27	ns, max
Clock to Pin34	T_{MULTCK_P34}	2.36	2.82	3.16	ns, max
Clock to Pin33	T_{MULTCK_P33}	2.28	2.72	3.05	ns, max
Clock to Pin32	T_{MULTCK_P32}	2.20	2.62	2.93	ns, max
Clock to Pin31	T_{MULTCK_P31}	2.12	2.52	2.82	ns, max
Clock to Pin30	T_{MULTCK_P30}	2.03	2.42	2.71	ns, max
Clock to Pin29	T_{MULTCK_P29}	1.95	2.32	2.60	ns, max
Clock to Pin28	T_{MULTCK_P28}	1.87	2.22	2.48	ns, max
Clock to Pin27	T_{MULTCK_P27}	1.79	2.12	2.37	ns, max
Clock to Pin26	T_{MULTCK_P26}	1.70	2.02	2.26	ns, max
Clock to Pin25	T_{MULTCK_P25}	1.62	1.92	2.15	ns, max
Clock to Pin24	T_{MULTCK_P24}	1.54	1.82	2.03	ns, max
Clock to Pin23	T_{MULTCK_P23}	1.46	1.71	1.92	ns, max
Clock to Pin22	T_{MULTCK_P22}	1.37	1.61	1.81	ns, max
Clock to Pin21	T_{MULTCK_P21}	1.29	1.51	1.69	ns, max
Clock to Pin20	T_{MULTCK_P20}	1.21	1.41	1.58	ns, max
Clock to Pin19	T_{MULTCK_P19}	1.13	1.31	1.47	ns, max
Clock to Pin18	T_{MULTCK_P18}	1.04	1.21	1.36	ns, max
Clock to Pin17	T_{MULTCK_P17}	0.96	1.11	1.24	ns, max
Clock to Pin16	T_{MULTCK_P16}	0.88	1.01	1.13	ns, max
Clock to Pin15	T_{MULTCK_P15}	0.80	0.91	1.02	ns, max
Clock to Pin14	T_{MULTCK_P14}	0.71	0.81	0.91	ns, max
Clock to Pin13	T_{MULTCK_P13}	0.63	0.71	0.79	ns, max
Clock to Pin12	T_{MULTCK_P12}	0.63	0.71	0.79	ns, max
Clock to Pin11	T_{MULTCK_P11}	0.63	0.71	0.79	ns, max
Clock to Pin10	T_{MULTCK_P10}	0.63	0.71	0.79	ns, max
Clock to Pin9	T_{MULTCK_P9}	0.63	0.71	0.79	ns, max
Clock to Pin8	T_{MULTCK_P8}	0.63	0.71	0.79	ns, max
Clock to Pin7	T_{MULTCK_P7}	0.63	0.71	0.79	ns, max
Clock to Pin6	T_{MULTCK_P6}	0.63	0.71	0.79	ns, max
Clock to Pin5	T_{MULTCK_P5}	0.63	0.71	0.79	ns, max
Clock to Pin4	T_{MULTCK_P4}	0.63	0.71	0.79	ns, max
Clock to Pin3	T_{MULTCK_P3}	0.63	0.71	0.79	ns, max
Clock to Pin2	T_{MULTCK_P2}	0.63	0.71	0.79	ns, max
Clock to Pin1	T_{MULTCK_P1}	0.63	0.71	0.79	ns, max
Clock to Pin0	T_{MULTCK_P0}	0.63	0.71	0.79	ns, max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 7; corresponding timing characteristics are listed in Table 49.

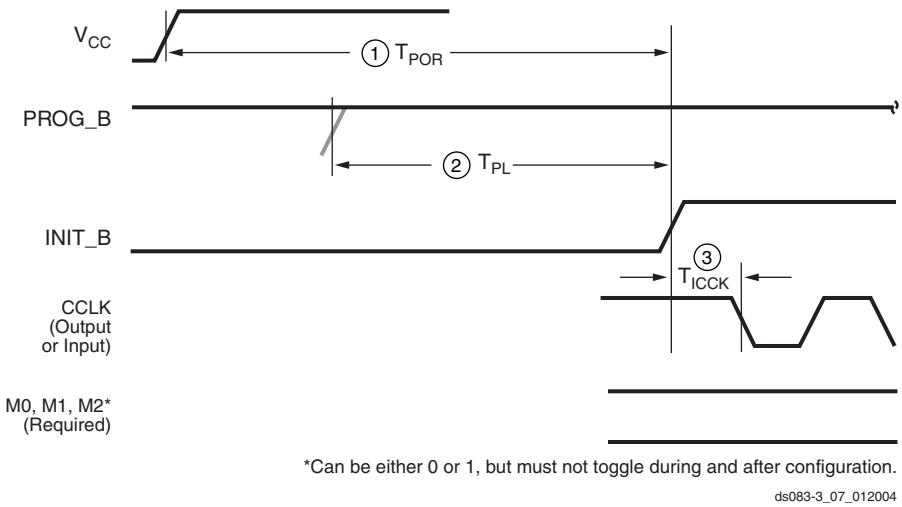

Figure 7: **Configuration Power-Up Timing**

Table 49: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.25	µs, min
			4.00	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 56: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2	1.80/–0.44	1.85/–0.41	1.96/–0.43	ns
		XC2VP4	1.82/–0.53	1.83/–0.31	1.90/–0.29	ns
		XC2VP7	1.80/–0.34	1.81/–0.24	1.88/–0.19	ns
		XC2VP20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VPX20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VP30	1.75/–0.22	1.92/–0.26	1.99/–0.23	ns
		XC2VP40	2.25/–0.54	2.40/–0.56	2.49/–0.54	ns
		XC2VP50	2.93/–1.02	2.98/–0.93	3.00/–0.83	ns
		XC2VP70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VPX70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VP100	N/A	5.58/–2.35	5.60/–2.35	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/BUSY/DOUT(1)	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0/DIN(1)	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 7, XC2VP20, XC2VP30, and XC2VP40 Virtex-II Pro devices are available in the FG676/FGG676 fine-pitch BGA package. The pins in these devices are the same, except for the differences shown in the "No Connects" column. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L01N_0/VRP_0	E5			
0	IO_L01P_0/VRN_0	D5			
0	IO_L02N_0	E6			
0	IO_L02P_0	D6			
0	IO_L03N_0	G7			
0	IO_L03P_0/VREF_0	F7			
0	IO_L05_0/No_Pair	E7			
0	IO_L06N_0	D7			
0	IO_L06P_0	C7			
0	IO_L07N_0	H8			
0	IO_L07P_0	G8			
0	IO_L09N_0	F8			
0	IO_L09P_0/VREF_0	E8			
0	IO_L37N_0	B8			
0	IO_L37P_0	A8			
0	IO_L39N_0	H9			
0	IO_L39P_0	G9			
0	IO_L43N_0	F9			
0	IO_L43P_0	E9			
0	IO_L45N_0	D9			
0	IO_L45P_0/VREF_0	C9			
0	IO_L46N_0	H10			
0	IO_L46P_0	H11			
0	IO_L48N_0	E10			
0	IO_L48P_0	E11			
0	IO_L49N_0	D10			
0	IO_L49P_0	C10			
0	IO_L50_0/No_Pair	G11			
0	IO_L53_0/No_Pair	F11			
0	IO_L54N_0	J12			
0	IO_L54P_0	H12			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AF34				
N/A	GND	B34				
N/A	GND	C1				
N/A	GND	C2				
N/A	GND	C10				
N/A	GND	C16				
N/A	GND	C19				
N/A	GND	C25				
N/A	GND	C33				
N/A	GND	C34				
N/A	GND	D4				
N/A	GND	D31				
N/A	GND	E5				
N/A	GND	E12				
N/A	GND	E23				
N/A	GND	E30				
N/A	GND	F6				
N/A	GND	F29				
N/A	GND	G7				
N/A	GND	G28				
N/A	GND	B1				
N/A	GND	H8				
N/A	GND	H12				
N/A	GND	H15				
N/A	GND	H20				
N/A	GND	J1				
N/A	GND	H27				
N/A	GND	AF1				
N/A	GND	K3				
N/A	GND	K32				
N/A	GND	M5				
N/A	GND	M8				
N/A	GND	M27				
N/A	GND	M30				
N/A	GND	P14				
N/A	GND	P15				
N/A	GND	P16				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	P17				
N/A	GND	P18				
N/A	GND	P19				
N/A	GND	P20				
N/A	GND	P21				
N/A	GND	R8				
N/A	GND	R14				
N/A	GND	R15				
N/A	GND	R16				
N/A	GND	R17				
N/A	GND	R18				
N/A	GND	R19				
N/A	GND	R20				
N/A	GND	R21				
N/A	GND	R27				
N/A	GND	T1				
N/A	GND	T14				
N/A	GND	T15				
N/A	GND	T16				
N/A	GND	T17				
N/A	GND	T18				
N/A	GND	T19				
N/A	GND	T20				
N/A	GND	T21				
N/A	GND	T34				
N/A	GND	U14				
N/A	GND	U15				
N/A	GND	U16				
N/A	GND	U17				
N/A	GND	U18				
N/A	GND	U19				
N/A	GND	U20				
N/A	GND	U21				
N/A	GND	V14				
N/A	GND	V15				
N/A	GND	V16				
N/A	GND	V17				
N/A	GND	V18				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L59P_2	U11		
2	IO_L60N_2	R1		
2	IO_L60P_2	R2		
2	IO_L85N_2	T3		
2	IO_L85P_2	T4		
2	IO_L86N_2	U8		
2	IO_L86P_2	U9		
2	IO_L87N_2	U2		
2	IO_L87P_2	T2		
2	IO_L88N_2/VREF_2	U4		
2	IO_L88P_2	U5		
2	IO_L89N_2	U6		
2	IO_L89P_2	U7		
2	IO_L90N_2	V3		
2	IO_L90P_2	U3		
3	IO_L90N_3	V6		
3	IO_L90P_3	V7		
3	IO_L89N_3	V10		
3	IO_L89P_3	V11		
3	IO_L88N_3	V4		
3	IO_L88P_3	V5		
3	IO_L87N_3/VREF_3	V2		
3	IO_L87P_3	W2		
3	IO_L86N_3	V8		
3	IO_L86P_3	V9		
3	IO_L85N_3	W6		
3	IO_L85P_3	W7		
3	IO_L60N_3	W3		
3	IO_L60P_3	W4		
3	IO_L59N_3	W10		
3	IO_L59P_3	W11		
3	IO_L58N_3	Y5		
3	IO_L58P_3	Y6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	AA3		
3	IO_L56N_3	W8		
3	IO_L56P_3	Y7		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L36N_3	AE4		
3	IO_L36P_3	AF4		
3	IO_L35N_3	AC10		
3	IO_L35P_3	AD10		
3	IO_L34N_3	AE1		
3	IO_L34P_3	AE2		
3	IO_L33N_3/VREF_3	AF6		
3	IO_L33P_3	AF7		
3	IO_L32N_3	AC8		
3	IO_L32P_3	AC9		
3	IO_L31N_3	AF2		
3	IO_L31P_3	AF3		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AG6		
3	IO_L29N_3	AD9		
3	IO_L29P_3	AE9		
3	IO_L28N_3	AG4		
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AG2		
3	IO_L27P_3	AG3		
3	IO_L26N_3	AD7		
3	IO_L26P_3	AE7		
3	IO_L25N_3	AH6		
3	IO_L25P_3	AH7		
3	IO_L24N_3	AH5		
3	IO_L24P_3	AJ5		
3	IO_L23N_3	AE8		
3	IO_L23P_3	AF8		
3	IO_L22N_3	AH1		
3	IO_L22P_3	AH2		
3	IO_L21N_3/VREF_3	AJ6		
3	IO_L21P_3	AK6		
3	IO_L20N_3	AG7		
3	IO_L20P_3	AG8		
3	IO_L19N_3	AJ3		
3	IO_L19P_3	AJ4		
3	IO_L18N_3	AJ1		
3	IO_L18P_3	AJ2		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L51P_7	N31		
7	IO_L51N_7	P31		
7	IO_L50P_7	T27		
7	IO_L50N_7	R28		
7	IO_L49P_7	M33		
7	IO_L49N_7	M34		
7	IO_L48P_7	M31		
7	IO_L48N_7	M32		
7	IO_L47P_7	R24		
7	IO_L47N_7	R25		
7	IO_L46P_7	M29		
7	IO_L46N_7/VREF_7	M30		
7	IO_L45P_7	L33		
7	IO_L45N_7	L34		
7	IO_L44P_7	P27		
7	IO_L44N_7	P28		
7	IO_L43P_7	L29		
7	IO_L43N_7	L30		
7	IO_L42P_7	K33		
7	IO_L42N_7	K34		
7	IO_L41P_7	P26		
7	IO_L41N_7	R26		
7	IO_L40P_7	K32		
7	IO_L40N_7/VREF_7	L32		
7	IO_L39P_7	K29		
7	IO_L39N_7	K30		
7	IO_L38P_7	P24		
7	IO_L38N_7	P25		
7	IO_L37P_7	J32		
7	IO_L37N_7	J33		
7	IO_L36P_7	J31		
7	IO_L36N_7	K31		
7	IO_L35P_7	N28		
7	IO_L35N_7	N29		
7	IO_L34P_7	H32		
7	IO_L34N_7/VREF_7	H33		
7	IO_L33P_7	H29		
7	IO_L33N_7	H30		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AJ7		
3	IO_L27P_3	AJ8		
3	IO_L26N_3	AF8		
3	IO_L26P_3	AF9		
3	IO_L25N_3	AJ5		
3	IO_L25P_3	AJ6		
3	IO_L24N_3	AJ3		
3	IO_L24P_3	AJ4		
3	IO_L23N_3	AF10		
3	IO_L23P_3	AG10		
3	IO_L22N_3	AJ1		
3	IO_L22P_3	AJ2		
3	IO_L21N_3/VREF_3	AK6		
3	IO_L21P_3	AK7		
3	IO_L20N_3	AF11		
3	IO_L20P_3	AF12		
3	IO_L19N_3	AK4		
3	IO_L19P_3	AK5		
3	IO_L18N_3	AK1		
3	IO_L18P_3	AK2		
3	IO_L17N_3	AG9		
3	IO_L17P_3	AH8		
3	IO_L16N_3	AL6		
3	IO_L16P_3	AL7		
3	IO_L15N_3/VREF_3	AK3		
3	IO_L15P_3	AL3		
3	IO_L14N_3	AG11		
3	IO_L14P_3	AH11		
3	IO_L13N_3	AL1		
3	IO_L13P_3	AL2		
3	IO_L12N_3	AM6		
3	IO_L12P_3	AM7		
3	IO_L11N_3	AH10		
3	IO_L11P_3	AJ9		
3	IO_L10N_3	AL5		
3	IO_L10P_3	AM4		
3	IO_L09N_3/VREF_3	AM2		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L27P_7		P33		
7	IO_L27N_7		P34		
7	IO_L26P_7		N31		
7	IO_L26N_7		N32		
7	IO_L25P_7		N41		
7	IO_L25N_7		N42		
7	IO_L24P_7		N39		
7	IO_L24N_7		N40		
7	IO_L23P_7		N33		
7	IO_L23N_7		N34		
7	IO_L22P_7		N37		
7	IO_L22N_7/VREF_7		N38		
7	IO_L21P_7		N35		
7	IO_L21N_7		N36		
7	IO_L20P_7		M38		
7	IO_L20N_7		M39		
7	IO_L19P_7		M40		
7	IO_L19N_7		M41		
7	IO_L18P_7		M33		
7	IO_L18N_7		M34		
7	IO_L17P_7		M31		
7	IO_L17N_7		M32		
7	IO_L16P_7		M35		
7	IO_L16N_7/VREF_7		M36		
7	IO_L15P_7		L41		
7	IO_L15N_7		L42		
7	IO_L14P_7		L39		
7	IO_L14N_7		L38		
7	IO_L13P_7		L40		
7	IO_L13N_7		K40		
7	IO_L12P_7		L36		
7	IO_L12N_7		L37		
7	IO_L11P_7		L34		
7	IO_L11N_7		L35		
7	IO_L10P_7		K42		
7	IO_L10N_7/VREF_7		K41		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L06N_3	BA8	
3	IO_L06P_3	BB8	
3	IO_L05N_3	AW8	
3	IO_L05P_3	AW9	
3	IO_L04N_3	BA7	
3	IO_L04P_3	BB7	
3	IO_L03N_3/VREF_3	BA6	
3	IO_L03P_3	BB6	
3	IO_L02N_3	AY9	
3	IO_L02P_3	BA9	
3	IO_L01N_3/VRP_3	BA4	
3	IO_L01P_3/VRN_3	BB4	
4	IO_L01N_4/BUSY/DOUT(1)	AL11	
4	IO_L01P_4/INIT_B	AL12	
4	IO_L02N_4/D0/DIN(1)	AV10	
4	IO_L02P_4/D1	AU10	
4	IO_L03N_4/D2	AN11	
4	IO_L03P_4/D3	AM11	
4	IO_L05_4/No_Pair	AT10	
4	IO_L06N_4/VRP_4	AY11	
4	IO_L06P_4/VRN_4	AY10	
4	IO_L07N_4	BB10	
4	IO_L07P_4/VREF_4	BA10	
4	IO_L08N_4	AU11	
4	IO_L08P_4	AT11	
4	IO_L09N_4	AR11	
4	IO_L09P_4/VREF_4	AP11	
4	IO_L19N_4	AW11	
4	IO_L19P_4	AV11	
4	IO_L20N_4	BB11	
4	IO_L20P_4	BA11	
4	IO_L21N_4	AN12	
4	IO_L21P_4	AM12	
4	IO_L25N_4	AR13	
4	IO_L25P_4	AT12	
4	IO_L26N_4	AV12	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L87P_7	AA37	
7	IO_L87N_7	AA38	
7	IO_L86P_7	AA33	
7	IO_L86N_7	AA34	
7	IO_L85P_7	Y40	
7	IO_L85N_7	Y41	
7	IO_L60P_7	W41	
7	IO_L60N_7	W42	
7	IO_L59P_7	AA31	
7	IO_L59N_7	AA32	
7	IO_L58P_7	V40	
7	IO_L58N_7/VREF_7	W40	
7	IO_L57P_7	W37	
7	IO_L57N_7	W38	
7	IO_L56P_7	Y36	
7	IO_L56N_7	Y37	
7	IO_L55P_7	V41	
7	IO_L55N_7	V42	
7	IO_L54P_7	V38	
7	IO_L54N_7	V39	
7	IO_L53P_7	Y31	
7	IO_L53N_7	Y32	
7	IO_L52P_7	U40	
7	IO_L52N_7/VREF_7	U41	
7	IO_L51P_7	T40	
7	IO_L51N_7	U39	
7	IO_L50P_7	Y35	
7	IO_L50N_7	W36	
7	IO_L49P_7	T37	
7	IO_L49N_7	U37	
7	IO_L48P_7	T41	
7	IO_L48N_7	T42	
7	IO_L47P_7	Y33	
7	IO_L47N_7	W34	
7	IO_L46P_7	T38	
7	IO_L46N_7/VREF_7	T39	
7	IO_L45P_7	R36	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	BB34	
N/A	GND	AV34	
N/A	GND	AP34	
N/A	GND	AK34	
N/A	GND	AF34	
N/A	GND	AC34	
N/A	GND	Y34	
N/A	GND	U34	
N/A	GND	N34	
N/A	GND	J34	
N/A	GND	E34	
N/A	GND	A34	
N/A	GND	AD31	
N/A	GND	W31	
N/A	GND	BB30	
N/A	GND	AV30	
N/A	GND	AP30	
N/A	GND	J30	
N/A	GND	E30	
N/A	GND	A30	
N/A	GND	BB26	
N/A	GND	AV26	
N/A	GND	AP26	
N/A	GND	AE26	
N/A	GND	AD26	
N/A	GND	AC26	
N/A	GND	AB26	
N/A	GND	AA26	
N/A	GND	Y26	
N/A	GND	W26	
N/A	GND	V26	
N/A	GND	J26	
N/A	GND	E26	
N/A	GND	A26	
N/A	GND	AF25	
N/A	GND	AE25	
N/A	GND	AD25	