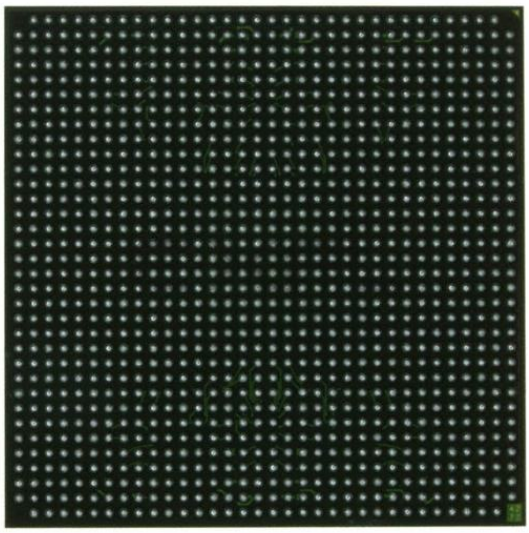

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4848 |
| Number of Logic Elements/Cells | 43632 |
| Total RAM Bits | 3538944 |
| Number of I/O | 692 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp40-7ff1152c |

implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test Boundary-Scan instructions. In test mode, Boundary-Scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

### *Configuration*

Virtex-II Pro / Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Enviornment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See **DS080**, *System ACE CompactFlash Solution* for more information.

### *Readback and Integrated Logic Analyzer*

Configuration data stored in Virtex-II Pro / Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops and latches, distributed SelectRAM+, and block SelectRAM+ memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

## IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro / Virtex-II Pro X by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to **www.xilinx.com/ipcenter** for the latest and most complete list of cores.

### Hardware Cores

- Bus Infrastructure cores (arbiters, bridges, and more)
- Memory cores (DDR, Flash, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

### Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

### Output Swing and Emphasis

The output swing and emphasis levels are fully programmable. Each is controlled via attributes at configuration, and can be modified via the PMA attribute programming bus.

The programmable output swing control can adjust the differential peak-to-peak output level between 200 mV and 1600 mV.

With emphasis, the differential voltage swing is boosted to create a stronger rising or falling waveform. This method compensates for high frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Emphasis can be described from two perspectives, additive to the smaller voltage ($V_{SM}$) (pre-emphasis) or subtractive from the larger voltage ($V_{LG}$) (de-emphasis). The resulting benefits in compensating for channel loss are identical. It is simply a relative way of specifying the effect at the transmitter.

The equations for calculating pre-emphasis as a percentage and dB are as follows:

$$\text{Pre-Emphasis}_{\%} = ((V_{LG}-V_{SM}) / V_{SM}) \times 100$$
$$\text{Pre-Emphasis}_{dB} = 20 \log(V_{LG}/V_{SM})$$

The equations for calculating de-emphasis as a percentage and dB are as follows:

$$\text{De-Emphasis}_{\%} = (V_{LG} - V_{SM}) / V_{LG}) \times 100$$
$$\text{De-Emphasis}_{dB} = 20 \log(V_{SM}/V_{LG})$$

The pre-emphasis amount can be programmed in discrete steps between 0% and 500%. The de-emphasis amount can be programmed in discrete steps between 0% and 83%.

### Serializer

The serializer multiplies the reference frequency provided on REFCLK by 10, 16, 20, 32, or 40, depending on the operation mode. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

### Deserializer

Synchronous serial data reception is facilitated by a clock and data recovery (CDR) circuit. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The CDR circuit extracts both phase and frequency from the incoming data stream.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{10}$, $^1/_{16}$, $^1/_{20}$, $^1/_{32}$, or $^1/_{40}$ the incoming data rate depending on the operating mode.

A sufficient number of transitions must be present in the data stream for CDR to work properly. The CDR circuit is guaranteed to work with 8B/10B and 64B/66B encoding. Further, CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

### Receiver Lock Control

The CDR circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100 ppm of the nominal frequency.

During normal operation, the receiver PLL automatically locks to incoming data (when present) or to the local reference clock (when data is not present). This is the default configuration for all primitives. This function can be overridden via the PMARXLOCKSEL port

When receive PLL lock is forced to the local reference, phase information from the incoming data stream is ignored. Data continues to be sampled, but synchronous to the local reference rather than relative to edges in the data stream.

### Receive Equalization

In addition to transmit emphasis, the RocketIO X MGT provides a programmable active receive equalization feature to further compensate the effects of channel attenuation at high frequencies.

By adjusting RXFER, the right amount of equalization can be added to reverse the signal degradation caused by a printed circuit board, a backplane, or a line/switch card. RXFER can be set through software configuration or the PMA Attribute Bus.

### Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver termination supply ($V_{TRX}$) is the center tap of differential termination to

### Serializer

The serializer multiplies the reference frequency provided on REFCLK by 20. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

### Deserializer

The serial transceiver input is locked to the input data stream through Clock and Data Recovery (CDR), a built-in feature of the RocketIO transceiver. CDR keys off the rising and falling edges of incoming data and derives a clock that is representative of the incoming data rate.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{20}$ the incoming data rate.

A sufficient number of transitions must be present in the data stream for CDR to work properly. CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost. The CDR circuit is guaranteed to work with 8B/10B encoding.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

### Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50Ω (default) or 75Ω impedance, as shown in Figure 11.

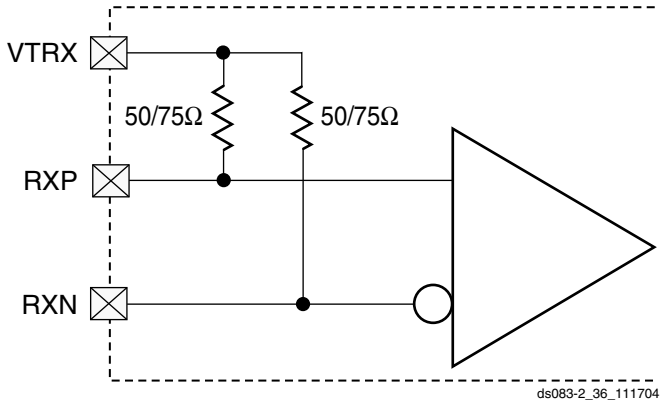


*Figure 11:* **RocketIO Receive Termination**

## PCS

### Fabric Data Interface

Internally, the PCS operates in 2-byte mode (16/20 bits). The FPGA fabric interface can either be 1, 2, or 4 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 5 summarizes the USRCLK2 to USRCLK ratios for the three fabric data widths.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

The Trace port provides instruction execution trace information to an external trace tool. The PPC405 core is capable of back trace and forward trace. Back trace is the tracing of instructions prior to a debug event while forward trace is the tracing of instructions after a debug event.

The processor JTAG port and the FPGA JTAG port can be accessed independently, or the two can be programmatically linked together and accessed via the dedicated FPGA JTAG pins.

For detailed information on the PPC405 JTAG interface, please refer to the "JTAG Interface" section of the **PowerPC 405 Processor Block Reference Guide**

## CoreConnect™ Bus Architecture

The Processor Block is compatible with the CoreConnect™ bus architecture. Any CoreConnect compliant cores including Xilinx soft IP can integrate with the Processor Block through this high-performance bus architecture implemented on FPGA fabric.

The CoreConnect architecture provides three buses for interconnecting Processor Blocks, Xilinx soft IP, third party IP, and custom logic, as shown in Figure 15:

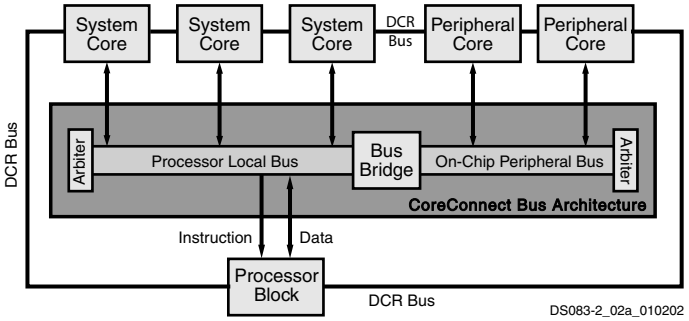


*Figure 15:* **CoreConnect Block Diagram**

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) bus

High-performance peripherals connect to the high-bandwidth, low-latency PLB. Slower peripheral cores connect to the OPB, which reduces traffic on the PLB, resulting in greater overall system performance.

For more information, refer to:
**http://www-3.ibm.com/chips/techlib/techlib.nfs/productfamilies/CoreConnect_Bus_Architecture/**

# Functional Description: Embedded PowerPC 405 Core

This section offers a brief overview of the various functional blocks shown in Figure 16.

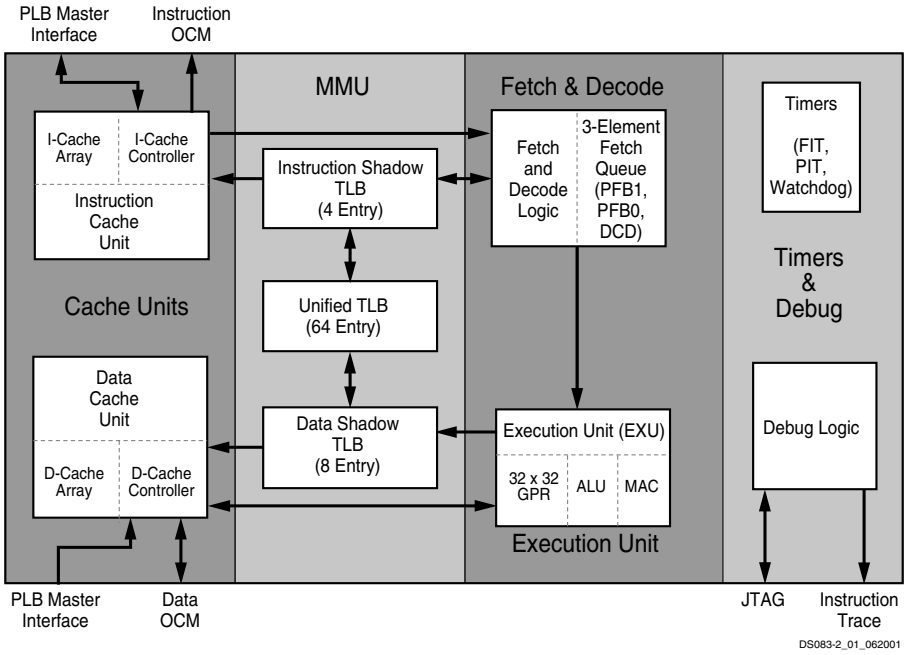


*Figure 16:* **Embedded PPC405 Core Block Diagram**

## Embedded PPC405 Core

The embedded PPC405 core is a 32-bit Harvard architecture processor. Figure 16 illustrates its functional blocks:

- Cache units
- Memory Management unit
- Fetch Decode unit

*Table 9:* **Supported Differential Signal I/O Standards**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Output $V_{OD}$ |
|---|---|---|---|---|
| LDT_25 | 2.5 | N/R | N/R | 0.500 – 0.740 |
| LVDS_25 | 2.5 | N/R | N/R | 0.247 – 0.454 |
| LVDSEXT_25 | 2.5 | N/R | N/R | 0.440 – 0.820 |
| BLVDS_25 | 2.5 | N/R | N/R | 0.250 – 0.450 |
| ULVDS_25 | 2.5 | N/R | N/R | 0.500 – 0.740 |
| LVPECL_25 | 2.5 | N/R | N/R | 0.345 – 1.185 |
| LDT_25_DT(1) | 2.5 | 2.5 | N/R | 0.500 – 0.740 |
| LVDS_25_DT(1) | 2.5 | 2.5 | N/R | 0.247 – 0.454 |
| LVDSEXT_25_DT(1) | 2.5 | 2.5 | N/R | 0.330 – 0.700 |
| ULVDS_25_DT(1) | 2.5 | 2.5 | N/R | 0.500 – 0.740 |

**Notes:**
1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

*Table 10:* **Supported DCI I/O Standards**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Termination Type |
|---|---|---|---|---|
| LVDCI_33(1) | 3.3 | 3.3 | N/R | Series |
| LVDCI_25 | 2.5 | 2.5 | N/R | Series |
| LVDCI_DV2_25 | 2.5 | 2.5 | N/R | Series |
| LVDCI_18 | 1.8 | 1.8 | N/R | Series |
| LVDCI_DV2_18 | 1.8 | 1.8 | N/R | Series |
| LVDCI_15 | 1.5 | 1.5 | N/R | Series |
| LVDCI_DV2_15 | 1.5 | 1.5 | N/R | Series |
| GTL_DCI | 1.2 | 1.2 | 0.8 | Single |
| GTLP_DCI | 1.5 | 1.5 | 1.0 | Single |
| HSTL_I_DCI | 1.5 | 1.5 | 0.75 | Split |
| HSTL_II_DCI | 1.5 | 1.5 | 0.75 | Split |
| HSTL_III_DCI | 1.5 | 1.5 | 0.9 | Single |
| HSTL_IV_DCI | 1.5 | 1.5 | 0.9 | Single |
| HSTL_I_DCI_18 | 1.8 | 1.8 | 0.9 | Split |
| HSTL_II_DCI_18 | 1.8 | 1.8 | 0.9 | Split |
| HSTL_III_DCI_18 | 1.8 | 1.8 | 1.1 | Single |
| HSTL_IV_DCI_18 | 1.8 | 1.8 | 1.1 | Single |
| SSTL2_I_DCI(2) | 2.5 | 2.5 | 1.25 | Split |
| SSTL2_II_DCI(2) | 2.5 | 2.5 | 1.25 | Split |
| SSTL18_I_DCI (3) | 1.8 | 1.8 | 0.9 | Split |
| SSTL18_II_DCI | 1.8 | 1.8 | 0.9 | Split |

*Table 10:* **Supported DCI I/O Standards *(Continued)***

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Termination Type |
|---|---|---|---|---|
| LVDS_25_DCI | 2.5 | 2.5 | N/R | Split |
| LVDSEXT_25_DCI | 2.5 | 2.5 | N/R | Split |

**Notes:**
1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

## Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

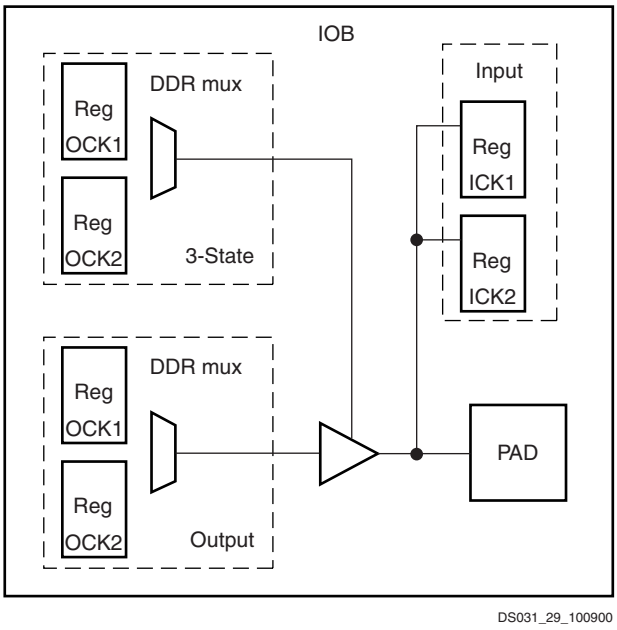


*Figure 19:* **Virtex-II Pro IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

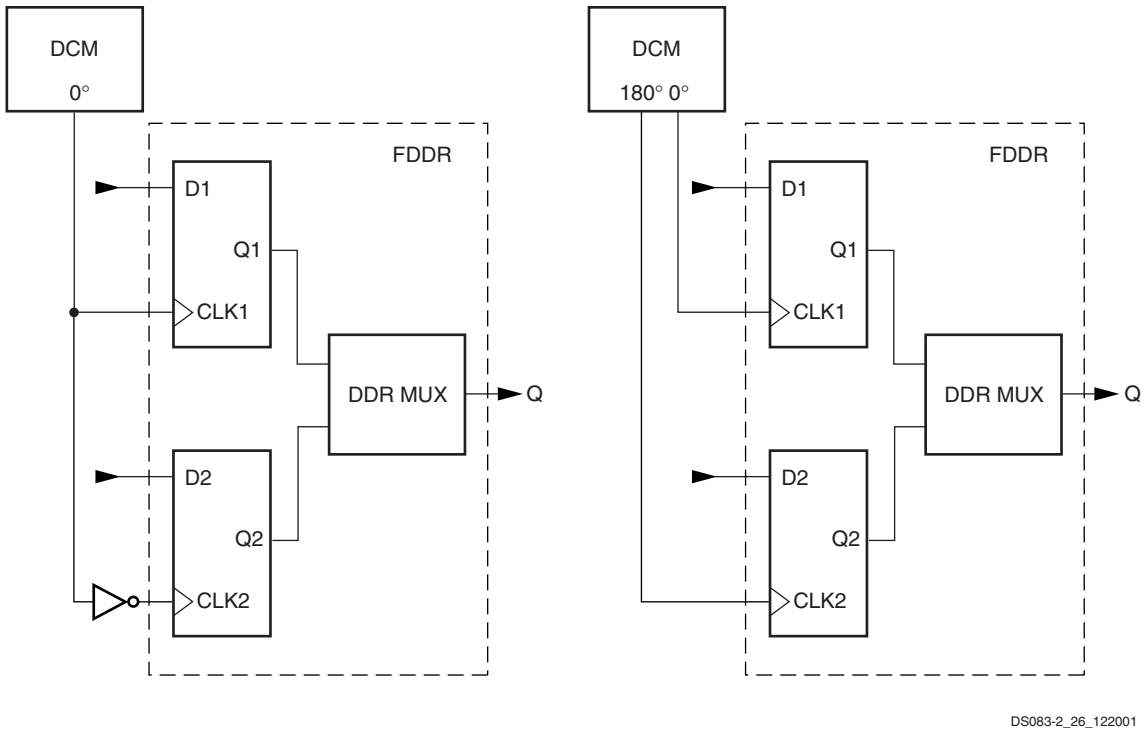


*Figure 20:* **Double Data Rate Registers**

This DDR mechanism can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II Pro devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals). Two neighboring IOBs have a shared routing resource connecting the ICLK and OTCLK pins on pairs of IOBs. If two adjacent IOBs using DDR registers do not share the same clock signals on their clock pins (ICLK1, ICLK2, OTCLK1, and OTCLK2), one of the clock signals will be unroutable.

The IOB pairing is identical to the LVDS IOB pairs. Hence, the package pin-out table can also be used for pin assignment to avoid conflict.

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic 1. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch, independent of all other registers or latches, can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Refer to Figure 21.

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

## Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

### Virtex-II Pro DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description[1] | | Virtex-II Pro X | Virtex-II Pro | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | –0.5 to 1.6 | | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | –0.5 to 3.0 | | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | | –0.5 to 3.75 | | V |
| $V_{BATT}$ | Key memory battery backup supply | | –0.5 to 4.05 | | V |
| $V_{REF}$ | Input reference voltage | | –0.3 to 3.75 | | V |
| $V_{IN}$ | 3.3V I/O input voltage relative to GND (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| $V_{TS}$ | Voltage applied to 3-state 3.3V output (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| AVCCAUXRX | Receive auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 2.0 | –0.5 to 3.0 | V |
| AVCCAUXTX | Transmit auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TRX}$ | Terminal receive supply voltage relative to GND | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TTX}$ | Terminal transmit supply voltage relative to GND | | –0.5 to 1.6 | –0.5 to 3.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | | °C |
| $T_{SOL}$ | Maximum soldering temperature[2] | All regular FG/FF flip-chip packages | +220 | | °C |
| | | Pb-free FGG256 wire-bond package | N/A | +260 | °C |
| | | Pb-free FGG456 and FGG676 wire-bond packages | N/A | +250 | °C |
| $T_J$ | Maximum junction temperature[2] | | +125 | | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

## Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as Virtex-II Pro Switching Characteristics (speed files).

Table 13 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

*Table 13:* **Pin-to-Pin Performance**

| Description | Device Used & Speed Grade | Pin-to-Pin Performance (with I/O Delays) | Units |
|---|---|---|---|
| **Basic Functions:** | | | |
| 16-bit Address Decoder | XC2VP20FF1152-6 | 7.20 | ns |
| 32-bit Address Decoder | XC2VP20FF1152-6 | 8.08 | ns |
| 64-bit Address Decoder | XC2VP20FF1152-6 | 8.15 | ns |
| 4:1 MUX | XC2VP20FF1152-6 | 3.85 | ns |
| 8:1 MUX | XC2VP20FF1152-6 | 7.24 | ns |
| 16:1 MUX | XC2VP20FF1152-6 | 7.30 | ns |
| 32:1 MUX | XC2VP20FF1152-6 | 7.64 | ns |
| Combinatorial (pad to LUT to pad) | XC2VP20FF1152-6 | 3.26 | ns |
| **Memory:** | | | |
| **Block RAM** | | | |
| Pad to setup | XC2VP20FF1152-6 | 1.72 | ns |
| Clock to Pad | XC2VP20FF1152-6 | 6.63 | ns |
| **Distributed RAM** | | | |
| Pad to setup | XC2VP20FF1152-6 | 1.78 | ns |
| Clock to Pad | XC2VP20FF1152-6 | 4.12 | ns |

*Table 46:* **Pipelined Multiplier Switching Characteristics**

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -7 | -6 | -5 | |
| **Setup and Hold Times Before/After Clock** | | | | | |
| Data Inputs | $T_{MULIDCK}/T_{MULCKID}$ | 1.86/ 0.00 | 2.06/ 0.00 | 2.31/ 0.00 | ns, max |
| Clock Enable | $T_{MULIDCK\_CE}/T_{MULCKID\_CE}$ | 0.23/ 0.00 | 0.25/ 0.00 | 0.28/ 0.00 | ns, max |
| Reset | $T_{MULIDCK\_RST}/T_{MULCKID\_RST}$ | 0.21/–0.09 | 0.24/–0.09 | 0.26/–0.10 | ns, max |
| **Clock to Output Pin** | | | | | |
| Clock to Pin35 | $T_{MULTCK\_P35}$ | 2.45 | 2.92 | 3.27 | ns, max |
| Clock to Pin34 | $T_{MULTCK\_P34}$ | 2.36 | 2.82 | 3.16 | ns, max |
| Clock to Pin33 | $T_{MULTCK\_P33}$ | 2.28 | 2.72 | 3.05 | ns, max |
| Clock to Pin32 | $T_{MULTCK\_P32}$ | 2.20 | 2.62 | 2.93 | ns, max |
| Clock to Pin31 | $T_{MULTCK\_P31}$ | 2.12 | 2.52 | 2.82 | ns, max |
| Clock to Pin30 | $T_{MULTCK\_P30}$ | 2.03 | 2.42 | 2.71 | ns, max |
| Clock to Pin29 | $T_{MULTCK\_P29}$ | 1.95 | 2.32 | 2.60 | ns, max |
| Clock to Pin28 | $T_{MULTCK\_P28}$ | 1.87 | 2.22 | 2.48 | ns, max |
| Clock to Pin27 | $T_{MULTCK\_P27}$ | 1.79 | 2.12 | 2.37 | ns, max |
| Clock to Pin26 | $T_{MULTCK\_P26}$ | 1.70 | 2.02 | 2.26 | ns, max |
| Clock to Pin25 | $T_{MULTCK\_P25}$ | 1.62 | 1.92 | 2.15 | ns, max |
| Clock to Pin24 | $T_{MULTCK\_P24}$ | 1.54 | 1.82 | 2.03 | ns, max |
| Clock to Pin23 | $T_{MULTCK\_P23}$ | 1.46 | 1.71 | 1.92 | ns, max |
| Clock to Pin22 | $T_{MULTCK\_P22}$ | 1.37 | 1.61 | 1.81 | ns, max |
| Clock to Pin21 | $T_{MULTCK\_P21}$ | 1.29 | 1.51 | 1.69 | ns, max |
| Clock to Pin20 | $T_{MULTCK\_P20}$ | 1.21 | 1.41 | 1.58 | ns, max |
| Clock to Pin19 | $T_{MULTCK\_P19}$ | 1.13 | 1.31 | 1.47 | ns, max |
| Clock to Pin18 | $T_{MULTCK\_P18}$ | 1.04 | 1.21 | 1.36 | ns, max |
| Clock to Pin17 | $T_{MULTCK\_P17}$ | 0.96 | 1.11 | 1.24 | ns, max |
| Clock to Pin16 | $T_{MULTCK\_P16}$ | 0.88 | 1.01 | 1.13 | ns, max |
| Clock to Pin15 | $T_{MULTCK\_P15}$ | 0.80 | 0.91 | 1.02 | ns, max |
| Clock to Pin14 | $T_{MULTCK\_P14}$ | 0.71 | 0.81 | 0.91 | ns, max |
| Clock to Pin13 | $T_{MULTCK\_P13}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin12 | $T_{MULTCK\_P12}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin11 | $T_{MULTCK\_P11}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin10 | $T_{MULTCK\_P10}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin9 | $T_{MULTCK\_P9}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin8 | $T_{MULTCK\_P8}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin7 | $T_{MULTCK\_P7}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin6 | $T_{MULTCK\_P6}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin5 | $T_{MULTCK\_P5}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin4 | $T_{MULTCK\_P4}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin3 | $T_{MULTCK\_P3}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin2 | $T_{MULTCK\_P2}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin1 | $T_{MULTCK\_P1}$ | 0.63 | 0.71 | 0.79 | ns, max |
| Clock to Pin0 | $T_{MULTCK\_P0}$ | 0.63 | 0.71 | 0.79 | ns, max |

## Input Clock Tolerances

*Table 58:* **Input Clock Tolerances**

| Description | Symbol | Constraints $F_{CLKIN}$ | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | –7 | | –6 | | –5 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| **Input Clock Low/High Pulse Width** | | | | | | | | | |
| PSCLK | PSCLK_PULSE | < 1MHz | 25.00 | | 25.00 | | 25.00 | | ns |
| PSCLK and CLKIN(3) | PSCLK_PULSE and CLKIN_PULSE | 1 – 10 MHz | 25.00 | | 25.00 | | 25.00 | | ns |
| | | 10 – 25 MHz | 10.00 | | 10.00 | | 10.00 | | ns |
| | | 25 – 50 MHz | 5.00 | | 5.00 | | 5.00 | | ns |
| | | 50 – 100 MHz | 3.00 | | 3.00 | | 3.00 | | ns |
| | | 100 – 150 MHz | 2.40 | | 2.40 | | 2.40 | | ns |
| | | 150 – 200 MHz | 2.00 | | 2.00 | | 2.00 | | ns |
| | | 200 – 250 MHz | 1.80 | | 1.80 | | 1.80 | | ns |
| | | 250 – 300 MHz | 1.50 | | 1.50 | | 1.50 | | ns |
| | | 300 – 350 MHz | 1.30 | | 1.30 | | 1.30 | | ns |
| | | 350 – 400 MHz | 1.15 | | 1.15 | | 1.15 | | ns |
| | | > 400 MHz | 1.05 | | 1.05 | | 1.05 | | ns |
| **Input Clock Cycle-Cycle Jitter (Low Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_CYC_JITT_DLL_LF | | | ±300 | | ±300 | | ±300 | ps |
| CLKIN (using CLKFX outputs)(2) | CLKIN_CYC_JITT_FX_LF | | | ±300 | | ±300 | | ±300 | ps |
| **Input Clock Cycle-Cycle Jitter (High Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_CYC_JITT_DLL_HF | | | ±150 | | ±150 | | ±150 | ps |
| CLKIN (using CLKFX outputs)(2) | CLKIN_CYC_JITT_FX_HF | | | ±150 | | ±150 | | ±150 | ps |
| **Input Clock Period Jitter (Low Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_PER_JITT_DLL_LF | | | ±1 | | ±1 | | ±1 | ns |
| CLKIN (using CLKFX outputs)(2) | CLKIN_PER_JITT_FX_LF | | | ±1 | | ±1 | | ±1 | ns |
| **Input Clock Period Jitter (High Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_PER_JITT_DLL_HF | | | ±1 | | ±1 | | ±1 | ns |
| CLKIN (using CLKFX outputs)(2) | CLKIN_PER_JITT_FX_HF | | | ±1 | | ±1 | | ±1 | ns |
| **Feedback Clock Path Delay Variation** | | | | | | | | | |
| CLKFB off-chip feedback | CLKFB_DELAY_VAR_EXT | | | ±1 | | ±1 | | ±1 | ns |

**Notes:**
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

## Miscellaneous Timing Parameters

*Table 61:* **Miscellaneous Timing Parameters**

| Description | Symbol | Constraints $F_{CLKIN}$ | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| **Time Required to Achieve LOCK** | | | | | | |
| Using DLL outputs(1) | LOCK_DLL: | | | | | |
| | LOCK_DLL_60 | > 60MHz | 20.00 | 20.00 | 20.00 | us |
| | LOCK_DLL_50_60 | 50 - 60 MHz | 25.00 | 25.00 | 25.00 | us |
| | LOCK_DLL_40_50 | 40 - 50 MHz | 50.00 | 50.00 | 50.00 | us |
| | LOCK_DLL_30_40 | 30 - 40 MHz | 90.00 | 90.00 | 90.00 | us |
| | LOCK_DLL_24_30 | 24 - 30 MHz | 120.00 | 120.00 | 120.00 | us |
| Using CLKFX outputs | LOCK_FX_MIN | | 10.00 | 10.00 | 10.00 | ms |
| | LOCK_FX_MAX | | 10.00 | 10.00 | 10.00 | ms |
| Additional lock time with fine phase shifting | LOCK_DLL_FINE_SHIFT | | 50.00 | 50.00 | 50.00 | us |
| **Fine Phase Shifting** | | | | | | |
| Absolute shifting range | FINE_SHIFT_RANGE | | 10.00 | 10.00 | 10.00 | ns |
| **Delay Lines** | | | | | | |
| Tap delay resolution | DCM_TAP_MIN | | 30.00 | 30.00 | 30.00 | ps |
| | DCM_TAP_MAX | | 50.00 | 50.00 | 50.00 | ps |

**Notes:**
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

## Frequency Synthesis

*Table 62:* **Frequency Synthesis**

| Attribute | Min | Max |
|---|---|---|
| CLKFX_MULTIPLY | 2 | 32 |
| CLKFX_DIVIDE | 1 | 32 |

## Parameter Cross-Reference

*Table 63:* **Parameter Cross-Reference**

| Libraries Guide | Data Sheet |
|---|---|
| DLL_CLKOUT_{MIN\|MAX}_LF | CLKOUT_FREQ_{1X\|2X\|DV}_LF |
| DFS_CLKOUT_{MIN\|MAX}_LF | CLKOUT_FREQ_FX_LF |
| DLL_CLKIN_{MIN\|MAX}_LF | CLKIN_FREQ_DLL_LF |
| DFS_CLKIN_{MIN\|MAX}_LF | CLKIN_FREQ_FX_LF |
| DLL_CLKOUT_{MIN\|MAX}_HF | CLKOUT_FREQ_{1X\|DV}_HF |
| DFS_CLKOUT_{MIN\|MAX}_HF | CLKOUT_FREQ_FX_HF |
| DLL_CLKIN_{MIN\|MAX}_HF | CLKIN_FREQ_DLL_HF |
| DFS_CLKIN_{MIN\|MAX}_HF | CLKIN_FREQ_FX_HF |

*Table 6:* **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| 7 | IO_L88N_7/VREF_7 | L5 | | | |
| 7 | IO_L86P_7 | L6 | | | |
| 7 | IO_L86N_7 | K6 | | | |
| 7 | IO_L85P_7 | K1 | | | |
| 7 | IO_L85N_7 | K2 | | | |
| 7 | IO_L60P_7 | K3 | NC | | |
| 7 | IO_L60N_7 | K4 | NC | | |
| 7 | IO_L58P_7 | K5 | NC | | |
| 7 | IO_L58N_7/VREF_7 | J5 | NC | | |
| 7 | IO_L56P_7 | J1 | NC | | |
| 7 | IO_L56N_7 | J2 | NC | | |
| 7 | IO_L55P_7 | J3 | NC | | |
| 7 | IO_L55N_7 | J4 | NC | | |
| 7 | IO_L54P_7 | J6 | NC | | |
| 7 | IO_L54N_7 | H5 | NC | | |
| 7 | IO_L52P_7 | H1 | NC | | |
| 7 | IO_L52N_7/VREF_7 | H2 | NC | | |
| 7 | IO_L50P_7 | H3 | NC | | |
| 7 | IO_L50N_7 | H4 | NC | | |
| 7 | IO_L49P_7 | G1 | NC | | |
| 7 | IO_L49N_7 | G2 | NC | | |
| 7 | IO_L48P_7 | G3 | NC | | |
| 7 | IO_L48N_7 | G4 | NC | | |
| 7 | IO_L46P_7 | G5 | NC | | |
| 7 | IO_L46N_7/VREF_7 | F5 | NC | | |
| 7 | IO_L43P_7 | F1 | NC | | |
| 7 | IO_L43N_7 | F2 | NC | | |
| 7 | IO_L06P_7 | F3 | | | |
| 7 | IO_L06N_7 | F4 | | | |
| 7 | IO_L04P_7 | E1 | | | |
| 7 | IO_L04N_7/VREF_7 | E2 | | | |
| 7 | IO_L03P_7 | E3 | | | |
| 7 | IO_L03N_7 | E4 | | | |
| 7 | IO_L02P_7 | D1 | | | |
| 7 | IO_L02N_7 | D2 | | | |
| 7 | IO_L01P_7/VRN_7 | C1 | | | |
| 7 | IO_L01N_7/VRP_7 | C2 | | | |

*Table 6:* **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| N/A | VCCAUX | L1 | | | |
| N/A | VCCAUX | B21 | | | |
| N/A | VCCAUX | B2 | | | |
| N/A | VCCAUX | AB11 | | | |
| N/A | VCCAUX | AA21 | | | |
| N/A | VCCAUX | AA2 | | | |
| N/A | VCCAUX | A12 | | | |
| N/A | GND | Y3 | | | |
| N/A | GND | Y20 | | | |
| N/A | GND | W4 | | | |
| N/A | GND | W19 | | | |
| N/A | GND | V5 | | | |
| N/A | GND | V18 | | | |
| N/A | GND | P9 | | | |
| N/A | GND | P14 | | | |
| N/A | GND | P13 | | | |
| N/A | GND | P12 | | | |
| N/A | GND | P11 | | | |
| N/A | GND | P10 | | | |
| N/A | GND | N9 | | | |
| N/A | GND | N14 | | | |
| N/A | GND | N13 | | | |
| N/A | GND | N12 | | | |
| N/A | GND | N11 | | | |
| N/A | GND | N10 | | | |
| N/A | GND | M9 | | | |
| N/A | GND | M14 | | | |
| N/A | GND | M13 | | | |
| N/A | GND | M12 | | | |
| N/A | GND | M11 | | | |
| N/A | GND | M10 | | | |
| N/A | GND | M1 | | | |
| N/A | GND | L9 | | | |
| N/A | GND | L22 | | | |
| N/A | GND | L14 | | | |
| N/A | GND | L13 | | | |
| N/A | GND | L12 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 6 | IO_L01P_6/VRN_6 | AJ30 | | | | |
| 6 | IO_L01N_6/VRP_6 | AJ31 | | | | |
| 6 | IO_L02P_6 | AJ27 | | | | |
| 6 | IO_L02N_6 | AJ28 | | | | |
| 6 | IO_L03P_6 | AK31 | | | | |
| 6 | IO_L03N_6/VREF_6 | AK32 | | | | |
| 6 | IO_L04P_6 | AH29 | | | | |
| 6 | IO_L04N_6 | AH30 | | | | |
| 6 | IO_L05P_6 | AH27 | | | | |
| 6 | IO_L05N_6 | AG28 | | | | |
| 6 | IO_L06P_6 | AL33 | | | | |
| 6 | IO_L06N_6 | AL34 | | | | |
| 6 | IO_L15P_6 | AG29 | NC | | | |
| 6 | IO_L15N_6/VREF_6 | AG30 | NC | | | |
| 6 | IO_L16P_6 | AK33 | NC | | | |
| 6 | IO_L16N_6 | AK34 | NC | | | |
| 6 | IO_L17P_6 | AF27 | NC | | | |
| 6 | IO_L17N_6 | AF28 | NC | | | |
| 6 | IO_L18P_6 | AJ33 | NC | | | |
| 6 | IO_L18N_6 | AJ34 | NC | | | |
| 6 | IO_L19P_6 | AH31 | NC | | | |
| 6 | IO_L19N_6 | AH32 | NC | | | |
| 6 | IO_L20P_6 | AD25 | NC | | | |
| 6 | IO_L20N_6 | AD26 | NC | | | |
| 6 | IO_L21P_6 | AG31 | NC | | | |
| 6 | IO_L21N_6/VREF_6 | AG32 | NC | | | |
| 6 | IO_L22P_6 | AF29 | NC | | | |
| 6 | IO_L22N_6 | AF30 | NC | | | |
| 6 | IO_L23P_6 | AE27 | NC | | | |
| 6 | IO_L23N_6 | AE28 | NC | | | |
| 6 | IO_L24P_6 | AH33 | NC | | | |
| 6 | IO_L24N_6 | AH34 | NC | | | |
| 6 | IO_L31P_6 | AF31 | | | | |
| 6 | IO_L31N_6 | AF32 | | | | |
| 6 | IO_L32P_6 | AC25 | | | | |
| 6 | IO_L32N_6 | AC26 | | | | |
| 6 | IO_L33P_6 | AG33 | | | | |
| 6 | IO_L33N_6/VREF_6 | AG34 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 2 | IO_L21P_2 | E6 | | |
| 2 | IO_L22N_2/VREF_2 | F7 | | |
| 2 | IO_L22P_2 | F8 | | |
| 2 | IO_L23N_2 | M10 | | |
| 2 | IO_L23P_2 | L10 | | |
| 2 | IO_L24N_2 | G5 | | |
| 2 | IO_L24P_2 | F5 | | |
| 2 | IO_L25N_2 | F3 | | |
| 2 | IO_L25P_2 | F4 | | |
| 2 | IO_L26N_2 | M8 | | |
| 2 | IO_L26P_2 | M9 | | |
| 2 | IO_L27N_2 | F1 | | |
| 2 | IO_L27P_2 | F2 | | |
| 2 | IO_L28N_2/VREF_2 | G6 | | |
| 2 | IO_L28P_2 | G7 | | |
| 2 | IO_L29N_2 | M7 | | |
| 2 | IO_L29P_2 | N8 | | |
| 2 | IO_L30N_2 | G3 | | |
| 2 | IO_L30P_2 | H4 | | |
| 2 | IO_L31N_2 | G1 | | |
| 2 | IO_L31P_2 | G2 | | |
| 2 | IO_L32N_2 | N10 | | |
| 2 | IO_L32P_2 | N11 | | |
| 2 | IO_L33N_2 | H5 | | |
| 2 | IO_L33P_2 | H6 | | |
| 2 | IO_L34N_2/VREF_2 | H2 | | |
| 2 | IO_L34P_2 | H3 | | |
| 2 | IO_L35N_2 | N6 | | |
| 2 | IO_L35P_2 | N7 | | |
| 2 | IO_L36N_2 | K4 | | |
| 2 | IO_L36P_2 | J4 | | |
| 2 | IO_L37N_2 | J2 | | |
| 2 | IO_L37P_2 | J3 | | |
| 2 | IO_L38N_2 | P10 | | |
| 2 | IO_L38P_2 | P11 | | |
| 2 | IO_L39N_2 | K5 | | |
| 2 | IO_L39P_2 | K6 | | |
| 2 | IO_L40N_2/VREF_2 | L3 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 7 | IO_L51P_7 | N31 | | |
| 7 | IO_L51N_7 | P31 | | |
| 7 | IO_L50P_7 | T27 | | |
| 7 | IO_L50N_7 | R28 | | |
| 7 | IO_L49P_7 | M33 | | |
| 7 | IO_L49N_7 | M34 | | |
| 7 | IO_L48P_7 | M31 | | |
| 7 | IO_L48N_7 | M32 | | |
| 7 | IO_L47P_7 | R24 | | |
| 7 | IO_L47N_7 | R25 | | |
| 7 | IO_L46P_7 | M29 | | |
| 7 | IO_L46N_7/VREF_7 | M30 | | |
| 7 | IO_L45P_7 | L33 | | |
| 7 | IO_L45N_7 | L34 | | |
| 7 | IO_L44P_7 | P27 | | |
| 7 | IO_L44N_7 | P28 | | |
| 7 | IO_L43P_7 | L29 | | |
| 7 | IO_L43N_7 | L30 | | |
| 7 | IO_L42P_7 | K33 | | |
| 7 | IO_L42N_7 | K34 | | |
| 7 | IO_L41P_7 | P26 | | |
| 7 | IO_L41N_7 | R26 | | |
| 7 | IO_L40P_7 | K32 | | |
| 7 | IO_L40N_7/VREF_7 | L32 | | |
| 7 | IO_L39P_7 | K29 | | |
| 7 | IO_L39N_7 | K30 | | |
| 7 | IO_L38P_7 | P24 | | |
| 7 | IO_L38N_7 | P25 | | |
| 7 | IO_L37P_7 | J32 | | |
| 7 | IO_L37N_7 | J33 | | |
| 7 | IO_L36P_7 | J31 | | |
| 7 | IO_L36N_7 | K31 | | |
| 7 | IO_L35P_7 | N28 | | |
| 7 | IO_L35N_7 | N29 | | |
| 7 | IO_L34P_7 | H32 | | |
| 7 | IO_L34N_7/VREF_7 | H33 | | |
| 7 | IO_L33P_7 | H29 | | |
| 7 | IO_L33N_7 | H30 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 7 | IO_L32P_7 | N24 | | |
| 7 | IO_L32N_7 | N25 | | |
| 7 | IO_L31P_7 | G33 | | |
| 7 | IO_L31N_7 | G34 | | |
| 7 | IO_L30P_7 | H31 | | |
| 7 | IO_L30N_7 | G32 | | |
| 7 | IO_L29P_7 | N27 | | |
| 7 | IO_L29N_7 | M28 | | |
| 7 | IO_L28P_7 | G28 | | |
| 7 | IO_L28N_7/VREF_7 | G29 | | |
| 7 | IO_L27P_7 | F33 | | |
| 7 | IO_L27N_7 | F34 | | |
| 7 | IO_L26P_7 | M26 | | |
| 7 | IO_L26N_7 | M27 | | |
| 7 | IO_L25P_7 | F31 | | |
| 7 | IO_L25N_7 | F32 | | |
| 7 | IO_L24P_7 | F30 | | |
| 7 | IO_L24N_7 | G30 | | |
| 7 | IO_L23P_7 | L25 | | |
| 7 | IO_L23N_7 | M25 | | |
| 7 | IO_L22P_7 | F27 | | |
| 7 | IO_L22N_7/VREF_7 | F28 | | |
| 7 | IO_L21P_7 | E29 | | |
| 7 | IO_L21N_7 | F29 | | |
| 7 | IO_L20P_7 | L28 | | |
| 7 | IO_L20N_7 | K28 | | |
| 7 | IO_L19P_7 | D33 | | |
| 7 | IO_L19N_7 | D34 | | |
| 7 | IO_L18P_7 | D32 | | |
| 7 | IO_L18N_7 | E32 | | |
| 7 | IO_L17P_7 | K26 | | |
| 7 | IO_L17N_7 | L26 | | |
| 7 | IO_L16P_7 | D31 | | |
| 7 | IO_L16N_7/VREF_7 | E31 | | |
| 7 | IO_L15P_7 | D29 | | |
| 7 | IO_L15N_7 | D30 | | |
| 7 | IO_L14P_7 | J28 | | |
| 7 | IO_L14N_7 | J29 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | M2 | AJ29 | | |
| N/A | TCK | E8 | | |
| N/A | TDI | L30 | | |
| N/A | TDO | L10 | | |
| N/A | TMS | F9 | | |
| N/A | PWRDWN_B | AP9 | | |
| N/A | HSWAP_EN | E32 | | |
| N/A | RSVD | D8 | | |
| N/A | VBATT | L11 | | |
| N/A | DXP | L29 | | |
| N/A | DXN | F31 | | |
| N/A | AVCCAUXTX2 | B35 | | |
| N/A | VTTXPAD2 | B36 | | |
| N/A | TXNPAD2 | A36 | | |
| N/A | TXPPAD2 | A35 | | |
| N/A | GNDA2 | C34 | | |
| N/A | RXPPAD2 | A34 | | |
| N/A | RXNPAD2 | A33 | | |
| N/A | VTRXPAD2 | B34 | | |
| N/A | AVCCAUXRX2 | B33 | | |
| N/A | AVCCAUXTX4 | B31 | | |
| N/A | VTTXPAD4 | B32 | | |
| N/A | TXNPAD4 | A32 | | |
| N/A | TXPPAD4 | A31 | | |
| N/A | GNDA4 | C31 | | |
| N/A | RXPPAD4 | A30 | | |
| N/A | RXNPAD4 | A29 | | |
| N/A | VTRXPAD4 | B30 | | |
| N/A | AVCCAUXRX4 | B29 | | |
| N/A | AVCCAUXTX5 | B27 | | |
| N/A | VTTXPAD5 | B28 | | |
| N/A | TXNPAD5 | A28 | | |
| N/A | TXPPAD5 | A27 | | |
| N/A | GNDA5 | C27 | | |
| N/A | RXPPAD5 | A26 | | |
| N/A | RXNPAD5 | A25 | | |
| N/A | VTRXPAD5 | B26 | | |
| N/A | AVCCAUXRX5 | B25 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | GNDA18 | AU16 | | |
| N/A | TXPPAD18 | AW18 | | |
| N/A | TXNPAD18 | AW19 | | |
| N/A | VTTXPAD18 | AV19 | | |
| N/A | AVCCAUXTX18 | AV18 | | |
| N/A | AVCCAUXRX19 | AV21 | | |
| N/A | VTRXPAD19 | AV22 | | |
| N/A | RXNPAD19 | AW21 | | |
| N/A | RXPPAD19 | AW22 | | |
| N/A | GNDA19 | AU24 | | |
| N/A | TXPPAD19 | AW23 | | |
| N/A | TXNPAD19 | AW24 | | |
| N/A | VTTXPAD19 | AV24 | | |
| N/A | AVCCAUXTX19 | AV23 | | |
| N/A | AVCCAUXRX20 | AV25 | | |
| N/A | VTRXPAD20 | AV26 | | |
| N/A | RXNPAD20 | AW25 | | |
| N/A | RXPPAD20 | AW26 | | |
| N/A | GNDA20 | AU27 | | |
| N/A | TXPPAD20 | AW27 | | |
| N/A | TXNPAD20 | AW28 | | |
| N/A | VTTXPAD20 | AV28 | | |
| N/A | AVCCAUXTX20 | AV27 | | |
| N/A | AVCCAUXRX21 | AV29 | | |
| N/A | VTRXPAD21 | AV30 | | |
| N/A | RXNPAD21 | AW29 | | |
| N/A | RXPPAD21 | AW30 | | |
| N/A | GNDA21 | AU31 | | |
| N/A | TXPPAD21 | AW31 | | |
| N/A | TXNPAD21 | AW32 | | |
| N/A | VTTXPAD21 | AV32 | | |
| N/A | AVCCAUXTX21 | AV31 | | |
| N/A | AVCCAUXRX23 | AV33 | | |
| N/A | VTRXPAD23 | AV34 | | |
| N/A | RXNPAD23 | AW33 | | |
| N/A | RXPPAD23 | AW34 | | |
| N/A | GNDA23 | AU34 | | |
| N/A | TXPPAD23 | AW35 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 0 | IO_L67P_0 | J22 | |
| 0 | IO_L68N_0 | K23 | |
| 0 | IO_L68P_0 | L23 | |
| 0 | IO_L69N_0 | F22 | |
| 0 | IO_L69P_0/VREF_0 | G22 | |
| 0 | IO_L73N_0 | D22 | |
| 0 | IO_L73P_0 | E22 | |
| 0 | IO_L74N_0/GCLK7P | K22 | |
| 0 | IO_L74P_0/GCLK6S | L22 | |
| 0 | IO_L75N_0/GCLK5P | B22 | |
| 0 | IO_L75P_0/GCLK4S | C22 | |
| | | | |
| 1 | IO_L75N_1/GCLK3P | C21 | |
| 1 | IO_L75P_1/GCLK2S | B21 | |
| 1 | IO_L74N_1/GCLK1P | L21 | |
| 1 | IO_L74P_1/GCLK0S | K21 | |
| 1 | IO_L73N_1 | E21 | |
| 1 | IO_L73P_1 | D21 | |
| 1 | IO_L69N_1/VREF_1 | G21 | |
| 1 | IO_L69P_1 | F21 | |
| 1 | IO_L68N_1 | L20 | |
| 1 | IO_L68P_1 | K20 | |
| 1 | IO_L67N_1 | J21 | |
| 1 | IO_L67P_1 | H21 | |
| 1 | IO_L66N_1/VREF_1 | C20 | |
| 1 | IO_L66P_1 | B20 | |
| 1 | IO_L65N_1 | M20 | |
| 1 | IO_L65P_1 | M21 | |
| 1 | IO_L64N_1 | G20 | |
| 1 | IO_L64P_1 | F20 | |
| 1 | IO_L60N_1 | B19 | |
| 1 | IO_L60P_1 | A19 | |
| 1 | IO_L59N_1 | K19 | |
| 1 | IO_L59P_1 | J19 | |
| 1 | IO_L58N_1 | D19 | |
| 1 | IO_L58P_1 | D20 | |
| 1 | IO_L57N_1/VREF_1 | F19 | |