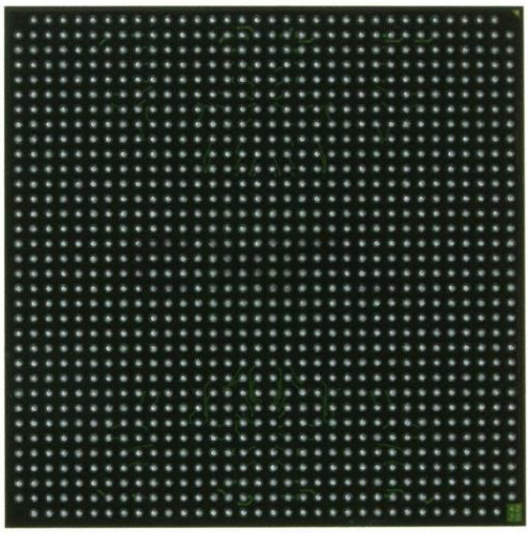

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-7ffg1152c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

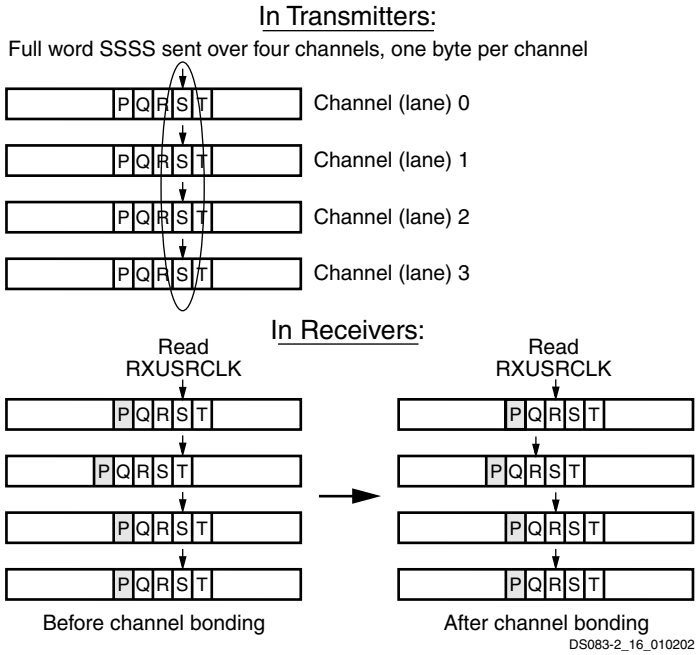

Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

Table 5: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2
1-byte	1:2 (1)
2-byte	1:1
4-byte	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, or 4) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

The Trace port provides instruction execution trace information to an external trace tool. The PPC405 core is capable of back trace and forward trace. Back trace is the tracing of instructions prior to a debug event while forward trace is the tracing of instructions after a debug event.

The processor JTAG port and the FPGA JTAG port can be accessed independently, or the two can be programmatically linked together and accessed via the dedicated FPGA JTAG pins.

For detailed information on the PPC405 JTAG interface, please refer to the "JTAG Interface" section of the **PowerPC 405 Processor Block Reference Guide**

CoreConnect™ Bus Architecture

The Processor Block is compatible with the CoreConnect™ bus architecture. Any CoreConnect compliant cores including Xilinx soft IP can integrate with the Processor Block through this high-performance bus architecture implemented on FPGA fabric.

The CoreConnect architecture provides three buses for interconnecting Processor Blocks, Xilinx soft IP, third party IP, and custom logic, as shown in Figure 15:

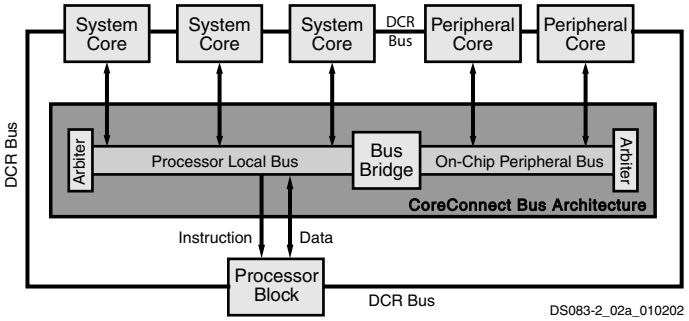

Figure 15: **CoreConnect Block Diagram**

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) bus

High-performance peripherals connect to the high-bandwidth, low-latency PLB. Slower peripheral cores connect to the OPB, which reduces traffic on the PLB, resulting in greater overall system performance.

For more information, refer to:
http://www-3.ibm.com/chips/techlib/techlib.nfs/productfamilies/CoreConnect_Bus_Architecture/

Functional Description: Embedded PowerPC 405 Core

This section offers a brief overview of the various functional blocks shown in Figure 16.

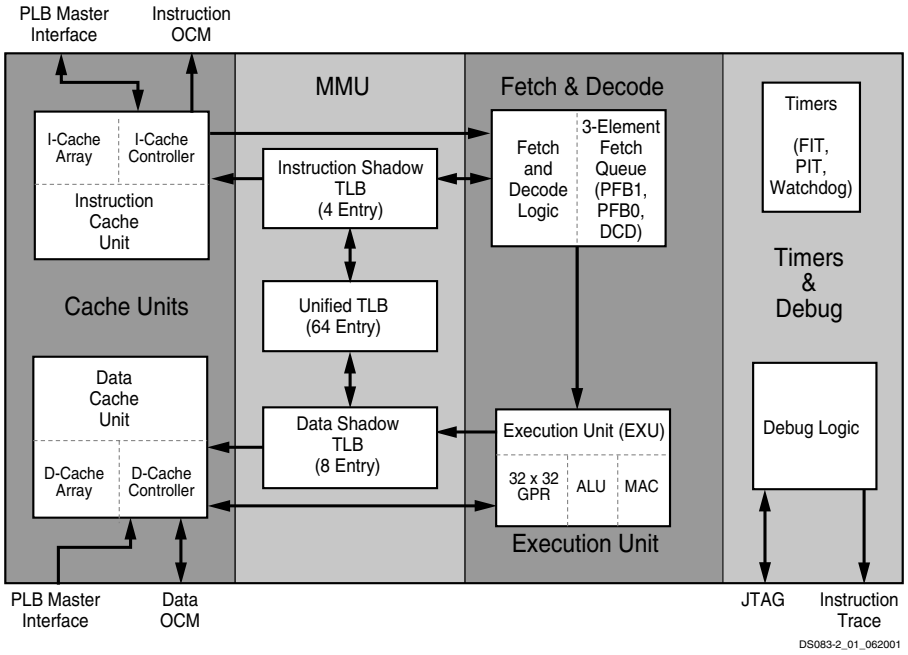

Figure 16: **Embedded PPC405 Core Block Diagram**

Embedded PPC405 Core

The embedded PPC405 core is a 32-bit Harvard architecture processor. Figure 16 illustrates its functional blocks:

- Cache units
- Memory Management unit
- Fetch Decode unit

memory protection. Working with appropriate system-level software, the MMU provides the following functions:

- Translation of the 4 GB effective address space into physical addresses
- Independent enabling of instruction and data translation/protection
- Page-level access control using the translation mechanism
- Software control of page replacement strategy
- Additional control over protection using zones
- Storage attributes for cache policy and speculative memory access control

The MMU can be disabled under software control. If the MMU is not used, the PPC405 core provides other storage control mechanisms.

Translation Look-Aside Buffer (TLB)

The Translation Look-Aside Buffer (TLB) is the hardware resource that controls translation and protection. It consists of 64 entries, each specifying a page to be translated. The TLB is fully associative; a given page entry can be placed anywhere in the TLB. The translation function of the MMU occurs pre-cache. Cache tags and indexing use physical addresses.

Software manages the establishment and replacement of TLB entries. This gives system software significant flexibility in implementing a custom page replacement strategy. For example, to reduce TLB thrashing or translation delays, software can reserve several TLB entries in the TLB for globally accessible static mappings. The instruction set provides several instructions used to manage TLB entries. These instructions are privileged and require the software to be executing in supervisor state. Additional TLB instructions are provided to move TLB entry fields to and from GPRs.

The MMU divides logical storage into pages. Eight page sizes (1 KB, 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB) are simultaneously supported, such that, at any given time, the TLB can contain entries for any combination of page sizes. In order for a logical to physical translation to exist, a valid entry for the page containing the logical address must be in the TLB. Addresses for which no TLB entry exists cause TLB-Miss exceptions.

To improve performance, four instruction-side and eight data-side TLB entries are kept in shadow arrays. The shadow arrays allow single-cycle address translation and also help to avoid TLB contention between load/store and instruction fetch operations. Hardware manages the replacement and invalidation of shadow-TLB entries; no system software action is required.

Memory Protection

When address translation is enabled, the translation mechanism provides a basic level of protection.

The Zone Protection Register (ZPR) enables the system software to override the TLB access controls. For example, the ZPR provides a way to deny read access to application programs. The ZPR can be used to classify storage by type; access by type can be changed without manipulating individual TLB entries.

The PowerPC Architecture provides WIU0GE (write-back / write-through, cacheability, user-defined 0, guarded, endian) storage attributes that control memory accesses, using bits in the TLB or, when address translation is disabled, storage attribute control registers.

When address translation is enabled, storage attribute control bits in the TLB control the storage attributes associated with the current page. When address translation is disabled, bits in each storage attribute control register control the storage attributes associated with storage regions. Each storage attribute control register contains 32 fields. Each field sets the associated storage attribute for a 128 MB memory region.

Timers

The embedded PPC405 core contains a 64-bit time base and three timers, as shown in Figure 17:

- Programmable Interval Timer (PIT)
- Fixed Interval Timer (FIT)
- Watchdog Timer (WDT)

The time base counter increments either by an internal signal equal to the CPU clock rate or by a separate external timer clock signal. No interrupts are generated when the time base rolls over. The three timers are synchronous with the time base.

The PIT is a 32-bit register that decrements at the same rate as the time base is incremented. The user loads the PIT register with a value to create the desired delay. When the register reaches zero, the timer stops decrementing and generates a PIT interrupt. Optionally, the PIT can be programmed to auto-reload the last value written to the PIT register, after which the PIT continues to decrement.

The FIT generates periodic interrupts based on one of four selectable bits in the time base. When the selected bit changes from 0 to 1, the PPC405 core generates a FIT interrupt.

The WDT provides a periodic critical-class interrupt based on a selected bit in the time base. This interrupt can be used for system error recovery in the event of software or system lockups. Users may select one of four time periods for the interval and the type of reset generated if the WDT expires twice without an intervening clear from software. If enabled, the watchdog timer generates a reset unless an exception handler updates the WDT status bit before the timer has completed two of the selected timer intervals.

Figure 30 provides examples illustrating the use of the LVDS_25_DCI and LVDSEXT_25_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

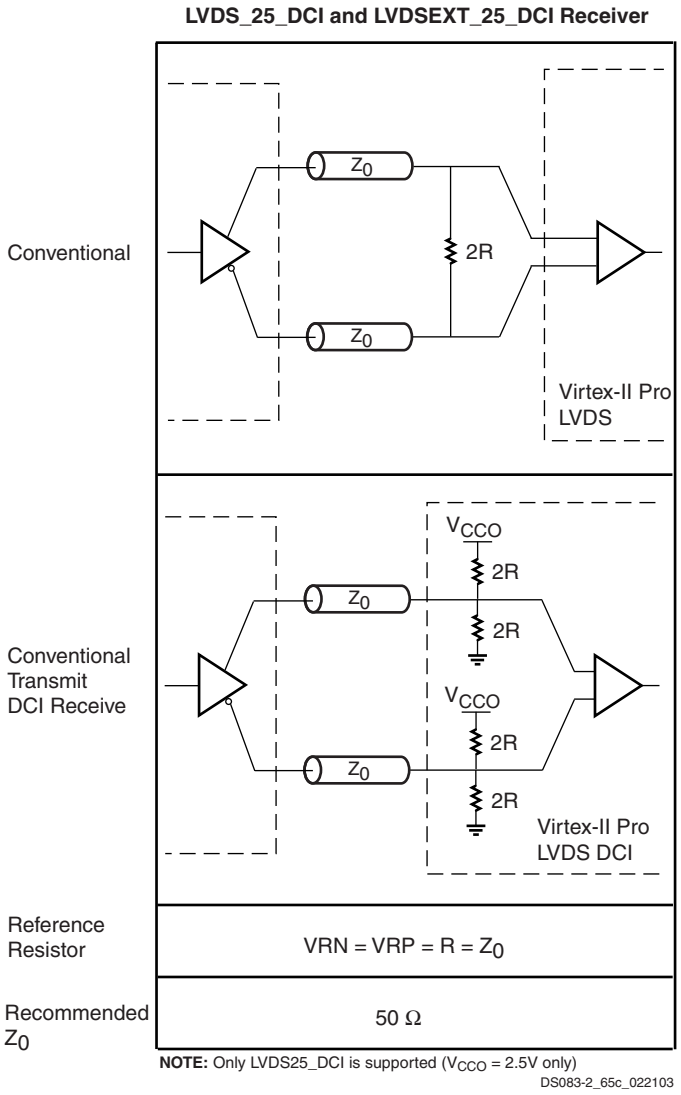

Figure 30: **LVDS DCI Usage Examples**

On-Chip Differential Termination

Virtex-II Pro provides a true 100Ω differential termination (DT) across the input differential receiver terminals. The LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT I/O standards. For further details, refer to **Solution Record 17244**. Also see the ***Virtex-II Pro Platform FPGA User Guide*** for more design information.

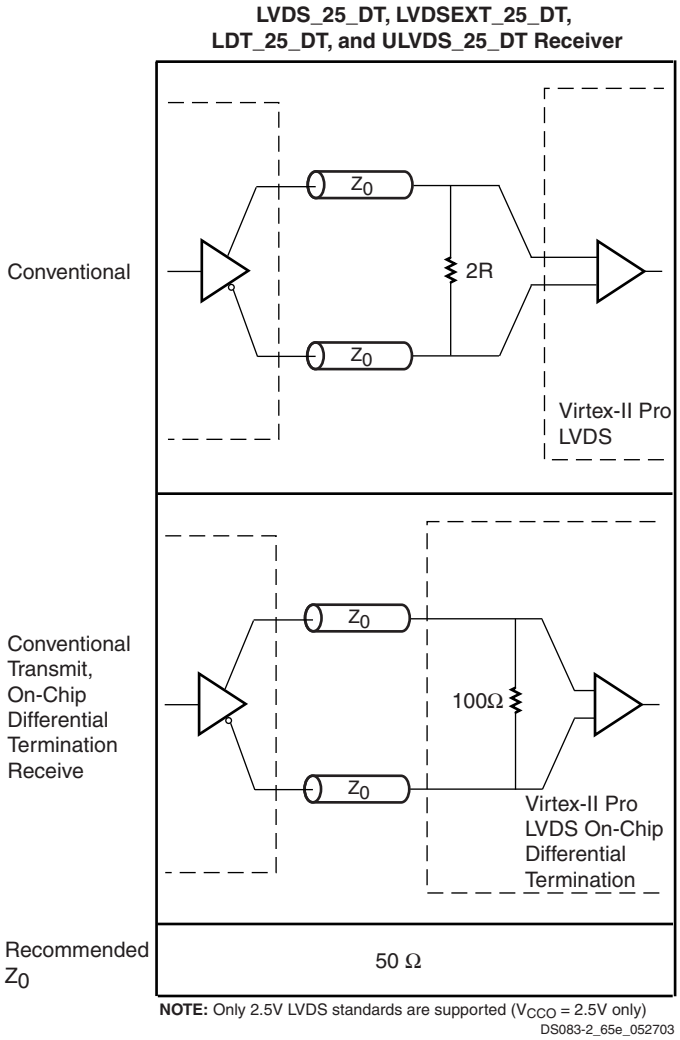

Figure 31: **LVDS Differential Termination Usage Examples**

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination *(Continued)***

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP70	Available User I/Os	-	-		-	-	-	-	964	996	-
	RocketIO MGT Pins	-	-		-	-	-	-	144	180	-
	Differential I/O Pairs	-	-		-	-	-	-	476	492	-
XC2VPX70	**Available User I/Os**	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**992**	**-**
	RocketIO X MGT Pins	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**180**	**-**
	Differential I/O Pairs	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**490**	**-**
XC2VP100	Available User I/Os	-	-		-	-	-	-	-	1040	1164
	RocketIO MGT Pins	-	-		-	-	-	-	-	180	0
	Differential I/O Pairs	-	-		-	-	-	-	-	512	572

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1)

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
1	IO_L45N_1/VREF_1	C18			
1	IO_L45P_1	D18			
1	IO_L43N_1	E18			
1	IO_L43P_1	F18			
1	IO_L39N_1	G18			
1	IO_L39P_1	H18			
1	IO_L37N_1	A19			
1	IO_L37P_1	B19			
1	IO_L09N_1/VREF_1	E19			
1	IO_L09P_1	F19			
1	IO_L07N_1	G19			
1	IO_L07P_1	H19			
1	IO_L06N_1	C20			
1	IO_L06P_1	D20			
1	IO_L05_1/No_Pair	E20			
1	IO_L03N_1/VREF_1	F20			
1	IO_L03P_1	G20			
1	IO_L02N_1	D21			
1	IO_L02P_1	E21			
1	IO_L01N_1/VRP_1	D22			
1	IO_L01P_1/VRN_1	E22			
2	IO_L01N_2/VRP_2	C25			
2	IO_L01P_2/VRN_2	C26			
2	IO_L02N_2	D25			
2	IO_L02P_2	D26			
2	IO_L03N_2	E23			
2	IO_L03P_2	F22			
2	IO_L04N_2/VREF_2	E25			
2	IO_L04P_2	E26			
2	IO_L06N_2	F21			
2	IO_L06P_2	G21			
2	IO_L24N_2	F23	NC		
2	IO_L24P_2	F24	NC		
2	IO_L31N_2	F25			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L52P_7	M7			
7	IO_L52N_7/VREF_7	L7			
7	IO_L50P_7	K1			
7	IO_L50N_7	K2			
7	IO_L49P_7	L3			
7	IO_L49N_7	K3			
7	IO_L48P_7	K4			
7	IO_L48N_7	K5			
7	IO_L46P_7	L8			
7	IO_L46N_7/VREF_7	K8			
7	IO_L44P_7	J1			
7	IO_L44N_7	J2			
7	IO_L43P_7	J3			
7	IO_L43N_7	J4			
7	IO_L42P_7	J5			
7	IO_L42N_7	J6			
7	IO_L40P_7	J7			
7	IO_L40N_7/VREF_7	J8			
7	IO_L38P_7	H1			
7	IO_L38N_7	H2			
7	IO_L37P_7	H6			
7	IO_L37N_7	H7			
7	IO_L36P_7	G1			
7	IO_L36N_7	G2			
7	IO_L34P_7	G3			
7	IO_L34N_7/VREF_7	G4			
7	IO_L32P_7	H5			
7	IO_L32N_7	G5			
7	IO_L31P_7	F1			
7	IO_L31N_7	F2			
7	IO_L24P_7	F3	NC		
7	IO_L24N_7	F4	NC		
7	IO_L06P_7	G6			
7	IO_L06N_7	F6			
7	IO_L04P_7	E1			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L34P_6	AE30				
6	IO_L34N_6	AE31				
6	IO_L35P_6	AD27				
6	IO_L35N_6	AD28				
6	IO_L36P_6	AF33				
6	IO_L36N_6	AE33				
6	IO_L37P_6	AD29				
6	IO_L37N_6	AD30				
6	IO_L38P_6	AB25				
6	IO_L38N_6	AB26				
6	IO_L39P_6	AD31				
6	IO_L39N_6/VREF_6	AD32				
6	IO_L40P_6	AC28				
6	IO_L40N_6	AC29				
6	IO_L41P_6	AB27				
6	IO_L41N_6	AB28				
6	IO_L42P_6	AE34				
6	IO_L42N_6	AD34				
6	IO_L43P_6	AC31				
6	IO_L43N_6	AC32				
6	IO_L44P_6	AA25				
6	IO_L44N_6	AA26				
6	IO_L45P_6	AD33				
6	IO_L45N_6/VREF_6	AC33				
6	IO_L46P_6	AB29				
6	IO_L46N_6	AB30				
6	IO_L47P_6	AA27				
6	IO_L47N_6	AA28				
6	IO_L48P_6	AB31				
6	IO_L48N_6	AB32				
6	IO_L49P_6	AA29				
6	IO_L49N_6	AA30				
6	IO_L50P_6	Y25				
6	IO_L50N_6	Y26				
6	IO_L51P_6	AC34				
6	IO_L51N_6/VREF_6	AB34				
6	IO_L52P_6	AA31				
6	IO_L52N_6	AA32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	VCCO_7	T23				
7	VCCO_7	U23				
N/A	CCLK	AE9				
N/A	PROG_B	J26				
N/A	DONE	AE10				
N/A	M0	AF26				
N/A	M1	AE26				
N/A	M2	AE25				
N/A	TCK	J9				
N/A	TDI	H28				
N/A	TDO	H7				
N/A	TMS	K10				
N/A	PWRDWN_B	AF9				
N/A	HSWAP_EN	K25				
N/A	RSVD	G8				
N/A	VBATT	K9				
N/A	DXP	K26				
N/A	DXN	G27				
N/A	AVCCAUXTX2	B32	NC	NC		
N/A	VTTXPAD2	B33	NC	NC		
N/A	TXNPAD2	A33	NC	NC		
N/A	TXPPAD2	A32	NC	NC		
N/A	GNDA2	C30	NC	NC		
N/A	RXPPAD2	A31	NC	NC		
N/A	RXNPAD2	A30	NC	NC		
N/A	VTRXPAD2	B31	NC	NC		
N/A	AVCCAUXRX2	B30	NC	NC		
N/A	AVCCAUXTX4	B28				
N/A	VTTXPAD4	B29				
N/A	TXNPAD4	A29				
N/A	TXPPAD4	A28				
N/A	GNDA4	C27				
N/A	RXPPAD4	A27				
N/A	RXNPAD4	A26				
N/A	VTRXPAD4	B27				
N/A	AVCCAUXRX4	B26				
N/A	AVCCAUXTX5	B24	NC	NC	NC	

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L59P_2	U11		
2	IO_L60N_2	R1		
2	IO_L60P_2	R2		
2	IO_L85N_2	T3		
2	IO_L85P_2	T4		
2	IO_L86N_2	U8		
2	IO_L86P_2	U9		
2	IO_L87N_2	U2		
2	IO_L87P_2	T2		
2	IO_L88N_2/VREF_2	U4		
2	IO_L88P_2	U5		
2	IO_L89N_2	U6		
2	IO_L89P_2	U7		
2	IO_L90N_2	V3		
2	IO_L90P_2	U3		
3	IO_L90N_3	V6		
3	IO_L90P_3	V7		
3	IO_L89N_3	V10		
3	IO_L89P_3	V11		
3	IO_L88N_3	V4		
3	IO_L88P_3	V5		
3	IO_L87N_3/VREF_3	V2		
3	IO_L87P_3	W2		
3	IO_L86N_3	V8		
3	IO_L86P_3	V9		
3	IO_L85N_3	W6		
3	IO_L85P_3	W7		
3	IO_L60N_3	W3		
3	IO_L60P_3	W4		
3	IO_L59N_3	W10		
3	IO_L59P_3	W11		
3	IO_L58N_3	Y5		
3	IO_L58P_3	Y6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	AA3		
3	IO_L56N_3	W8		
3	IO_L56P_3	Y7		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M23		
N/A	VCCINT	AB22		
N/A	VCCINT	AA22		
N/A	VCCINT	Y22		
N/A	VCCINT	W22		
N/A	VCCINT	V22		
N/A	VCCINT	U22		
N/A	VCCINT	T22		
N/A	VCCINT	R22		
N/A	VCCINT	P22		
N/A	VCCINT	N22		
N/A	VCCINT	AB21		
N/A	VCCINT	N21		
N/A	VCCINT	AB20		
N/A	VCCINT	N20		
N/A	VCCINT	AB19		
N/A	VCCINT	N19		
N/A	VCCINT	AB18		
N/A	VCCINT	N18		
N/A	VCCINT	AB17		
N/A	VCCINT	N17		
N/A	VCCINT	AB16		
N/A	VCCINT	N16		
N/A	VCCINT	AB15		
N/A	VCCINT	N15		
N/A	VCCINT	AB14		
N/A	VCCINT	N14		
N/A	VCCINT	AB13		
N/A	VCCINT	AA13		
N/A	VCCINT	Y13		
N/A	VCCINT	W13		
N/A	VCCINT	V13		
N/A	VCCINT	U13		
N/A	VCCINT	T13		
N/A	VCCINT	R13		
N/A	VCCINT	P13		
N/A	VCCINT	N13		
N/A	VCCINT	AC12		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L09N_4		AR11		
4	IO_L09P_4/VREF_4		AP11		
4	IO_L19N_4		AV11		
4	IO_L19P_4		AU11		
4	IO_L20N_4		AY10		
4	IO_L20P_4		AY11		
4	IO_L21N_4		AN12		
4	IO_L21P_4		AM12		
4	IO_L25N_4		AR12		
4	IO_L25P_4		AP12		
4	IO_L26N_4		AT12		
4	IO_L26P_4		AU12		
4	IO_L27N_4		AW12		
4	IO_L27P_4/VREF_4		AV12		
4	IO_L28N_4		AM13		
4	IO_L28P_4		AL13		
4	IO_L29N_4		AP13		
4	IO_L29P_4		AN13		
4	IO_L30N_4		AT13		
4	IO_L30P_4		AR13		
4	IO_L34N_4		AV13		
4	IO_L34P_4		AU13		
4	IO_L35N_4		AW13		
4	IO_L35P_4		AY13		
4	IO_L36N_4		AL15		
4	IO_L36P_4/VREF_4		AL14		
4	IO_L78N_4		AN14	NC	
4	IO_L78P_4		AM14	NC	
4	IO_L83_4/No_Pair		AR14	NC	
4	IO_L84N_4		AU14	NC	
4	IO_L84P_4		AT14	NC	
4	IO_L85N_4		AW14	NC	
4	IO_L85P_4		AV14	NC	
4	IO_L86N_4		AM15	NC	
4	IO_L86P_4		AN15	NC	
4	IO_L87N_4		AR15	NC	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L34P_0	C30	
0	IO_L35N_0	L29	
0	IO_L35P_0	M29	
0	IO_L36N_0	H28	
0	IO_L36P_0/VREF_0	G29	
0	IO_L76N_0	E29	
0	IO_L76P_0	F29	
0	IO_L77N_0	J29	
0	IO_L77P_0	K29	
0	IO_L78N_0	D28	
0	IO_L78P_0	C29	
0	IO_L79N_0	A29	
0	IO_L79P_0	B29	
0	IO_L80_0/No_Pair	L28	
0	IO_L83_0/No_Pair	M28	
0	IO_L84N_0	G27	
0	IO_L84P_0	G28	
0	IO_L85N_0	E28	
0	IO_L85P_0	F28	
0	IO_L86N_0	J28	
0	IO_L86P_0	K28	
0	IO_L87N_0	C27	
0	IO_L87P_0/VREF_0	C28	
0	IO_L37N_0	A28	
0	IO_L37P_0	B28	
0	IO_L38N_0	L27	
0	IO_L38P_0	M27	
0	IO_L39N_0	H26	
0	IO_L39P_0	H27	
0	IO_L43N_0	E27	
0	IO_L43P_0	F27	
0	IO_L44N_0	J27	
0	IO_L44P_0	K27	
0	IO_L45N_0	D26	
0	IO_L45P_0/VREF_0	D27	
0	IO_L10N_0	A27	NC
0	IO_L10P_0	B27	NC

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	VCCO_3	AF14	
3	VCCO_3	AE14	
3	VCCO_3	AD14	
3	VCCO_3	AC14	
3	VCCO_3	AB14	
3	VCCO_3	AR10	
3	VCCO_3	AL10	
3	VCCO_3	AN8	
3	VCCO_3	AJ8	
3	VCCO_3	AD8	
3	VCCO_3	AW6	
3	VCCO_3	AU4	
3	VCCO_3	AN4	
3	VCCO_3	AJ4	
3	VCCO_3	AD4	
2	VCCO_2	AA15	
2	VCCO_2	Y15	
2	VCCO_2	W15	
2	VCCO_2	V15	
2	VCCO_2	U15	
2	VCCO_2	T15	
2	VCCO_2	AA14	
2	VCCO_2	Y14	
2	VCCO_2	W14	
2	VCCO_2	V14	
2	VCCO_2	U14	
2	VCCO_2	T14	
2	VCCO_2	R14	
2	VCCO_2	M10	
2	VCCO_2	H10	
2	VCCO_2	W8	
2	VCCO_2	P8	
2	VCCO_2	K8	
2	VCCO_2	D6	
2	VCCO_2	W4	
2	VCCO_2	P4	
2	VCCO_2	K4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	M2	AM33	
N/A	TCK	K10	
N/A	TDI	M32	
N/A	TDO	M11	
N/A	TMS	L10	
N/A	PWRDWN_B	AP10	
N/A	HSWAP_EN	K33	
N/A	RSVD	J10	
N/A	VBATT	M12	
N/A	DXP	M31	
N/A	DXN	L33	
N/A	VCCINT	AK30	
N/A	VCCINT	N30	
N/A	VCCINT	AJ29	
N/A	VCCINT	P29	
N/A	VCCINT	AJ28	
N/A	VCCINT	AH28	
N/A	VCCINT	R28	
N/A	VCCINT	P28	
N/A	VCCINT	AJ27	
N/A	VCCINT	AH27	
N/A	VCCINT	AG27	
N/A	VCCINT	AF27	
N/A	VCCINT	AE27	
N/A	VCCINT	AD27	
N/A	VCCINT	AC27	
N/A	VCCINT	AB27	
N/A	VCCINT	AA27	
N/A	VCCINT	Y27	
N/A	VCCINT	W27	
N/A	VCCINT	V27	
N/A	VCCINT	U27	
N/A	VCCINT	T27	
N/A	VCCINT	R27	
N/A	VCCINT	P27	
N/A	VCCINT	AH26	