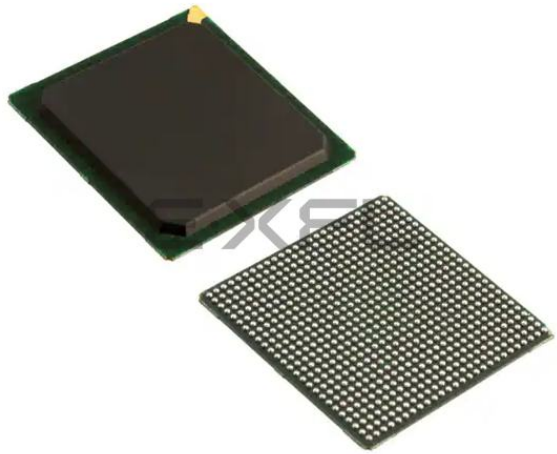

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4848
Number of Logic Elements/Cells	43632
Total RAM Bits	3538944
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp40-7fgg676c

RocketIO and RocketIO X Feature Comparison

Table 7 summarizes the major differences between the RocketIO and RocketIO X MGTs. The ***RocketIO X Transceiver User Guide*** has more details, including a design migration guide in the Appendix.

Table 7: **RocketIO PMA versus RocketIO X PMA**

	RocketIO X Transceiver	RocketIO Transceiver
PCS Features:		
FPGA interface	1, 2, 4, and 8 byte width	1, 2, and 4 byte width
Coding support	8B/10B and 64B/66B bypassable	8B/10B bypassable
Gearbox/scrambler support	Yes	N/A
CRC Support	No	Yes
Half rate	No	Yes
PMA Features:		
Baud rate	2.488 Gb/s - 6.25 Gb/s(2)	622 Mb/s - 3.125 Gb/s
Reference clock frequency tolerance	350 PPM	100 PPM
Reference clock multiplier	x16, x20, x32, x40	x20
Max run length	75	75
Receive equalization	Built-in analog linear, programmable	None
Output swing (differential p-p)	200 mV to 1600 mV, programmable	800 mV to 1600 mV, programmable
Pre-emphasis	0% to 500%, programmable	4 selectable levels from 10% to 33%
Slew rate control	2 selectable levels	None
Termination	On-chip internal, 50Ω	On-chip internal, 50Ω/75Ω selectable
AC coupling capacitor	On-chip internal. Can be AC- or DC-coupled externally	None
Transmit supply voltage (AVCCAUXTX)	2.5V	2.5V
Receive supply voltage (AVCCAUXRX)	1.5V, 1.8V(1)	2.5V
PMA configuration support	Direct, dynamic, and partial configuration	Partial configuration
Others:		
JTAG support	Input only	None
Process technology	0.13 µm	0.25 µm
Available packages	Flip-chip only	Flip-chip and wire-bond

Notes:
1. AVCCAUXRX for RocketIO X MGT is 1.5V (nominal) for 8B/10B-encoded data. For all other encoding protocols, AVCCAUXRX is 1.8V (nominal).
2. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.

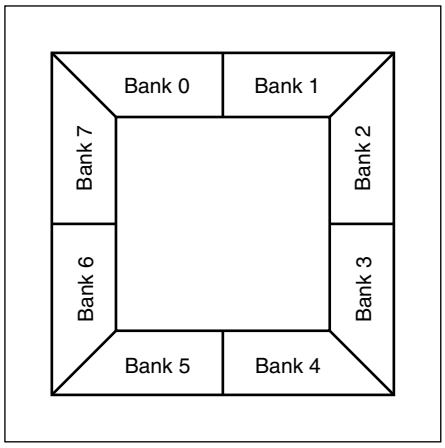


Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

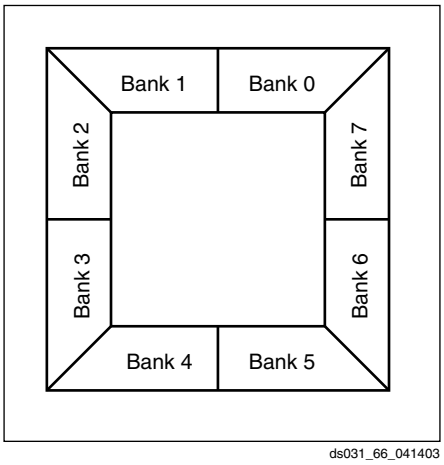


Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

Configuration

Virtex-II Pro devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1, and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. (The TDO pin is open-drain and does not have an internal pull-up resistor.) Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 2.5V is used for these pins. All configuration pins are LVCMOS25 12mA. See Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

A "persist" option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II Pro supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

Refer to Table 32, page 57.

A detailed description of configuration modes is provided in the *Virtex-II Pro Platform FPGA User Guide.*

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying [111] to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II Pro FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II Pro FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II Pro FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Table 14 shows internal (register-to-register) performance. Values are reported in MHz.

Table 14: **Register-to-Register Performance**

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions:			
16-bit Address Decoder	XC2VP20FF1152-6	547	MHz
32-bit Address Decoder	XC2VP20FF1152-6	392	MHz
64-bit Address Decoder	XC2VP20FF1152-6	310	MHz
4:1 MUX	XC2VP20FF1152-6	710	MHz
8:1 MUX	XC2VP20FF1152-6	609	MHz
16:1 MUX	XC2VP20FF1152-6	472	MHz
32:1 MUX	XC2VP20FF1152-6	400	MHz
Register to LUT to Register	XC2VP20FF1152-6	1046	MHz
8-bit Adder	XC2VP20FF1152-6	337	MHz
16-bit Adder	XC2VP20FF1152-6	334	MHz
32-bit Adder	XC2VP20FF1152-6	252	MHz
64-bit Adder	XC2VP20FF1152-6	202	MHz
128-bit Adder	XC2VP20FF1152-6	131	MHz
24-bit Counter	XC2VP20FF1152-6	309	MHz
64-bit Counter	XC2VP20FF1152-6	207	MHz
64-bit Accumulator	XC2VP20FF1152-6	150	MHz
Multiplier 18x18 (with Block RAM inputs)	XC2VP20FF1152-6	135	MHz
Multiplier 18x18 (with Register inputs)	XC2VP20FF1152-6	147	MHz
Memory:			
Block RAM			
Single-Port 4096 x 4 bits	XC2VP20FF1152-6	355	MHz
Distributed RAM			
Single-Port 16 x 8-bit	XC2VP20FF1152-6	555	MHz
Single-Port 32 x 8-bit	XC2VP20FF1152-6	557	MHz
Single-Port 64 x 8-bit	XC2VP20FF1152-6	408	MHz
Single-Port 128 x 8-bit	XC2VP20FF1152-6	336	MHz
Dual-Port 16 x 8-bit	XC2VP20FF1152-6	549	MHz
Dual-Port 32 x 8-bit	XC2VP20FF1152-6	460	MHz
Dual-Port 64 x 8-bit	XC2VP20FF1152-6	407	MHz

Block SelectRAM+ Switching Characteristics

Table 47: **Block SelectRAM+ Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	1.41	1.50	1.68	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.27/ 0.22	0.31/ 0.25	0.35/ 0.28	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.20/ 0.22	0.23/ 0.25	0.26/ 0.28	ns, min
EN input	T_{BECK}/T_{BCKE}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.33/ 0.00	0.35/ 0.00	0.39/ 0.00	ns, min
Clock CLK					
CLKA to CLKB setup time for different ports	T_{BCCS}	1.0	1.0	1.0	ns, min
Minimum Pulse Width, High	T_{BPWH}	1.17	1.30	1.50	ns, min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.30	1.50	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 48: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.88	1.01	1.12	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.48	0.55	0.61	ns, max
TRI input to valid data on OUT output	T_{ON}	0.48	0.55	0.61	ns, max

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 6, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FG456/FGG456 fine-pitch BGA package. The pins in these devices are same, except for the differences shown in the "No Connects" column. Following this table are the FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	D5			
0	IO_L01P_0/VRN_0	D6			
0	IO_L02N_0	E6			
0	IO_L02P_0	E7			
0	IO_L03N_0	D7			
0	IO_L03P_0/VREF_0	C7			
0	IO_L05_0/No_Pair	E8			
0	IO_L06N_0	D8			
0	IO_L06P_0	C8			
0	IO_L07N_0	F9			
0	IO_L07P_0	E9			
0	IO_L09N_0	D9			
0	IO_L09P_0/VREF_0	D10			
0	IO_L67N_0	F10			
0	IO_L67P_0	E10			
0	IO_L69N_0	C10			
0	IO_L69P_0/VREF_0	B11			
0	IO_L74N_0/GCLK7P	F11			
0	IO_L74P_0/GCLK6S	E11			
0	IO_L75N_0/GCLK5P	D11			
0	IO_L75P_0/GCLK4S	C11			
1	IO_L75N_1/GCLK3P	C12			
1	IO_L75P_1/GCLK2S	D12			
1	IO_L74N_1/GCLK1P	E12			
1	IO_L74P_1/GCLK0S	F12			
1	IO_L69N_1/VREF_1	B12			
1	IO_L69P_1	C13			
1	IO_L67N_1	E13			
1	IO_L67P_1	F13			
1	IO_L09N_1/VREF_1	D13			
1	IO_L09P_1	D14			
1	IO_L07N_1	E14			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L03P_3	AC25			
3	IO_L02N_3	AC24			
3	IO_L02P_3	AD25			
3	IO_L01N_3/VRP_3	AD26			
3	IO_L01P_3/VRN_3	AE26			
4	IO_L01N_4/BUSY/DOUT(1)	AB22			
4	IO_L01P_4/INIT_B	AC22			
4	IO_L02N_4/D0/DIN(1)	AB21			
4	IO_L02P_4/D1	AC21			
4	IO_L03N_4/D2	Y20			
4	IO_L03P_4/D3	AA20			
4	IO_L05_4/No_Pair	AB20			
4	IO_L06N_4/VRP_4	AC20			
4	IO_L06P_4/VRN_4	AD20			
4	IO_L07N_4	W19			
4	IO_L07P_4/VREF_4	Y19			
4	IO_L09N_4	AA19			
4	IO_L09P_4/VREF_4	AB19			
4	IO_L37N_4	AE19			
4	IO_L37P_4	AF19			
4	IO_L39N_4	W18			
4	IO_L39P_4	Y18			
4	IO_L43N_4	AA18			
4	IO_L43P_4	AB18			
4	IO_L45N_4	AC18			
4	IO_L45P_4/VREF_4	AD18			
4	IO_L46N_4	W17			
4	IO_L46P_4	W16			
4	IO_L48N_4	AB17			
4	IO_L48P_4	AB16			
4	IO_L49N_4	AC17			
4	IO_L49P_4	AD17			
4	IO_L50_4/No_Pair	Y16			
4	IO_L53_4/No_Pair	AA16			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	R15			
N/A	GND	R16			
N/A	GND	R24			
N/A	GND	T11			
N/A	GND	T12			
N/A	GND	T13			
N/A	GND	T14			
N/A	GND	T15			
N/A	GND	T16			
N/A	GND	U6			
N/A	GND	U21			
N/A	GND	W4			
N/A	GND	W23			
N/A	GND	AA10			
N/A	GND	AA17			
N/A	GND	AC4			
N/A	GND	AC8			
N/A	GND	AC19			
N/A	GND	AC23			
N/A	GND	AD3			
N/A	GND	AD24			
N/A	GND	AE2			
N/A	GND	AE25			
N/A	GND	AF1			
N/A	GND	AF26			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in Table 8, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L48N_3	W1	NC		
3	IO_L48P_3	W2	NC		
3	IO_L47N_3	W3	NC		
3	IO_L47P_3	W4	NC		
3	IO_L46N_3	W5	NC		
3	IO_L46P_3	W6	NC		
3	IO_L45N_3/VREF_3	Y1	NC		
3	IO_L45P_3	AA1	NC		
3	IO_L44N_3	Y3	NC		
3	IO_L44P_3	Y4	NC		
3	IO_L43N_3	Y5	NC		
3	IO_L43P_3	Y6	NC		
3	IO_L42N_3	AA2	NC	NC	NC
3	IO_L42P_3	AA3	NC	NC	NC
3	IO_L41N_3	AA4	NC	NC	NC
3	IO_L41P_3	AA5	NC	NC	NC
3	IO_L39N_3/VREF_3	AB1	NC	NC	NC
3	IO_L39P_3	AB2	NC	NC	NC
3	IO_L06N_3	AB3			
3	IO_L06P_3	AB4			
3	IO_L05N_3	AC1			
3	IO_L05P_3	AC2			
3	IO_L04N_3	AD1			
3	IO_L04P_3	AD2			
3	IO_L03N_3/VREF_3	AE1			
3	IO_L03P_3	AF2			
3	IO_L02N_3	AC3			
3	IO_L02P_3	AD4			
3	IO_L01N_3/VRP_3	AE3			
3	IO_L01P_3/VRN_3	AF3			
4	IO_L01N_4/BUSY/DOUT(1)	AC6			
4	IO_L01P_4/INIT_B	AD6			
4	IO_L02N_4/D0/DIN(1)	AB7			
4	IO_L02P_4/D1	AC7			
4	IO_L03N_4/D2	AA7			
4	IO_L03P_4/D3	AA8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	P17				
N/A	GND	P18				
N/A	GND	P19				
N/A	GND	P20				
N/A	GND	P21				
N/A	GND	R8				
N/A	GND	R14				
N/A	GND	R15				
N/A	GND	R16				
N/A	GND	R17				
N/A	GND	R18				
N/A	GND	R19				
N/A	GND	R20				
N/A	GND	R21				
N/A	GND	R27				
N/A	GND	T1				
N/A	GND	T14				
N/A	GND	T15				
N/A	GND	T16				
N/A	GND	T17				
N/A	GND	T18				
N/A	GND	T19				
N/A	GND	T20				
N/A	GND	T21				
N/A	GND	T34				
N/A	GND	U14				
N/A	GND	U15				
N/A	GND	U16				
N/A	GND	U17				
N/A	GND	U18				
N/A	GND	U19				
N/A	GND	U20				
N/A	GND	U21				
N/A	GND	V14				
N/A	GND	V15				
N/A	GND	V16				
N/A	GND	V17				
N/A	GND	V18				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L44N_6	AA28		
6	IO_L45P_6	AC31		
6	IO_L45N_6/VREF_6	AC32		
6	IO_L46P_6	AC29		
6	IO_L46N_6	AC30		
6	IO_L47P_6	AA24		
6	IO_L47N_6	AA25		
6	IO_L48P_6	AB32		
6	IO_L48N_6	AB33		
6	IO_L49P_6	AB28		
6	IO_L49N_6	AB29		
6	IO_L50P_6	AA26		
6	IO_L50N_6	Y26		
6	IO_L51P_6	AA33		
6	IO_L51N_6/VREF_6	AA34		
6	IO_L52P_6	AB31		
6	IO_L52N_6	AA31		
6	IO_L53P_6	Y24		
6	IO_L53N_6	Y25		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AA30		
6	IO_L55P_6	Y33		
6	IO_L55N_6	Y34		
6	IO_L56P_6	Y28		
6	IO_L56N_6	W27		
6	IO_L57P_6	AA32		
6	IO_L57N_6/VREF_6	Y32		
6	IO_L58P_6	Y29		
6	IO_L58N_6	Y30		
6	IO_L59P_6	W24		
6	IO_L59N_6	W25		
6	IO_L60P_6	W31		
6	IO_L60N_6	W32		
6	IO_L85P_6	W28		
6	IO_L85N_6	W29		
6	IO_L86P_6	V26		
6	IO_L86N_6	V27		
6	IO_L87P_6	W33		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L43N_7	R37		
7	IO_L42P_7	R34		
7	IO_L42N_7	R35		
7	IO_L41P_7	U28		
7	IO_L41N_7	T28		
7	IO_L40P_7	R32		
7	IO_L40N_7/VREF_7	R33		
7	IO_L39P_7	P38		
7	IO_L39N_7	P39		
7	IO_L38P_7	T29		
7	IO_L38N_7	T30		
7	IO_L37P_7	N37		
7	IO_L37N_7	P37		
7	IO_L36P_7	P35		
7	IO_L36N_7	P36		
7	IO_L35P_7	T27		
7	IO_L35N_7	R27		
7	IO_L34P_7	P33		
7	IO_L34N_7/VREF_7	P34		
7	IO_L33P_7	N38		
7	IO_L33N_7	N39		
7	IO_L32P_7	R28		
7	IO_L32N_7	R29		
7	IO_L31P_7	N35		
7	IO_L31N_7	M36		
7	IO_L30P_7	N33		
7	IO_L30N_7	N34		
7	IO_L29P_7	R30		
7	IO_L29N_7	R31		
7	IO_L28P_7	M37		
7	IO_L28N_7/VREF_7	M38		
7	IO_L27P_7	M33		
7	IO_L27N_7	M34		
7	IO_L26P_7	P28		
7	IO_L26N_7	P29		
7	IO_L25P_7	L38		
7	IO_L25N_7	L39		
7	IO_L24P_7	L36		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L49P_0		G26		
0	IO_L50_0/No_Pair		D27		
0	IO_L53_0/No_Pair		D26		
0	IO_L54N_0		K25		
0	IO_L54P_0		L25		
0	IO_L55N_0		G25		
0	IO_L55P_0		H25		
0	IO_L56N_0		E26		
0	IO_L56P_0		E25		
0	IO_L57N_0		C25		
0	IO_L57P_0/VREF_0		C26		
0	IO_L58N_0		L24		
0	IO_L58P_0		M24		
0	IO_L59N_0		J24		
0	IO_L59P_0		K24		
0	IO_L60N_0		G24		
0	IO_L60P_0		H24		
0	IO_L64N_0		E24		
0	IO_L64P_0		F24		
0	IO_L65N_0		D24		
0	IO_L65P_0		C24		
0	IO_L66N_0		M22		
0	IO_L66P_0/VREF_0		M23		
0	IO_L67N_0		K23		
0	IO_L67P_0		L23		
0	IO_L68N_0		J23		
0	IO_L68P_0		H23		
0	IO_L69N_0		E23		
0	IO_L69P_0/VREF_0		F23		
0	IO_L73N_0		C23		
0	IO_L73P_0		D23		
0	IO_L74N_0/GCLK7P		K22		
0	IO_L74P_0/GCLK6S		J22		
0	IO_L75N_0/GCLK5P	BREFCLKN	F22		
0	IO_L75P_0/GCLK4S	BREFCLKP	G22		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L19P_5		AV32		
5	IO_L09N_5/VREF_5		AP32		
5	IO_L09P_5		AR32		
5	IO_L08N_5		AW33		
5	IO_L08P_5		AV33		
5	IO_L07N_5/VREF_5		AT33		
5	IO_L07P_5		AU33		
5	IO_L06N_5/VRP_5		AP33		
5	IO_L06P_5/VRN_5		AR33		
5	IO_L05_5/No_Pair		AN32		
5	IO_L03N_5/D4		AW34		
5	IO_L03P_5/D5		AY34		
5	IO_L02N_5/D6		AV34		
5	IO_L02P_5/D7		AU34		
5	IO_L01N_5/RDWR_B		AR34		
5	IO_L01P_5/CS_B		AT34		
6	IO_L01P_6/VRN_6		AW37		
6	IO_L01N_6/VRP_6		AV37		
6	IO_L02P_6		AW36		
6	IO_L02N_6		AV36		
6	IO_L03P_6		AY37		
6	IO_L03N_6/VREF_6		AY38		
6	IO_L04P_6		AU36		
6	IO_L04N_6		AT37		
6	IO_L05P_6		AU35		
6	IO_L05N_6		AT35		
6	IO_L06P_6		AW41		
6	IO_L06N_6		AW42		
6	IO_L73P_6		AV41		
6	IO_L73N_6		AV42		
6	IO_L74P_6		AW40		
6	IO_L74N_6		AV40		
6	IO_L75P_6		AU39		
6	IO_L75N_6/VREF_6		AU40		
6	IO_L76P_6		AU41		

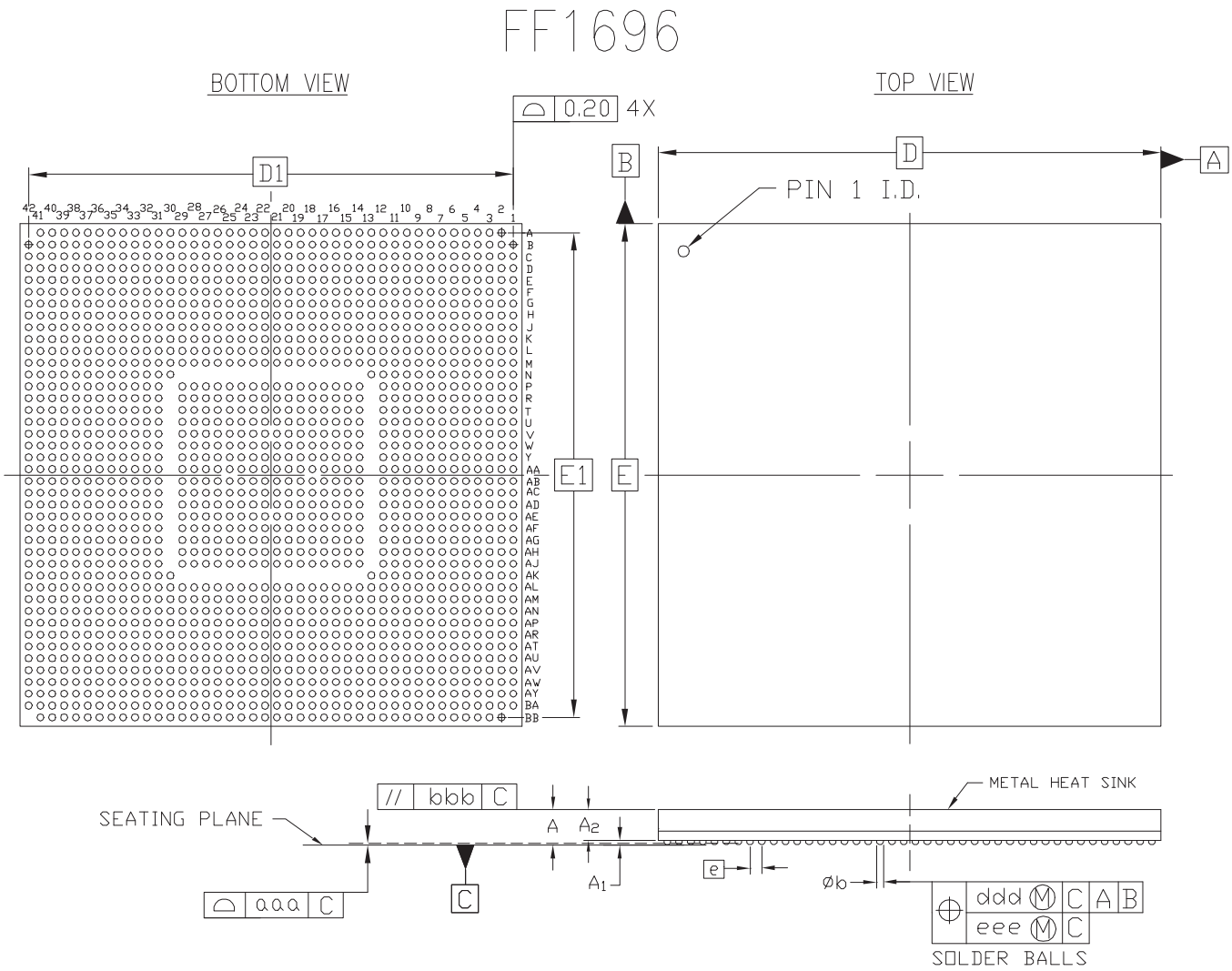
Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AE19		
N/A	GND		AE18		
N/A	GND		AE17		
N/A	GND		AE9		
N/A	GND		AE6		
N/A	GND		AF25		
N/A	GND		AF24		
N/A	GND		AF23		
N/A	GND		AF22		
N/A	GND		AF21		
N/A	GND		AF20		
N/A	GND		AF19		
N/A	GND		AF18		
N/A	GND		AG42		
N/A	GND		AG1		
N/A	GND		AH39		
N/A	GND		AH36		
N/A	GND		AH7		
N/A	GND		AH4		
N/A	GND		AL42		
N/A	GND		AL1		
N/A	GND		AM22		
N/A	GND		AM21		
N/A	GND		AN39		
N/A	GND		AN4		
N/A	GND		AP34		
N/A	GND		AP9		
N/A	GND		AR42		
N/A	GND		AR35		
N/A	GND		AR22		
N/A	GND		AR21		
N/A	GND		AR8		
N/A	GND		AR1		
N/A	GND		AT36		
N/A	GND		AT7		
N/A	GND		AU37		

FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	
A_1	0.40	0.50	0.60	
A_2			2.85	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

Figure 10: **FF1696 Flip-Chip Fine-Pitch BGA Package Specifications**