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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	812
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-5ff1148c

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

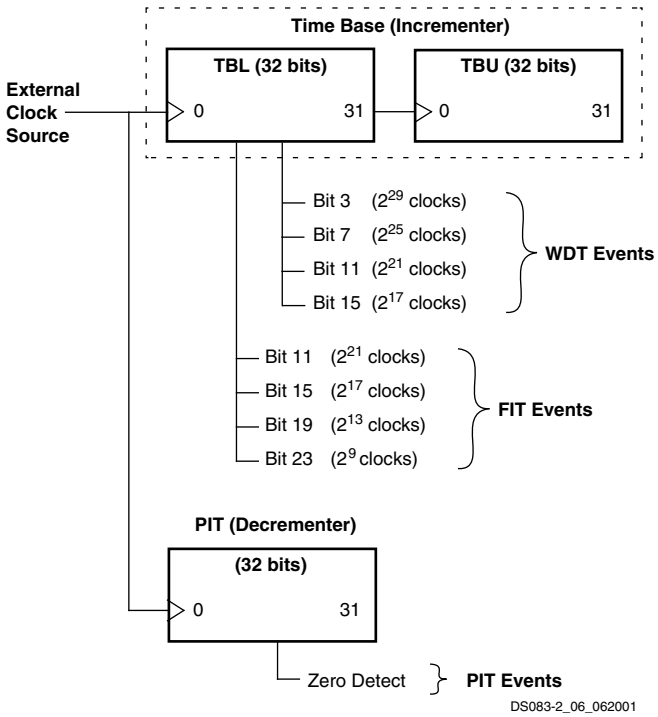

Figure 17: **Relationship of Timer Facilities to Base Clock**

Interrupts

The PPC405 provides an interface to an interrupt controller that is logically outside the PPC405 core. This controller combines the asynchronous interrupt inputs and presents them to the embedded core as a single interrupt signal. The sources of asynchronous interrupts are external signals, the JTAG/debug unit, and any implemented peripherals.

Debug Logic

All architected resources on the embedded PPC405 core can be accessed through the debug logic. Upon a debug event, the PPC405 core provides debug information to an external debug tool. Three different types of tools are supported depending on the debug mode: ROM monitors, JTAG debuggers, and instruction trace tools.

In internal debug mode, a debug event enables exception-handling software at a dedicated interrupt vector to take over the CPU core and communicate with a debug tool. The debug tool has read-write access to all registers and can set hardware or software breakpoints. ROM monitors typically use the internal debug mode.

In external debug mode, the CPU core enters stop state (stops instruction execution) when a debug event occurs. This mode offers a debug tool read-write access to all registers in the PPC405 core. Once the CPU core is in stop state, the debug tool can start the CPU core, step an instruction, freeze the timers, or set hardware or software break points. In addition to CPU core control, the debug logic is capable of writing instructions into the instruction cache, eliminating the need for external memory during initial board bring-up. Communication to a debug tool using external debug mode is through the JTAG port.

Debug wait mode offers the same functionality as external debug mode with one exception. In debug wait mode, the CPU core goes into wait state instead of stop state after a debug event. Wait state is identical to stop state until an interrupt occurs. In wait state, the PPC405 core can vector to an exception handler, service an interrupt and return to wait state. This mode is particularly useful when debugging real time control systems.

Real-time trace debug mode is always enabled. The debug logic continuously broadcasts instruction trace information to the trace port. When a debug event occurs, the debug logic signals an external debug tool to save instruction trace information before and after the event. The number of instructions traced depends on the trace tool.

Debug events signal the debug logic to stop the CPU core, put the CPU core in debug wait state, cause a debug exception or save instruction trace information.

Big Endian and Little Endian Support

The embedded PPC405 core supports big endian or little endian byte ordering for instructions stored in external memory. Since the PowerPC architecture is big endian internally, the ICU rearranges the instructions stored as little endian into the big endian format. Therefore, the instruction cache always contains instructions in big endian format so that the byte ordering is correct for the execution unit. This feature allows the 405 core to be used in systems designed to function in a little endian environment.

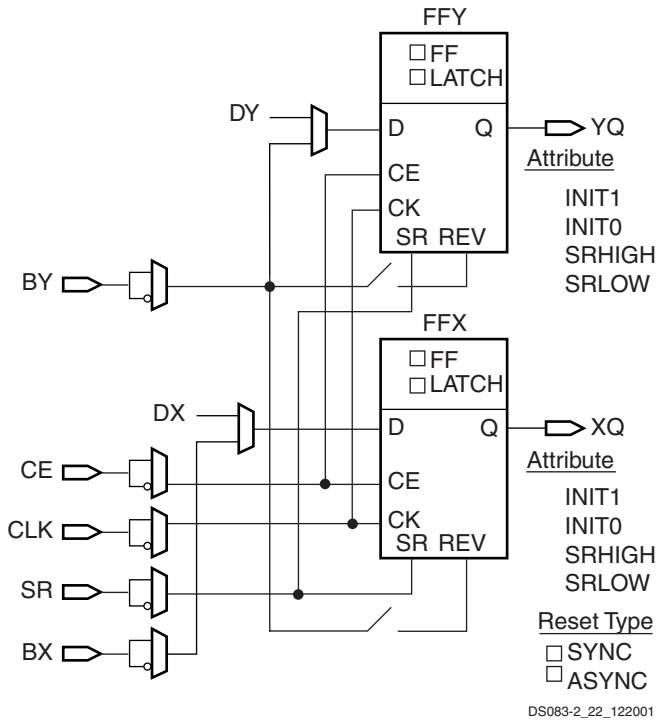

Figure 35: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM
- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: **Distributed SelectRAM+ Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

Table 36: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.07	0.08	0.09	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.04	0.05	0.05	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.00	0.00	0.00	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.29	0.33	0.36	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.36	0.41	0.45	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.31	0.36	0.40	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.33	0.37	0.41	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.31	0.36	0.40	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.31	0.36	0.40	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{ILVPECL\_25}$	0.69	0.80	0.88	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.14	0.16	0.18	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.15	0.17	0.19	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.12	0.13	0.15	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.59	0.68	0.74	ns
GTL Plus	GTLP	T_{IGTLP}	0.63	0.72	0.79	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.59	0.68	0.75	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.59	0.68	0.75	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.57	0.66	0.72	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.58	0.67	0.74	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.57	0.65	0.72	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.55	0.63	0.69	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.56	0.64	0.70	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.57	0.65	0.71	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.62	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.64	0.73	0.81	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	–0.05	–0.05	–0.06	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.00	0.00	0.00	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.07	0.09	0.09	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.13	0.15	0.17	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.00	0.00	0.00	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.07	0.09	0.09	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.13	0.15	0.17	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.59	0.68	0.75	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Pro Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 38) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

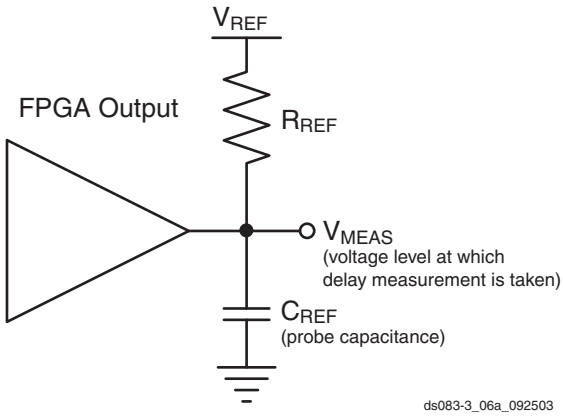

Figure 6: **Generalized Test Setup**

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.65	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	0
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Master/Slave SelectMAP Parameters

Figure 10 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

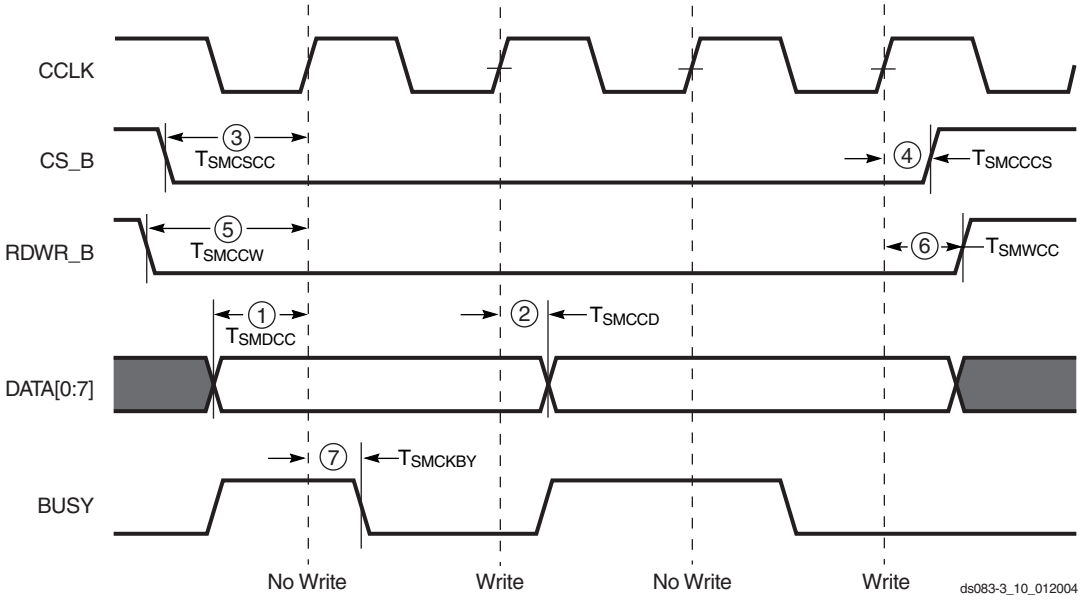

Figure 10: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 51: **SelectMAP Mode Write Timing Characteristics**

	Description	Device	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	XC2VP2	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
		XC2VP4			5.0/0.0	ns, min
		XC2VP7			5.0/0.0	ns, min
		XC2VP20			5.0/0.0	ns, min
		XC2VPX20			5.0/0.0	ns, min
		XC2VP30			5.0/0.0	ns, min
		XC2VP40			5.0/0.0	ns, min
		XC2VP50			5.0/0.0	ns, min
		XC2VP70			6.0/0.0	ns, min
		XC2VPX70			6.0/0.0	ns, min
		XC2VP100			7.5/0.0	ns, min
	CS_B setup/hold		3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold		5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay		7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency			$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency			$F_{CC\_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake			F_{CCNH}	50	MHz, max

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM

Table 54: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2VP2	3.19	3.52	3.82	ns
		XC2VP4	3.39	3.91	4.27	ns
		XC2VP7	3.59	4.00	4.36	ns
		XC2VP20	3.62	4.08	4.46	ns
		XC2VPX20	3.62	4.08	4.46	ns
		XC2VP30	3.73	4.12	4.50	ns
		XC2VP40	3.89	4.28	4.67	ns
		XC2VP50	4.00	4.43	4.84	ns
		XC2VP70	4.38	4.87	5.33	ns
		XC2VPX70	4.38	4.87	5.33	ns
		XC2VP100	N/A	5.32	5.82	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
VTRXPAD#	Input	Receive termination supply for the RocketIO multi-gigabit transceiver (1.8V - 2.8V).
VTTXPAD#	Input	Transmit termination supply for the RocketIO multi-gigabit transceiver (1.8V - 2.8V).
GNDA#	Input	Ground for the analog circuitry of the RocketIO multi-gigabit transceiver.
RXPPAD#	Input	Positive differential receive port of the RocketIO multi-gigabit transceiver.
RXNPAD#	Input	Negative differential receive port of the RocketIO multi-gigabit transceiver.
TXPPAD#	Output	Positive differential transmit port of the RocketIO multi-gigabit transceiver.
TXNPAD#	Output	Negative differential transmit port of the RocketIO multi-gigabit transceiver.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).
2. Virtex-II Pro X devices XC2VPX20 and XC2VPX70 only. Each BREFCLK(N/P) differential clock input pair takes the place of one regular Virtex-II Pro dual-function IO/GCLKx(S/P) pair on each side of the chip (top or bottom). For RocketIO BREFCLK, see section BREFCLK Pin Definitions (RocketIO Only) immediately following.

BREFCLK Pin Definitions (RocketIO Only)

These dedicated clocks use the same clock inputs for all packages:

Top	BREFCLK	P	GCLK4S	Bottom	BREFCLK	P	GCLK6P
		N	GCLK5P			N	GCLK7S
	BREFCLK2	P	GCLK2S		BREFCLK2	P	GCLK0P
		N	GCLK3P			N	GCLK1S

For detailed information about using BREFCLK/BREFCLK2, including routing considerations and pin numbers for all package types, refer to Chapter 2, "Digital Design Considerations," in the **RocketIO Transceiver User Guide**.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	K7			
7	VCCO_7	J7			
7	VCCO_7	H6			
7	VCCO_7	G6			
N/A	CCLK	W20			
N/A	PROG_B	B1			
N/A	DONE	Y18			
N/A	M0	Y4			
N/A	M1	W3			
N/A	M2	Y5			
N/A	TCK	B22			
N/A	TDI	D3			
N/A	TDO	D20			
N/A	TMS	A21			
N/A	PWRDWN_B	Y19			
N/A	HSWAP_EN	A2			
N/A	RSVD	C18			
N/A	VBATT	C19			
N/A	DXP	C4			
N/A	DXN	C5			
N/A	AVCCAUXTX4	B4	NC	NC	
N/A	VTTXPAD4	B3	NC	NC	
N/A	TXNPAD4	A3	NC	NC	
N/A	TXPPAD4	A4	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	RXPPAD4	A5	NC	NC	
N/A	RXNPAD4	A6	NC	NC	
N/A	VTRXPAD4	B5	NC	NC	
N/A	AVCCAUXRX4	B6	NC	NC	
N/A	AVCCAUXTX6	B8			
N/A	VTTXPAD6	B7			
N/A	TXNPAD6	A7			
N/A	TXPPAD6	A8			
N/A	GNDA6	C9			
N/A	RXPPAD6	A9			
N/A	RXNPAD6	A10			

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 7, XC2VP20, XC2VP30, and XC2VP40 Virtex-II Pro devices are available in the FG676/FGG676 fine-pitch BGA package. The pins in these devices are the same, except for the differences shown in the "No Connects" column. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L01N_0/VRP_0	E5			
0	IO_L01P_0/VRN_0	D5			
0	IO_L02N_0	E6			
0	IO_L02P_0	D6			
0	IO_L03N_0	G7			
0	IO_L03P_0/VREF_0	F7			
0	IO_L05_0/No_Pair	E7			
0	IO_L06N_0	D7			
0	IO_L06P_0	C7			
0	IO_L07N_0	H8			
0	IO_L07P_0	G8			
0	IO_L09N_0	F8			
0	IO_L09P_0/VREF_0	E8			
0	IO_L37N_0	B8			
0	IO_L37P_0	A8			
0	IO_L39N_0	H9			
0	IO_L39P_0	G9			
0	IO_L43N_0	F9			
0	IO_L43P_0	E9			
0	IO_L45N_0	D9			
0	IO_L45P_0/VREF_0	C9			
0	IO_L46N_0	H10			
0	IO_L46P_0	H11			
0	IO_L48N_0	E10			
0	IO_L48P_0	E11			
0	IO_L49N_0	D10			
0	IO_L49P_0	C10			
0	IO_L50_0/No_Pair	G11			
0	IO_L53_0/No_Pair	F11			
0	IO_L54N_0	J12			
0	IO_L54P_0	H12			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L55P_6	T2			
6	IO_L55N_6	T1			
6	IO_L57P_6	R9			
6	IO_L57N_6/VREF_6	R8			
6	IO_L59P_6	R6			
6	IO_L59N_6	P6			
6	IO_L60P_6	R5			
6	IO_L60N_6	R4			
6	IO_L85P_6	R2			
6	IO_L85N_6	R1			
6	IO_L87P_6	P9			
6	IO_L87N_6/VREF_6	P8			
6	IO_L89P_6	P5			
6	IO_L89N_6	P4			
6	IO_L90P_6	P3			
6	IO_L90N_6	P2			
7	IO_L90P_7	N2			
7	IO_L90N_7	N3			
7	IO_L88P_7	N4			
7	IO_L88N_7/VREF_7	N5			
7	IO_L86P_7	N8			
7	IO_L86N_7	N9			
7	IO_L85P_7	M1			
7	IO_L85N_7	M2			
7	IO_L60P_7	M4			
7	IO_L60N_7	M5			
7	IO_L58P_7	N6			
7	IO_L58N_7/VREF_7	M6			
7	IO_L56P_7	M8			
7	IO_L56N_7	M9			
7	IO_L55P_7	L1			
7	IO_L55N_7	L2			
7	IO_L54P_7	L5			
7	IO_L54N_7	L6			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L53_0/No_Pair		A21	NC		
0	IO_L54N_0		H18	NC		
0	IO_L54P_0		G18	NC		
0	IO_L56N_0		C21	NC		
0	IO_L56P_0		C20	NC		
0	IO_L57N_0		J17	NC		
0	IO_L57P_0/VREF_0		H17	NC		
0	IO_L67N_0		E17			
0	IO_L67P_0		D17			
0	IO_L68N_0		D18			
0	IO_L68P_0		C18			
0	IO_L69N_0		J16			
0	IO_L69P_0/VREF_0		H16			
0	IO_L73N_0		E16			
0	IO_L73P_0		D16			
0	IO_L74N_0/GCLK7P		C16			
0	IO_L74P_0/GCLK6S		B16			
0	IO_L75N_0/GCLK5P	BREFCLKN	G16			
0	IO_L75P_0/GCLK4S	BREFCLKP	F16			
1	IO_L75N_1/GCLK3P		F15			
1	IO_L75P_1/GCLK2S		G15			
1	IO_L74N_1/GCLK1P		B15			
1	IO_L74P_1/GCLK0S		C15			
1	IO_L73N_1		D15			
1	IO_L73P_1		E15			
1	IO_L69N_1/VREF_1		H15			
1	IO_L69P_1		J15			
1	IO_L68N_1		C13			
1	IO_L68P_1		D13			
1	IO_L67N_1		D14			
1	IO_L67P_1		E14			
1	IO_L57N_1/VREF_1		H14	NC		
1	IO_L57P_1		J14	NC		
1	IO_L56N_1		C11	NC		
1	IO_L56P_1		C10	NC		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L13P_7	D28		
7	IO_L13N_7	E28		
7	IO_L12P_7	C33		
7	IO_L12N_7	C34		
7	IO_L11P_7	J27		
7	IO_L11N_7	K27		
7	IO_L10P_7	B30		
7	IO_L10N_7/VREF_7	C30		
7	IO_L09P_7	C28		
7	IO_L09N_7	C29		
7	IO_L08P_7	H27		
7	IO_L08N_7	H28		
7	IO_L07P_7	A32		
7	IO_L07N_7	B32		
7	IO_L06P_7	A31		
7	IO_L06N_7	B31		
7	IO_L05P_7	D27		
7	IO_L05N_7	E27		
7	IO_L04P_7	A29		
7	IO_L04N_7/VREF_7	B29		
7	IO_L03P_7	A28		
7	IO_L03N_7	B28		
7	IO_L02P_7	D26		
7	IO_L02N_7	C26		
7	IO_L01P_7/VRN_7	B26		
7	IO_L01N_7/VRP_7	B27		
7	VCCO_7	E33		
7	VCCO_7	R31		
7	VCCO_7	L31		
7	VCCO_7	G31		
7	VCCO_7	C31		
7	VCCO_7	R27		
7	VCCO_7	L27		
7	VCCO_7	G27		
7	VCCO_7	C27		
7	VCCO_7	J26		
7	VCCO_7	M24		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L66P_4/VREF_4	AU19		
4	IO_L67N_4	AM19		
4	IO_L67P_4	AL19		
4	IO_L68N_4	AK19		
4	IO_L68P_4	AJ19		
4	IO_L69N_4	AP19		
4	IO_L69P_4/VREF_4	AN19		
4	IO_L73N_4	AT19		
4	IO_L73P_4	AR19		
4	IO_L74N_4/GCLK3S	AH20		
4	IO_L74P_4/GCLK2P	AG20		
4	IO_L75N_4/GCLK1S	AL20		
4	IO_L75P_4/GCLK0P	AK20		
5	IO_L75N_5/GCLK7S	AR20		
5	IO_L75P_5/GCLK6P	AT20		
5	IO_L74N_5/GCLK5S	AH21		
5	IO_L74P_5/GCLK4P	AJ21		
5	IO_L73N_5	AP20		
5	IO_L73P_5	AP21		
5	IO_L69N_5/VREF_5	AU21		
5	IO_L69P_5	AU22		
5	IO_L68N_5	AK21		
5	IO_L68P_5	AL21		
5	IO_L67N_5	AR21		
5	IO_L67P_5	AT21		
5	IO_L66N_5/VREF_5	AN21		
5	IO_L66P_5	AN22		
5	IO_L65N_5	AM20		
5	IO_L65P_5	AM21		
5	IO_L64N_5	AR22		
5	IO_L64P_5	AT22		
5	IO_L60N_5	AP22		
5	IO_L60P_5	AR23		
5	IO_L59N_5	AG21		
5	IO_L59P_5	AG22		
5	IO_L58N_5	AL22		
5	IO_L58P_5	AM22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	VCCO_2	F8		
2	VCCO_2	U7		
2	VCCO_2	Y5		
2	VCCO_2	N4		
2	VCCO_2	J4		
2	VCCO_2	E4		
2	VCCO_2	U3		
2	VCCO_2	E1		
1	VCCO_1	N14		
1	VCCO_1	K13		
1	VCCO_1	F13		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	K17		
1	VCCO_1	F17		
1	VCCO_1	P16		
1	VCCO_1	N16		
1	VCCO_1	P15		
1	VCCO_1	N15		
0	VCCO_0	K27		
0	VCCO_0	F27		
0	VCCO_0	N26		
0	VCCO_0	P25		
0	VCCO_0	N25		
0	VCCO_0	P24		
0	VCCO_0	N24		
0	VCCO_0	P23		
0	VCCO_0	K23		
0	VCCO_0	F23		
0	VCCO_0	P22		
0	VCCO_0	P21		
N/A	CCLK	AJ10		
N/A	PROG_B	D32		
N/A	DONE	AJ11		
N/A	M0	AP31		
N/A	M1	AJ30		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L19P_5		AV32		
5	IO_L09N_5/VREF_5		AP32		
5	IO_L09P_5		AR32		
5	IO_L08N_5		AW33		
5	IO_L08P_5		AV33		
5	IO_L07N_5/VREF_5		AT33		
5	IO_L07P_5		AU33		
5	IO_L06N_5/VRP_5		AP33		
5	IO_L06P_5/VRN_5		AR33		
5	IO_L05_5/No_Pair		AN32		
5	IO_L03N_5/D4		AW34		
5	IO_L03P_5/D5		AY34		
5	IO_L02N_5/D6		AV34		
5	IO_L02P_5/D7		AU34		
5	IO_L01N_5/RDWR_B		AR34		
5	IO_L01P_5/CS_B		AT34		
6	IO_L01P_6/VRN_6		AW37		
6	IO_L01N_6/VRP_6		AV37		
6	IO_L02P_6		AW36		
6	IO_L02N_6		AV36		
6	IO_L03P_6		AY37		
6	IO_L03N_6/VREF_6		AY38		
6	IO_L04P_6		AU36		
6	IO_L04N_6		AT37		
6	IO_L05P_6		AU35		
6	IO_L05N_6		AT35		
6	IO_L06P_6		AW41		
6	IO_L06N_6		AW42		
6	IO_L73P_6		AV41		
6	IO_L73N_6		AV42		
6	IO_L74P_6		AW40		
6	IO_L74N_6		AV40		
6	IO_L75P_6		AU39		
6	IO_L75N_6/VREF_6		AU40		
6	IO_L76P_6		AU41		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	VCCO_2	F4	
1	VCCO_1	R21	
1	VCCO_1	P21	
1	VCCO_1	R20	
1	VCCO_1	P20	
1	VCCO_1	R19	
1	VCCO_1	P19	
1	VCCO_1	R18	
1	VCCO_1	P18	
1	VCCO_1	H18	
1	VCCO_1	D18	
1	VCCO_1	P17	
1	VCCO_1	H14	
1	VCCO_1	D14	
1	VCCO_1	M13	
1	VCCO_1	D10	
0	VCCO_0	D33	
0	VCCO_0	M30	
0	VCCO_0	H29	
0	VCCO_0	D29	
0	VCCO_0	P26	
0	VCCO_0	R25	
0	VCCO_0	P25	
0	VCCO_0	H25	
0	VCCO_0	D25	
0	VCCO_0	R24	
0	VCCO_0	P24	
0	VCCO_0	R23	
0	VCCO_0	P23	
0	VCCO_0	R22	
0	VCCO_0	P22	
N/A	CCLK	AM10	
N/A	PROG_B	J33	
N/A	DONE	AN10	
N/A	M0	AP33	
N/A	M1	AN33	