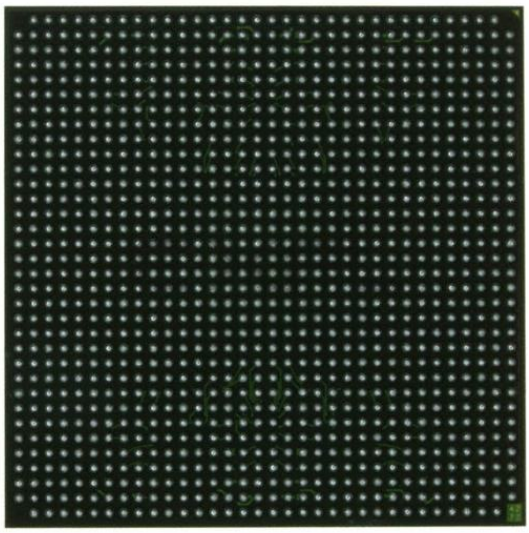

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 5904 |
| Number of Logic Elements/Cells | 53136 |
| Total RAM Bits | 4276224 |
| Number of I/O | 692 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp50-5ff1152i |

RXP and RXN as shown in Figure 5. This supports multiple termination styles, including high-side, low-side, and differential (floating or active). This configuration supports receiver termination compatible to Virtex-II Pro devices, using a CML (high-side) termination to an active supply of 1.8V – 2.5V. For DC coupling of two Virtex-II Pro X devices, a 1.5V CML termination for VTRX is recommended.

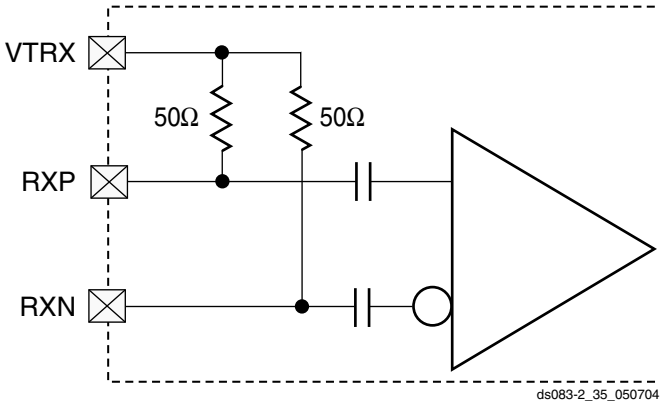


*Figure 5:* **RocketIO X Receive Termination**

## PCS

### *Fabric Data Interface*

Internally, the PCS operates in either 2-byte mode (16/20 bits) or 4-byte mode (32/40 bits). When in 2-byte mode, the FPGA fabric interface can either be 1, 2, or 4 bytes wide. When in 4-byte mode, the FPGA fabric interface can either be 4 or 8 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 2 summarizes the USRCLK2-to-USRCLK ratios for the different possible combinations of data widths.

*Table 2:* **Clock Ratios for Various Data Widths**

| Fabric Data Width | Frequency Ratio of USRCLK:USRCLK2 | |
|---|---|---|
| | 2-Byte Internal Data Width | 4-Byte Internal Data Width |
| 1 byte | 1:2 (1) | N/A |
| 2 byte | 1:1 | N/A |
| 4 byte | 2:1 (1) | 1:1 |
| 8 byte | N/A | 2:1 (1) |

**Notes:**
1. Each edge of slower clock must align with falling edge of faster clock.

As a general guide, use 2-byte internal data width mode when the serial speed is below 5 Gb/s, and 4-byte internal data width mode when the serial speed is greater than 5 Gb/s. In 2-byte mode, the PCS processes 4-byte data every other byte.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

### *FPGA Transmit Interface*

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

### *64B/66B Encoder/Decoder*

The RocketIO X PCS features a 64B/66B encoder/decoder, scrambler/descrambler, and gearbox functions that can be bypassed as needed. The encoder is compliant with IEEE 802.3ae specifications.

### *Scrambler/Gearbox*

The bypassable scrambler operates on the read side of the transmit FIFO. The scrambler uses the following generator polynomial to scramble 64B/66B payload data:

$$G(x) = 1 + x^{39} + x^{58}$$

The scrambler works in conjunction with the gearbox, which frames 64B/66B data for the PMA. The gearbox should always be enabled when using the 64B/66B protocal.

### Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

### Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

### 8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

### 8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

### Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

#### Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

# Configuration

Virtex-II Pro devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1, and M0 are dedicated pins. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or $V_{CCAUX}$. The mode pins should not be toggled during and after configuration.

An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the Boundary-Scan pins: TDI, TDO, TMS, and TCK. (The TDO pin is open-drain and does not have an internal pull-up resistor.) Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and Boundary-Scan pins are independent of the $V_{CCO}$. The auxiliary power supply ($V_{CCAUX}$) of 2.5V is used for these pins. All configuration pins are LVCMOS25 12mA. See Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

A "persist" option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the Boundary-Scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

## Configuration Modes

Virtex-II Pro supports the following five configuration modes:

- Slave-Serial Mode
- Master-Serial Mode
- Slave SelectMAP Mode
- Master SelectMAP Mode
- Boundary-Scan (JTAG, IEEE 1532) Mode

Refer to Table 32, page 57.

A detailed description of configuration modes is provided in the *Virtex-II Pro Platform FPGA User Guide.*

### *Slave-Serial Mode*

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Slave-serial mode is selected by applying [111] to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

### *Master-Serial Mode*

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II Pro FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the falling CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

### *Slave SelectMAP Mode*

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II Pro FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II Pro FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

## IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

*Table 37:* **IOB Output Switching Characteristics**

| | | Speed Grade | | | |
|---|---|---|---|---|---|
| **Description** | **Symbol** | **-7** | **-6** | **-5** | **Units** |
| **Propagation Delays** | | | | | |
| O input to Pad | $T_{IOOP}$ | 1.58 | 1.68 | 1.85 | ns, max |
| O input to Pad via transparent latch | $T_{IOOLP}$ | 1.65 | 1.82 | 1.99 | ns, max |
| **3-State Delays** | | | | | |
| T input to Pad high-impedance(2) | $T_{IOTHZ}$ | 1.23 | 1.35 | 1.51 | ns, max |
| T input to valid data on Pad | $T_{IOTP}$ | 1.51 | 1.63 | 1.78 | ns, max |
| T input to Pad high-impedance via transparent latch(2) | $T_{IOTLPHZ}$ | 1.08 | 1.22 | 1.36 | ns, max |
| T input to valid data on Pad via transparent latch | $T_{IOTLPON}$ | 1.56 | 1.69 | 1.85 | ns, max |
| GTS to Pad high-impedance(2) | $T_{GTS}$ | 4.11 | 4.73 | 5.20 | ns, max |
| **Sequential Delays** | | | | | |
| Clock CLK to Pad | $T_{IOCKP}$ | 1.59 | 1.76 | 1.93 | ns, max |
| Clock CLK to Pad high-impedance (synchronous)(2) | $T_{IOCKHZ}$ | 1.39 | 1.55 | 1.73 | ns, max |
| Clock CLK to valid data on Pad (synchronous) | $T_{IOCKON}$ | 1.67 | 1.82 | 2.00 | ns, max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| O input | $T_{IOOCK}/T_{IOCKO}$ | 0.23/ 0.12 | 0.26/ 0.14 | 0.29/ 0.15 | ns, min |
| OCE input | $T_{IOOCECK}/T_{IOCKOCE}$ | 0.39/ 0.01 | 0.44/ 0.01 | 0.49/ 0.01 | ns, min |
| SR input (OFF) | $T_{IOSRCKO}/T_{IOCKOSR}$ | 0.52/ 0.00 | 0.57/ 0.00 | 0.75/ 0.00 | ns, min |
| 3–State Setup Times, T input | $T_{IOTCK}/T_{IOCKT}$ | 0.23/ 0.12 | 0.26/ 0.14 | 0.29/ 0.15 | ns, min |
| 3-State Setup Times, TCE input | $T_{IOTCECK}/T_{IOCKTCE}$ | 0.39/ 0.01 | 0.44/ 0.01 | 0.49/ 0.01 | ns, min |
| 3-State Setup Times, SR input (TFF) | $T_{IOSRCKT}/T_{IOCKTSR}$ | 0.52/ 0.00 | 0.57/ 0.00 | 0.75/ 0.00 | ns, min |
| **Set/Reset Delays** | | | | | |
| Minimum Pulse Width, SR inputs (asynchronous) | $T_{RPW}$ | 0.37 | 0.40 | 0.45 | ns, min |
| SR input to Pad (asynchronous) | $T_{IOSRP}$ | 2.33 | 2.56 | 2.83 | ns, max |
| SR input to Pad high-impedance (asynchronous)(2) | $T_{IOSRHZ}$ | 1.97 | 2.16 | 2.41 | ns, max |
| SR input to valid data on Pad (asynchronous) | $T_{IOSRON}$ | 2.24 | 2.44 | 2.69 | ns, max |
| GSR to Pad | $T_{IOGSRQ}$ | 5.87 | 6.75 | 7.43 | ns, max |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

## IOB Output Switching Characteristics Standard Adjustments

Table 38 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, $C_{REF}$. Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

*Table 38:* **IOB Output Switching Characteristics Standard Adjustments**

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA | LVTTL_S2 | $T_{OLVTTL\_S2}$ | 5.42 | 6.24 | 6.86 | ns |
| LVTTL, Slow, 4 mA | LVTTL_S4 | $T_{OLVTTL\_S4}$ | 3.09 | 3.55 | 3.91 | ns |
| LVTTL, Slow, 6 mA | LVTTL_S6 | $T_{OLVTTL\_S6}$ | 2.26 | 2.60 | 2.86 | ns |
| LVTTL, Slow, 8 mA | LVTTL_S8 | $T_{OLVTTL\_S8}$ | 1.47 | 1.69 | 1.86 | ns |
| LVTTL, Slow, 12 mA | LVTTL_S12 | $T_{OLVTTL\_S12}$ | 1.02 | 1.18 | 1.29 | ns |
| LVTTL, Slow, 16 mA | LVTTL_S16 | $T_{OLVTTL\_S16}$ | 0.46 | 0.53 | 0.58 | ns |
| LVTTL, Slow, 24 mA | LVTTL_S24 | $T_{OLVTTL\_S24}$ | 0.37 | 0.42 | 0.47 | ns |
| LVTTL, Fast, 2 mA | LVTTL_F2 | $T_{OLVTTL\_F2}$ | 4.42 | 5.09 | 5.59 | ns |
| LVTTL, Fast, 4 mA | LVTTL_F4 | $T_{OLVTTL\_F4}$ | 1.95 | 2.24 | 2.46 | ns |
| LVTTL, Fast, 6 mA | LVTTL_F6 | $T_{OLVTTL\_F6}$ | 1.10 | 1.26 | 1.39 | ns |
| LVTTL, Fast, 8 mA | LVTTL_F8 | $T_{OLVTTL\_F8}$ | 0.40 | 0.46 | 0.51 | ns |
| LVTTL, Fast, 12 mA | LVTTL_F12 | $T_{OLVTTL\_F12}$ | 0.24 | 0.27 | 0.30 | ns |
| LVTTL, Fast, 16 mA | LVTTL_F16 | $T_{OLVTTL\_F16}$ | 0.05 | 0.06 | 0.07 | ns |
| LVTTL, Fast, 24 mA | LVTTL_F24 | $T_{OLVTTL\_F24}$ | –0.01 | –0.01 | –0.01 | ns |
| LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA | LVCMOS33_S2 | $T_{OLVCMOS33\_S2}$ | 5.42 | 6.23 | 6.86 | ns |
| LVCMOS, 3.3V, Slow, 4 mA | LVCMOS33_S4 | $T_{OLVCMOS33\_S4}$ | 3.14 | 3.61 | 3.97 | ns |
| LVCMOS, 3.3V, Slow, 6 mA | LVCMOS33_S6 | $T_{OLVCMOS33\_S6}$ | 2.26 | 2.60 | 2.86 | ns |
| LVCMOS, 3.3V, Slow, 8 mA | LVCMOS33_S8 | $T_{OLVCMOS33\_S8}$ | 1.47 | 1.69 | 1.86 | ns |
| LVCMOS, 3.3V, Slow, 12 mA | LVCMOS33_S12 | $T_{OLVCMOS33\_S12}$ | 1.03 | 1.18 | 1.30 | ns |
| LVCMOS, 3.3V, Slow, 16 mA | LVCMOS33_S16 | $T_{OLVCMOS33\_S16}$ | 0.45 | 0.52 | 0.57 | ns |
| LVCMOS, 3.3V, Slow, 24 mA | LVCMOS33_S24 | $T_{OLVCMOS33\_S24}$ | 0.39 | 0.44 | 0.49 | ns |
| LVCMOS, 3.3V, Fast, 2 mA | LVCMOS33_F2 | $T_{OLVCMOS33\_F2}$ | 4.46 | 5.13 | 5.64 | ns |
| LVCMOS, 3.3V, Fast, 4 mA | LVCMOS33_F4 | $T_{OLVCMOS33\_F4}$ | 1.96 | 2.25 | 2.48 | ns |
| LVCMOS, 3.3V, Fast, 6 mA | LVCMOS33_F6 | $T_{OLVCMOS33\_F6}$ | 1.11 | 1.28 | 1.40 | ns |
| LVCMOS, 3.3V, Fast, 8 mA | LVCMOS33_F8 | $T_{OLVCMOS33\_F8}$ | 0.41 | 0.47 | 0.52 | ns |
| LVCMOS, 3.3V, Fast, 12 mA | LVCMOS33_F12 | $T_{OLVCMOS33\_F12}$ | 0.23 | 0.26 | 0.28 | ns |
| LVCMOS, 3.3V, Fast, 16 mA | LVCMOS33_F16 | $T_{OLVCMOS33\_F16}$ | 0.02 | 0.02 | 0.03 | ns |
| LVCMOS, 3.3V, Fast, 24 mA | LVCMOS33_F24 | $T_{OLVCMOS33\_F24}$ | –0.07 | –0.08 | –0.09 | ns |
| LVCMOS, 2.5V, Slow, 2 mA | LVCMOS25_S2 | $T_{OLVCMOS25\_S2}$ | 4.12 | 4.74 | 5.21 | ns |
| LVCMOS, 2.5V, Slow, 4 mA | LVCMOS25_S4 | $T_{OLVCMOS25\_S4}$ | 2.43 | 2.80 | 3.07 | ns |
| LVCMOS, 2.5V, Slow, 6 mA | LVCMOS25_S6 | $T_{OLVCMOS25\_S6}$ | 1.76 | 2.02 | 2.22 | ns |
| LVCMOS, 2.5V, Slow, 8 mA | LVCMOS25_S8 | $T_{OLVCMOS25\_S8}$ | 1.04 | 1.19 | 1.31 | ns |
| LVCMOS, 2.5V, Slow, 12 mA | LVCMOS25_S12 | $T_{OLVCMOS25\_S12}$ | 0.76 | 0.87 | 0.96 | ns |
| LVCMOS, 2.5V, Slow, 16 mA | LVCMOS25_S16 | $T_{OLVCMOS25\_S16}$ | 0.41 | 0.47 | 0.52 | ns |
| LVCMOS, 2.5V, Slow, 24 mA | LVCMOS25_S24 | $T_{OLVCMOS25\_S24}$ | 0.23 | 0.26 | 0.28 | ns |
| LVCMOS, 2.5V, Fast, 2 mA | LVCMOS25_F2 | $T_{OLVCMOS25\_F2}$ | 3.29 | 3.78 | 4.16 | ns |
| LVCMOS, 2.5V, Fast, 4 mA | LVCMOS25_F4 | $T_{OLVCMOS25\_F4}$ | 1.31 | 1.50 | 1.65 | ns |

*Table 5:* **FG256/FGG256 — XC2VP2 and XC2VP4**

| Bank | Pin Description | Pin Number |
|---|---|---|
| N/A | AVCCAUXRX7 | B13 |
| N/A | AVCCAUXRX18 | R13 |
| N/A | VTRXPAD18 | R12 |
| N/A | RXNPAD18 | T13 |
| N/A | RXPPAD18 | T12 |
| N/A | GNDA18 | P11 |
| N/A | TXPPAD18 | T11 |
| N/A | TXNPAD18 | T10 |
| N/A | VTTXPAD18 | R10 |
| N/A | AVCCAUXTX18 | R11 |
| N/A | AVCCAUXRX19 | R7 |
| N/A | VTRXPAD19 | R6 |
| N/A | RXNPAD19 | T7 |
| N/A | RXPPAD19 | T6 |
| N/A | GNDA19 | P6 |
| N/A | TXPPAD19 | T5 |
| N/A | TXNPAD19 | T4 |
| N/A | VTTXPAD19 | R4 |
| N/A | AVCCAUXTX19 | R5 |
| | | |
| N/A | VCCINT | N4 |
| N/A | VCCINT | N13 |
| N/A | VCCINT | M5 |
| N/A | VCCINT | M12 |
| N/A | VCCINT | E5 |
| N/A | VCCINT | E12 |
| N/A | VCCINT | D4 |
| N/A | VCCINT | D13 |
| N/A | VCCAUX | R16 |
| N/A | VCCAUX | R1 |
| N/A | VCCAUX | B16 |
| N/A | VCCAUX | B1 |
| N/A | GND | T16 |
| N/A | GND | T1 |
| N/A | GND | R2 |

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| N/A | AVCCAUXRX19 | AE15 | | | |
| N/A | VTRXPAD19 | AE16 | | | |
| N/A | RXNPAD19 | AF15 | | | |
| N/A | RXPPAD19 | AF16 | | | |
| N/A | GNDA19 | AD16 | | | |
| N/A | TXPPAD19 | AF17 | | | |
| N/A | TXNPAD19 | AF18 | | | |
| N/A | VTTXPAD19 | AE18 | | | |
| N/A | AVCCAUXTX19 | AE17 | | | |
| N/A | AVCCAUXRX21 | AE20 | NC | NC | |
| N/A | VTRXPAD21 | AE21 | NC | NC | |
| N/A | RXNPAD21 | AF20 | NC | NC | |
| N/A | RXPPAD21 | AF21 | NC | NC | |
| N/A | GNDA21 | AD22 | NC | NC | |
| N/A | TXPPAD21 | AF22 | NC | NC | |
| N/A | TXNPAD21 | AF23 | NC | NC | |
| N/A | VTTXPAD21 | AE23 | NC | NC | |
| N/A | AVCCAUXTX21 | AE22 | NC | NC | |
| | | | | | |
| N/A | VCCINT | H8 | | | |
| N/A | VCCINT | J9 | | | |
| N/A | VCCINT | K9 | | | |
| N/A | VCCINT | U9 | | | |
| N/A | VCCINT | V9 | | | |
| N/A | VCCINT | W8 | | | |
| N/A | VCCINT | H19 | | | |
| N/A | VCCINT | J10 | | | |
| N/A | VCCINT | J17 | | | |
| N/A | VCCINT | J18 | | | |
| N/A | VCCINT | K11 | | | |
| N/A | VCCINT | K16 | | | |
| N/A | VCCINT | K18 | | | |
| N/A | VCCINT | L10 | | | |
| N/A | VCCINT | L17 | | | |
| N/A | VCCINT | T10 | | | |
| N/A | VCCINT | T17 | | | |
| N/A | VCCINT | U11 | | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | GND | AU3 | | |
| N/A | GND | AT3 | | |
| N/A | GND | D3 | | |
| N/A | GND | C3 | | |
| N/A | GND | B3 | | |
| N/A | GND | AN12 | | |
| N/A | GND | G12 | | |
| N/A | GND | C12 | | |
| N/A | GND | Y10 | | |
| N/A | GND | AH9 | | |
| N/A | GND | AD9 | | |
| N/A | GND | T9 | | |
| N/A | GND | M9 | | |
| N/A | GND | AU8 | | |
| N/A | GND | AN8 | | |
| N/A | GND | G8 | | |
| N/A | GND | C8 | | |
| N/A | GND | Y6 | | |
| N/A | GND | AM5 | | |
| N/A | GND | AH5 | | |
| N/A | GND | T17 | | |
| N/A | GND | AT16 | | |
| N/A | GND | AN16 | | |
| N/A | GND | AJ16 | | |
| N/A | GND | AC16 | | |
| N/A | GND | AB16 | | |
| N/A | GND | AA16 | | |
| N/A | GND | Y16 | | |
| N/A | GND | W16 | | |
| N/A | GND | V16 | | |
| N/A | GND | U16 | | |
| N/A | GND | L16 | | |
| N/A | GND | G16 | | |
| N/A | GND | D16 | | |
| N/A | GND | AU12 | | |
| N/A | GND | AB18 | | |
| N/A | GND | AA18 | | |
| N/A | GND | Y18 | | |

## FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 0 | IO_L01N_0/VRP_0 | | G34 | | |
| 0 | IO_L01P_0/VRN_0 | | H34 | | |
| 0 | IO_L02N_0 | | F34 | | |
| 0 | IO_L02P_0 | | E34 | | |
| 0 | IO_L03N_0 | | C34 | | |
| 0 | IO_L03P_0/VREF_0 | | D34 | | |
| 0 | IO_L05_0/No_Pair | | K32 | | |
| 0 | IO_L06N_0 | | H33 | | |
| 0 | IO_L06P_0 | | J33 | | |
| 0 | IO_L07N_0 | | F33 | | |
| 0 | IO_L07P_0 | | G33 | | |
| 0 | IO_L08N_0 | | E33 | | |
| 0 | IO_L08P_0 | | D33 | | |
| 0 | IO_L09N_0 | | H32 | | |
| 0 | IO_L09P_0/VREF_0 | | J32 | | |
| 0 | IO_L19N_0 | | E32 | | |
| 0 | IO_L19P_0 | | F32 | | |
| 0 | IO_L20N_0 | | C33 | | |
| 0 | IO_L20P_0 | | C32 | | |
| 0 | IO_L21N_0 | | K31 | | |
| 0 | IO_L21P_0 | | L31 | | |
| 0 | IO_L25N_0 | | H31 | | |
| 0 | IO_L25P_0 | | J31 | | |
| 0 | IO_L26N_0 | | G31 | | |
| 0 | IO_L26P_0 | | F31 | | |
| 0 | IO_L27N_0 | | D31 | | |
| 0 | IO_L27P_0/VREF_0 | | E31 | | |
| 0 | IO_L28N_0 | | L30 | | |
| 0 | IO_L28P_0 | | M30 | | |
| 0 | IO_L29N_0 | | J30 | | |
| 0 | IO_L29P_0 | | K30 | | |
| 0 | IO_L30N_0 | | G30 | | |
| 0 | IO_L30P_0 | | H30 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | IO_L77N_3 | | AT3 | | |
| 3 | IO_L77P_3 | | AT4 | | |
| 3 | IO_L76N_3 | | AU1 | | |
| 3 | IO_L76P_3 | | AU2 | | |
| 3 | IO_L75N_3/VREF_3 | | AU3 | | |
| 3 | IO_L75P_3 | | AU4 | | |
| 3 | IO_L74N_3 | | AV3 | | |
| 3 | IO_L74P_3 | | AW3 | | |
| 3 | IO_L73N_3 | | AV1 | | |
| 3 | IO_L73P_3 | | AV2 | | |
| 3 | IO_L06N_3 | | AW1 | | |
| 3 | IO_L06P_3 | | AW2 | | |
| 3 | IO_L05N_3 | | AT8 | | |
| 3 | IO_L05P_3 | | AU8 | | |
| 3 | IO_L04N_3 | | AT6 | | |
| 3 | IO_L04P_3 | | AU7 | | |
| 3 | IO_L03N_3/VREF_3 | | AY5 | | |
| 3 | IO_L03P_3 | | AY6 | | |
| 3 | IO_L02N_3 | | AV7 | | |
| 3 | IO_L02P_3 | | AW7 | | |
| 3 | IO_L01N_3/VRP_3 | | AV6 | | |
| 3 | IO_L01P_3/VRN_3 | | AW6 | | |
| | | | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | | AT9 | | |
| 4 | IO_L01P_4/INIT_B | | AR9 | | |
| 4 | IO_L02N_4/D0/DIN(1) | | AU9 | | |
| 4 | IO_L02P_4/D1 | | AV9 | | |
| 4 | IO_L03N_4/D2 | | AY9 | | |
| 4 | IO_L03P_4/D3 | | AW9 | | |
| 4 | IO_L05_4/No_Pair | | AN11 | | |
| 4 | IO_L06N_4/VRP_4 | | AR10 | | |
| 4 | IO_L06P_4/VRN_4 | | AP10 | | |
| 4 | IO_L07N_4 | | AU10 | | |
| 4 | IO_L07P_4/VREF_4 | | AT10 | | |
| 4 | IO_L08N_4 | | AV10 | | |
| 4 | IO_L08P_4 | | AW10 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 4 | IO_L87P_4/VREF_4 | | AP15 | NC | |
| 4 | IO_L37N_4 | | AV15 | | |
| 4 | IO_L37P_4 | | AU15 | | |
| 4 | IO_L38N_4 | | AY14 | | |
| 4 | IO_L38P_4 | | AY15 | | |
| 4 | IO_L39N_4 | | AM16 | | |
| 4 | IO_L39P_4 | | AL16 | | |
| 4 | IO_L43N_4 | | AP16 | | |
| 4 | IO_L43P_4 | | AN16 | | |
| 4 | IO_L44N_4 | | AR16 | | |
| 4 | IO_L44P_4 | | AT16 | | |
| 4 | IO_L45N_4 | | AV16 | | |
| 4 | IO_L45P_4/VREF_4 | | AU16 | | |
| 4 | IO_L46N_4 | | AL18 | | |
| 4 | IO_L46P_4 | | AL17 | | |
| 4 | IO_L47N_4 | | AM17 | | |
| 4 | IO_L47P_4 | | AN17 | | |
| 4 | IO_L48N_4 | | AR17 | | |
| 4 | IO_L48P_4 | | AP17 | | |
| 4 | IO_L49N_4 | | AU17 | | |
| 4 | IO_L49P_4 | | AT17 | | |
| 4 | IO_L50_4/No_Pair | | AW16 | | |
| 4 | IO_L53_4/No_Pair | | AW17 | | |
| 4 | IO_L54N_4 | | AN18 | | |
| 4 | IO_L54P_4 | | AM18 | | |
| 4 | IO_L55N_4 | | AT18 | | |
| 4 | IO_L55P_4 | | AR18 | | |
| 4 | IO_L56N_4 | | AV17 | | |
| 4 | IO_L56P_4 | | AV18 | | |
| 4 | IO_L57N_4 | | AY18 | | |
| 4 | IO_L57P_4/VREF_4 | | AY17 | | |
| 4 | IO_L58N_4 | | AM19 | | |
| 4 | IO_L58P_4 | | AL19 | | |
| 4 | IO_L59N_4 | | AP19 | | |
| 4 | IO_L59P_4 | | AN19 | | |
| 4 | IO_L60N_4 | | AT19 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 6 | IO_L16N_6 | | AM42 | | |
| 6 | IO_L17P_6 | | AL33 | | |
| 6 | IO_L17N_6 | | AL34 | | |
| 6 | IO_L18P_6 | | AL35 | | |
| 6 | IO_L18N_6 | | AL36 | | |
| 6 | IO_L19P_6 | | AL38 | | |
| 6 | IO_L19N_6 | | AL39 | | |
| 6 | IO_L20P_6 | | AL31 | | |
| 6 | IO_L20N_6 | | AL32 | | |
| 6 | IO_L21P_6 | | AL40 | | |
| 6 | IO_L21N_6/VREF_6 | | AL41 | | |
| 6 | IO_L22P_6 | | AK35 | | |
| 6 | IO_L22N_6 | | AK36 | | |
| 6 | IO_L23P_6 | | AK33 | | |
| 6 | IO_L23N_6 | | AK34 | | |
| 6 | IO_L24P_6 | | AK37 | | |
| 6 | IO_L24N_6 | | AK38 | | |
| 6 | IO_L25P_6 | | AK39 | | |
| 6 | IO_L25N_6 | | AK40 | | |
| 6 | IO_L26P_6 | | AK31 | | |
| 6 | IO_L26N_6 | | AK32 | | |
| 6 | IO_L27P_6 | | AK41 | | |
| 6 | IO_L27N_6/VREF_6 | | AK42 | | |
| 6 | IO_L28P_6 | | AJ35 | | |
| 6 | IO_L28N_6 | | AJ36 | | |
| 6 | IO_L29P_6 | | AJ33 | | |
| 6 | IO_L29N_6 | | AJ34 | | |
| 6 | IO_L30P_6 | | AJ37 | | |
| 6 | IO_L30N_6 | | AJ38 | | |
| 6 | IO_L31P_6 | | AJ41 | | |
| 6 | IO_L31N_6 | | AJ42 | | |
| 6 | IO_L32P_6 | | AJ31 | | |
| 6 | IO_L32N_6 | | AJ32 | | |
| 6 | IO_L33P_6 | | AH33 | | |
| 6 | IO_L33N_6/VREF_6 | | AH34 | | |
| 6 | IO_L34P_6 | | AH37 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | VCCO_3 | | AD14 | | |
| 3 | VCCO_3 | | AC15 | | |
| 3 | VCCO_3 | | AC14 | | |
| 3 | VCCO_3 | | AC8 | | |
| 3 | VCCO_3 | | AC5 | | |
| 3 | VCCO_3 | | AB15 | | |
| 3 | VCCO_3 | | AB14 | | |
| 4 | VCCO_4 | | AW18 | | |
| 4 | VCCO_4 | | AT20 | | |
| 4 | VCCO_4 | | AT15 | | |
| 4 | VCCO_4 | | AT11 | | |
| 4 | VCCO_4 | | AP18 | | |
| 4 | VCCO_4 | | AP14 | | |
| 4 | VCCO_4 | | AJ21 | | |
| 4 | VCCO_4 | | AJ20 | | |
| 4 | VCCO_4 | | AJ19 | | |
| 4 | VCCO_4 | | AJ18 | | |
| 4 | VCCO_4 | | AJ17 | | |
| 4 | VCCO_4 | | AH21 | | |
| 4 | VCCO_4 | | AH20 | | |
| 4 | VCCO_4 | | AH19 | | |
| 4 | VCCO_4 | | AH18 | | |
| 5 | VCCO_5 | | AW25 | | |
| 5 | VCCO_5 | | AT32 | | |
| 5 | VCCO_5 | | AT28 | | |
| 5 | VCCO_5 | | AT23 | | |
| 5 | VCCO_5 | | AP29 | | |
| 5 | VCCO_5 | | AP25 | | |
| 5 | VCCO_5 | | AJ26 | | |
| 5 | VCCO_5 | | AJ25 | | |
| 5 | VCCO_5 | | AJ24 | | |
| 5 | VCCO_5 | | AJ23 | | |
| 5 | VCCO_5 | | AJ22 | | |
| 5 | VCCO_5 | | AH25 | | |
| 5 | VCCO_5 | | AH24 | | |
| 5 | VCCO_5 | | AH23 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 1 | IO_L87N_1/VREF_1 | C15 | |
| 1 | IO_L87P_1 | C16 | |
| 1 | IO_L86N_1 | K15 | |
| 1 | IO_L86P_1 | J15 | |
| 1 | IO_L85N_1 | F15 | |
| 1 | IO_L85P_1 | E15 | |
| 1 | IO_L84N_1 | G15 | |
| 1 | IO_L84P_1 | G16 | |
| 1 | IO_L83_1/No_Pair | M15 | |
| 1 | IO_L80_1/No_Pair | L15 | |
| 1 | IO_L79N_1 | B14 | |
| 1 | IO_L79P_1 | A14 | |
| 1 | IO_L78N_1 | C14 | |
| 1 | IO_L78P_1 | D15 | |
| 1 | IO_L77N_1 | K14 | |
| 1 | IO_L77P_1 | J14 | |
| 1 | IO_L76N_1 | F14 | |
| 1 | IO_L76P_1 | E14 | |
| 1 | IO_L36N_1/VREF_1 | G14 | |
| 1 | IO_L36P_1 | H15 | |
| 1 | IO_L35N_1 | M14 | |
| 1 | IO_L35P_1 | L14 | |
| 1 | IO_L34N_1 | C13 | |
| 1 | IO_L34P_1 | B13 | |
| 1 | IO_L30N_1 | G13 | |
| 1 | IO_L30P_1 | F13 | |
| 1 | IO_L29N_1 | L13 | |
| 1 | IO_L29P_1 | K13 | |
| 1 | IO_L28N_1 | C12 | |
| 1 | IO_L28P_1 | B12 | |
| 1 | IO_L27N_1/VREF_1 | D12 | |
| 1 | IO_L27P_1 | D13 | |
| 1 | IO_L26N_1 | J12 | |
| 1 | IO_L26P_1 | H12 | |
| 1 | IO_L25N_1 | F12 | |
| 1 | IO_L25P_1 | E12 | |
| 1 | IO_L21N_1 | G12 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 2 | IO_L59N_2 | AA11 | |
| 2 | IO_L59P_2 | AA12 | |
| 2 | IO_L60N_2 | W1 | |
| 2 | IO_L60P_2 | W2 | |
| 2 | IO_L85N_2 | Y2 | |
| 2 | IO_L85P_2 | Y3 | |
| 2 | IO_L86N_2 | AA9 | |
| 2 | IO_L86P_2 | AA10 | |
| 2 | IO_L87N_2 | AA5 | |
| 2 | IO_L87P_2 | AA6 | |
| 2 | IO_L88N_2/VREF_2 | AA4 | |
| 2 | IO_L88P_2 | Y4 | |
| 2 | IO_L89N_2 | AA7 | |
| 2 | IO_L89P_2 | AA8 | |
| 2 | IO_L90N_2 | AA2 | |
| 2 | IO_L90P_2 | AA3 | |
| | | | |
| 3 | IO_L90N_3 | AB5 | |
| 3 | IO_L90P_3 | AB6 | |
| 3 | IO_L89N_3 | AB11 | |
| 3 | IO_L89P_3 | AB12 | |
| 3 | IO_L88N_3 | AB2 | |
| 3 | IO_L88P_3 | AB3 | |
| 3 | IO_L87N_3/VREF_3 | AB4 | |
| 3 | IO_L87P_3 | AC4 | |
| 3 | IO_L86N_3 | AB9 | |
| 3 | IO_L86P_3 | AB10 | |
| 3 | IO_L85N_3 | AC2 | |
| 3 | IO_L85P_3 | AC3 | |
| 3 | IO_L60N_3 | AD5 | |
| 3 | IO_L60P_3 | AD6 | |
| 3 | IO_L59N_3 | AB7 | |
| 3 | IO_L59P_3 | AB8 | |
| 3 | IO_L58N_3 | AD1 | |
| 3 | IO_L58P_3 | AD2 | |
| 3 | IO_L57N_3/VREF_3 | AE4 | |
| 3 | IO_L57P_3 | AE5 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 3 | IO_L06N_3 | BA8 | |
| 3 | IO_L06P_3 | BB8 | |
| 3 | IO_L05N_3 | AW8 | |
| 3 | IO_L05P_3 | AW9 | |
| 3 | IO_L04N_3 | BA7 | |
| 3 | IO_L04P_3 | BB7 | |
| 3 | IO_L03N_3/VREF_3 | BA6 | |
| 3 | IO_L03P_3 | BB6 | |
| 3 | IO_L02N_3 | AY9 | |
| 3 | IO_L02P_3 | BA9 | |
| 3 | IO_L01N_3/VRP_3 | BA4 | |
| 3 | IO_L01P_3/VRN_3 | BB4 | |
| | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | AL11 | |
| 4 | IO_L01P_4/INIT_B | AL12 | |
| 4 | IO_L02N_4/D0/DIN(1) | AV10 | |
| 4 | IO_L02P_4/D1 | AU10 | |
| 4 | IO_L03N_4/D2 | AN11 | |
| 4 | IO_L03P_4/D3 | AM11 | |
| 4 | IO_L05_4/No_Pair | AT10 | |
| 4 | IO_L06N_4/VRP_4 | AY11 | |
| 4 | IO_L06P_4/VRN_4 | AY10 | |
| 4 | IO_L07N_4 | BB10 | |
| 4 | IO_L07P_4/VREF_4 | BA10 | |
| 4 | IO_L08N_4 | AU11 | |
| 4 | IO_L08P_4 | AT11 | |
| 4 | IO_L09N_4 | AR11 | |
| 4 | IO_L09P_4/VREF_4 | AP11 | |
| 4 | IO_L19N_4 | AW11 | |
| 4 | IO_L19P_4 | AV11 | |
| 4 | IO_L20N_4 | BB11 | |
| 4 | IO_L20P_4 | BA11 | |
| 4 | IO_L21N_4 | AN12 | |
| 4 | IO_L21P_4 | AM12 | |
| 4 | IO_L25N_4 | AR13 | |
| 4 | IO_L25P_4 | AT12 | |
| 4 | IO_L26N_4 | AV12 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 4 | IO_L58P_4 | AW19 | |
| 4 | IO_L59N_4 | AP19 | |
| 4 | IO_L59P_4 | AN19 | |
| 4 | IO_L60N_4 | BB19 | |
| 4 | IO_L60P_4 | BA19 | |
| 4 | IO_L64N_4 | AU20 | |
| 4 | IO_L64P_4 | AT20 | |
| 4 | IO_L65N_4 | AL21 | |
| 4 | IO_L65P_4 | AL20 | |
| 4 | IO_L66N_4 | BA20 | |
| 4 | IO_L66P_4/VREF_4 | AY20 | |
| 4 | IO_L67N_4 | AR21 | |
| 4 | IO_L67P_4 | AP21 | |
| 4 | IO_L68N_4 | AN20 | |
| 4 | IO_L68P_4 | AM20 | |
| 4 | IO_L69N_4 | AU21 | |
| 4 | IO_L69P_4/VREF_4 | AT21 | |
| 4 | IO_L73N_4 | AW21 | |
| 4 | IO_L73P_4 | AV21 | |
| 4 | IO_L74N_4/GCLK3S | AN21 | |
| 4 | IO_L74P_4/GCLK2P | AM21 | |
| 4 | IO_L75N_4/GCLK1S | BA21 | |
| 4 | IO_L75P_4/GCLK0P | AY21 | |
| | | | |
| 5 | IO_L75N_5/GCLK7S | AY22 | |
| 5 | IO_L75P_5/GCLK6P | BA22 | |
| 5 | IO_L74N_5/GCLK5S | AM22 | |
| 5 | IO_L74P_5/GCLK4P | AN22 | |
| 5 | IO_L73N_5 | AV22 | |
| 5 | IO_L73P_5 | AW22 | |
| 5 | IO_L69N_5/VREF_5 | AT22 | |
| 5 | IO_L69P_5 | AU22 | |
| 5 | IO_L68N_5 | AM23 | |
| 5 | IO_L68P_5 | AN23 | |
| 5 | IO_L67N_5 | AP22 | |
| 5 | IO_L67P_5 | AR22 | |
| 5 | IO_L66N_5/VREF_5 | AY23 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 7 | VCCO_7 | AA29 | |
| 7 | VCCO_7 | Y29 | |
| 7 | VCCO_7 | W29 | |
| 7 | VCCO_7 | V29 | |
| 7 | VCCO_7 | U29 | |
| 7 | VCCO_7 | T29 | |
| 7 | VCCO_7 | R29 | |
| 7 | VCCO_7 | AA28 | |
| 7 | VCCO_7 | Y28 | |
| 7 | VCCO_7 | W28 | |
| 7 | VCCO_7 | V28 | |
| 7 | VCCO_7 | U28 | |
| 7 | VCCO_7 | T28 | |
| 6 | VCCO_6 | AU39 | |
| 6 | VCCO_6 | AN39 | |
| 6 | VCCO_6 | AJ39 | |
| 6 | VCCO_6 | AD39 | |
| 6 | VCCO_6 | AW37 | |
| 6 | VCCO_6 | AN35 | |
| 6 | VCCO_6 | AJ35 | |
| 6 | VCCO_6 | AD35 | |
| 6 | VCCO_6 | AR33 | |
| 6 | VCCO_6 | AL33 | |
| 6 | VCCO_6 | AH29 | |
| 6 | VCCO_6 | AG29 | |
| 6 | VCCO_6 | AF29 | |
| 6 | VCCO_6 | AE29 | |
| 6 | VCCO_6 | AD29 | |
| 6 | VCCO_6 | AC29 | |
| 6 | VCCO_6 | AB29 | |
| 6 | VCCO_6 | AG28 | |
| 6 | VCCO_6 | AF28 | |
| 6 | VCCO_6 | AE28 | |
| 6 | VCCO_6 | AD28 | |
| 6 | VCCO_6 | AC28 | |
| 6 | VCCO_6 | AB28 | |
| 5 | VCCO_5 | AW33 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 2 | VCCO_2 | F4 | |
| 1 | VCCO_1 | R21 | |
| 1 | VCCO_1 | P21 | |
| 1 | VCCO_1 | R20 | |
| 1 | VCCO_1 | P20 | |
| 1 | VCCO_1 | R19 | |
| 1 | VCCO_1 | P19 | |
| 1 | VCCO_1 | R18 | |
| 1 | VCCO_1 | P18 | |
| 1 | VCCO_1 | H18 | |
| 1 | VCCO_1 | D18 | |
| 1 | VCCO_1 | P17 | |
| 1 | VCCO_1 | H14 | |
| 1 | VCCO_1 | D14 | |
| 1 | VCCO_1 | M13 | |
| 1 | VCCO_1 | D10 | |
| 0 | VCCO_0 | D33 | |
| 0 | VCCO_0 | M30 | |
| 0 | VCCO_0 | H29 | |
| 0 | VCCO_0 | D29 | |
| 0 | VCCO_0 | P26 | |
| 0 | VCCO_0 | R25 | |
| 0 | VCCO_0 | P25 | |
| 0 | VCCO_0 | H25 | |
| 0 | VCCO_0 | D25 | |
| 0 | VCCO_0 | R24 | |
| 0 | VCCO_0 | P24 | |
| 0 | VCCO_0 | R23 | |
| 0 | VCCO_0 | P23 | |
| 0 | VCCO_0 | R22 | |
| 0 | VCCO_0 | P22 | |
| | | | |
| N/A | CCLK | AM10 | |
| N/A | PROG_B | J33 | |
| N/A | DONE | AN10 | |
| N/A | M0 | AP33 | |
| N/A | M1 | AN33 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| N/A | GND | BB34 | |
| N/A | GND | AV34 | |
| N/A | GND | AP34 | |
| N/A | GND | AK34 | |
| N/A | GND | AF34 | |
| N/A | GND | AC34 | |
| N/A | GND | Y34 | |
| N/A | GND | U34 | |
| N/A | GND | N34 | |
| N/A | GND | J34 | |
| N/A | GND | E34 | |
| N/A | GND | A34 | |
| N/A | GND | AD31 | |
| N/A | GND | W31 | |
| N/A | GND | BB30 | |
| N/A | GND | AV30 | |
| N/A | GND | AP30 | |
| N/A | GND | J30 | |
| N/A | GND | E30 | |
| N/A | GND | A30 | |
| N/A | GND | BB26 | |
| N/A | GND | AV26 | |
| N/A | GND | AP26 | |
| N/A | GND | AE26 | |
| N/A | GND | AD26 | |
| N/A | GND | AC26 | |
| N/A | GND | AB26 | |
| N/A | GND | AA26 | |
| N/A | GND | Y26 | |
| N/A | GND | W26 | |
| N/A | GND | V26 | |
| N/A | GND | J26 | |
| N/A | GND | E26 | |
| N/A | GND | A26 | |
| N/A | GND | AF25 | |
| N/A | GND | AE25 | |
| N/A | GND | AD25 | |