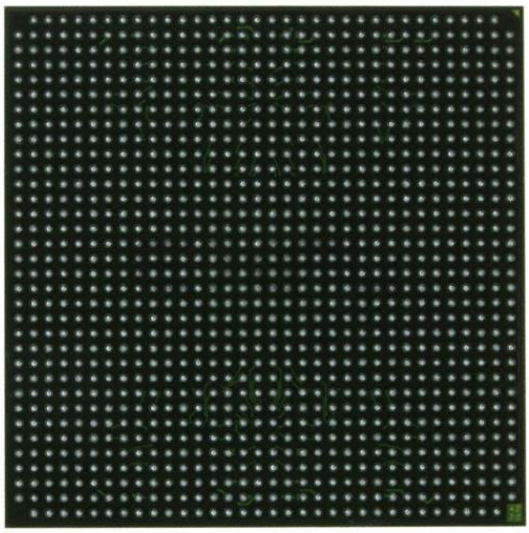
AMD Xilinx - XC2VP50-5FFG1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-5ffg1152i

- Execution unit
- Timers
- Debug logic unit

It operates on instructions in a five stage pipeline consisting of a fetch, decode, execute, write-back, and load write-back stage. Most instructions execute in a single cycle, including loads and stores.

Instruction and Data Cache

The embedded PPC405 core provides an instruction cache unit (ICU) and a data cache unit (DCU) that allow concurrent accesses and minimize pipeline stalls. The instruction and data cache array are 16 KB each. Both cache units are two-way set associative. Each way is organized into 256 lines of 32 bytes (eight words). The instruction set provides a rich assortment of cache control instructions, including instructions to read tag information and data arrays.

The PPC405 core accesses external memory through the instruction (ICU) and data cache units (DCU). The cache units each include a 64-bit PLB master interface, cache arrays, and a cache controller. The ICU and DCU handle cache misses as requests over the PLB to another PLB device such as an external bus interface unit. Cache hits are handled as single cycle memory accesses to the instruction and data caches.

Instruction Cache Unit (ICU)

The ICU provides one or two instructions per cycle to the instruction queue over a 64-bit bus. A line buffer (built into the output of the array for manufacturing test) enables the ICU to be accessed only once for every four instructions, to reduce power consumption by the array.

The ICU can forward any or all of the four or eight words of a line fill to the EXU to minimize pipeline stalls caused by cache misses. The ICU aborts speculative fetches abandoned by the EXU, eliminating unnecessary line fills and enabling the ICU to handle the next EXU fetch. Aborting abandoned requests also eliminates unnecessary external bus activity, thereby increasing external bus utilization.

Data Cache Unit (DCU)

The DCU transfers one, two, three, four, or eight bytes per cycle, depending on the number of byte enables presented by the CPU. The DCU contains a single-element command and store data queue to reduce pipeline stalls; this queue enables the DCU to independently process load/store and cache control instructions. Dynamic PLB request prioritization reduces pipeline stalls even further. When the DCU is busy with a low-priority request while a subsequent storage operation requested by the CPU is stalled; the DCU automatically increases the priority of the current request to the PLB.

The DCU provides additional features that allow the programmer to tailor its performance for a given application. The DCU can function in write-back or write-through mode, as controlled by the Data Cache Write-through Register (DCWR) or the Translation Look-aside Buffer (TLB); the cache controller can be tuned for a balance of performance and memory coherency. Write-on-allocate, controlled by the store word on allocate (SWOA) field of the Core Configuration Register 0 (CCR0), can inhibit line fills caused by store misses, to further reduce potential pipeline stalls and unwanted external bus traffic.

Fetch and Decode Logic

The fetch/decode logic maintains a steady flow of instructions to the execution unit by placing up to two instructions in the fetch queue. The fetch queue consists of three buffers: pre-fetch buffer 1 (PFB1), pre-fetch buffer 0 (PFB0), and decode (DCD). The fetch logic ensures that instructions proceed directly to decode when the queue is empty.

Static branch prediction as implemented on the PPC405 core takes advantage of some standard statistical properties of code. Branches with negative address displacement are by default assumed taken. Branches that do not test the condition or count registers are also predicted as taken. The PPC405 core bases branch prediction upon these default conditions when a branch is not resolved and speculatively fetches along the predicted path. The default prediction can be overridden by software at assembly or compile time.

Branches are examined in the decode and pre-fetch buffer 0 fetch queue stages. Two branch instructions can be handled simultaneously. If the branch in decode is not taken, the fetch logic fetches along the predicted path of the branch instruction in pre-fetch buffer 0. If the branch in decode is taken, the fetch logic ignores the branch instruction in pre-fetch buffer 0.

Execution Unit

The embedded PPC405 core has a single issue execution unit (EXU) containing the register file, arithmetic logic unit (ALU), and the multiply-accumulate (MAC) unit. The execution unit performs all 32-bit PowerPC integer instructions in hardware.

The register file is comprised of thirty-two 32-bit general purpose registers (GPR), which are accessed with three read ports and two write ports. During the decode stage, data is read out of the GPRs and fed to the execution unit. Likewise, during the write-back stage, results are written to the GPR. The use of the five ports on the register file enables either a load or a store operation to execute in parallel with an ALU operation.

Memory Management Unit (MMU)

The embedded PPC405 core has a 4 GB address space, which is presented as a flat address space.

The MMU provides address translation, protection functions, and storage attribute control for embedded applications. The MMU supports demand-paged virtual memory and other management schemes that require precise control of logical-to-physical address mapping and flexible

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
3	IO_L05P_3	L13
3	IO_L03N_3/VREF_3	L12
3	IO_L03P_3	M13
3	IO_L02N_3	M16
3	IO_L02P_3	N16
3	IO_L01N_3/VRP_3	M15
3	IO_L01P_3/VRN_3	M14
4	IO_L01N_4/BUSY/DOUT(1)	P15
4	IO_L01P_4/INIT_B	P14
4	IO_L02N_4/D0/DIN(1)	R14
4	IO_L02P_4/D1	P13
4	IO_L03N_4/D2	T15
4	IO_L03P_4/D3	T14
4	IO_L06N_4/VRP_4	N12
4	IO_L06P_4/VRN_4	P12
4	IO_L07P_4/VREF_4	N11
4	IO_L09N_4	M11
4	IO_L09P_4/VREF_4	M10
4	IO_L69N_4	N10
4	IO_L69P_4/VREF_4	P10
4	IO_L74N_4/GCLK3S	N9
4	IO_L74P_4/GCLK2P	P9
4	IO_L75N_4/GCLK1S	R9
4	IO_L75P_4/GCLK0P	T9
5	IO_L75N_5/GCLK7S	T8
5	IO_L75P_5/GCLK6P	R8
5	IO_L74N_5/GCLK5S	P8
5	IO_L74P_5/GCLK4P	N8
5	IO_L69N_5/VREF_5	P7
5	IO_L69P_5	N7
5	IO_L09N_5/VREF_5	M7
5	IO_L09P_5	M6
5	IO_L07N_5/VREF_5	N6

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VTTXPAD4	B4			
N/A	TXNPAD4	A4			
N/A	TXPPAD4	A5			
N/A	GNDA4	C6			
N/A	RXPPAD4	A6			
N/A	RXNPAD4	A7			
N/A	VTRXPAD4	B6			
N/A	AVCCAUXRX4	B7			
N/A	AVCCAUXTX6	B10			
N/A	VTTXPAD6	B9			
N/A	TXNPAD6	A9			
N/A	TXPPAD6	A10			
N/A	GNDA6	C11			
N/A	RXPPAD6	A11			
N/A	RXNPAD6	A12			
N/A	VTRXPAD6	B11			
N/A	AVCCAUXRX6	B12			
N/A	AVCCAUXTX7	B16			
N/A	VTTXPAD7	B15			
N/A	TXNPAD7	A15			
N/A	TXPPAD7	A16			
N/A	GNDA7	C16			
N/A	RXPPAD7	A17			
N/A	RXNPAD7	A18			
N/A	VTRXPAD7	B17			
N/A	AVCCAUXRX7	B18			
N/A	AVCCAUXTX9	B21			
N/A	VTTXPAD9	B20			
N/A	TXNPAD9	A20			
N/A	TXPPAD9	A21			
N/A	GNDA9	C21			
N/A	RXPPAD9	A22			
N/A	RXNPAD9	A23			
N/A	VTRXPAD9	B22			
N/A	AVCCAUXRX9	B23			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L02P_6		AH26			
6	IO_L02N_6		AG26			
6	IO_L03P_6		AH29			
6	IO_L03N_6/VREF_6		AH30			
6	IO_L04P_6		AH27			
6	IO_L04N_6		AG28			
6	IO_L05P_6		AD25			
6	IO_L05N_6		AD26			
6	IO_L06P_6		AG29			
6	IO_L06N_6		AG30			
6	IO_L31P_6		AF25	NC		
6	IO_L31N_6		AE26	NC		
6	IO_L32P_6		AB23	NC		
6	IO_L32N_6		AB24	NC		
6	IO_L33P_6		AE27	NC		
6	IO_L33N_6/VREF_6		AE28	NC		
6	IO_L34P_6		AF27	NC		
6	IO_L34N_6		AF28	NC		
6	IO_L35P_6		AC25	NC		
6	IO_L35N_6		AC26	NC		
6	IO_L36P_6		AF29	NC		
6	IO_L36N_6		AF30	NC		
6	IO_L37P_6		AD27	NC		
6	IO_L37N_6		AD28	NC		
6	IO_L38P_6		AA23	NC		
6	IO_L38N_6		AA24	NC		
6	IO_L39P_6		AE29	NC		
6	IO_L39N_6/VREF_6		AE30	NC		
6	IO_L40P_6		AB25	NC		
6	IO_L40N_6		AB26	NC		
6	IO_L41P_6		Y23	NC		
6	IO_L41N_6		Y24	NC		
6	IO_L42P_6		AD29	NC		
6	IO_L42N_6		AD30	NC		
6	IO_L43P_6		AC27			
6	IO_L43N_6		AC28			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L44P_6		AA25			
6	IO_L44N_6		AA26			
6	IO_L45P_6		AC29			
6	IO_L45N_6/VREF_6		AB29			
6	IO_L46P_6		AB27			
6	IO_L46N_6		AB28			
6	IO_L47P_6		W23			
6	IO_L47N_6		W24			
6	IO_L48P_6		AA27			
6	IO_L48N_6		AA28			
6	IO_L49P_6		Y26			
6	IO_L49N_6		Y27			
6	IO_L50P_6		W25			
6	IO_L50N_6		W26			
6	IO_L51P_6		AB30			
6	IO_L51N_6/VREF_6		AA30			
6	IO_L52P_6		W27			
6	IO_L52N_6		W28			
6	IO_L53P_6		V23			
6	IO_L53N_6		V24			
6	IO_L54P_6		AA29			
6	IO_L54N_6		Y29			
6	IO_L55P_6		V25			
6	IO_L55N_6		V26			
6	IO_L56P_6		U23			
6	IO_L56N_6		U24			
6	IO_L57P_6		Y30			
6	IO_L57N_6/VREF_6		W30			
6	IO_L58P_6		V27			
6	IO_L58N_6		V28			
6	IO_L59P_6		U22			
6	IO_L59N_6		T22			
6	IO_L60P_6		W29			
6	IO_L60N_6		V29			
6	IO_L85P_6		U26			
6	IO_L85N_6		U27			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L54N_7		L26			
7	IO_L53P_7		N26			
7	IO_L53N_7		N25			
7	IO_L52P_7		M30			
7	IO_L52N_7/VREF_7		L30			
7	IO_L51P_7		K28			
7	IO_L51N_7		K27			
7	IO_L50P_7		N24			
7	IO_L50N_7		N23			
7	IO_L49P_7		L29			
7	IO_L49N_7		K29			
7	IO_L48P_7		J28			
7	IO_L48N_7		J27			
7	IO_L47P_7		M26			
7	IO_L47N_7		M25			
7	IO_L46P_7		K30			
7	IO_L46N_7/VREF_7		J30			
7	IO_L45P_7		K26			
7	IO_L45N_7		K25			
7	IO_L44P_7		M24			
7	IO_L44N_7		M23			
7	IO_L43P_7		J29			
7	IO_L43N_7		H29			
7	IO_L42P_7		H28	NC		
7	IO_L42N_7		H27	NC		
7	IO_L41P_7		L24	NC		
7	IO_L41N_7		L23	NC		
7	IO_L40P_7		G30	NC		
7	IO_L40N_7/VREF_7		G29	NC		
7	IO_L39P_7		G28	NC		
7	IO_L39N_7		G27	NC		
7	IO_L38P_7		J26	NC		
7	IO_L38N_7		J25	NC		
7	IO_L37P_7		F30	NC		
7	IO_L37N_7		F29	NC		
7	IO_L36P_7		F28	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L43P_0	E22				
0	IO_L44N_0	E25				
0	IO_L44P_0	D25				
0	IO_L45N_0	H21				
0	IO_L45P_0/VREF_0	G21				
0	IO_L46N_0	D22				
0	IO_L46P_0	D23				
0	IO_L47N_0	D24				
0	IO_L47P_0	C24				
0	IO_L48N_0	K20				
0	IO_L48P_0	J20				
0	IO_L49N_0	F21				
0	IO_L49P_0	E21				
0	IO_L50_0/No_Pair	C21				
0	IO_L53_0/No_Pair	C22				
0	IO_L54N_0	L19				
0	IO_L54P_0	K19				
0	IO_L55N_0	G20				
0	IO_L55P_0	F20				
0	IO_L56N_0	D21				
0	IO_L56P_0	D20				
0	IO_L57N_0	J19				
0	IO_L57P_0/VREF_0	H19				
0	IO_L67N_0	G19				
0	IO_L67P_0	F19				
0	IO_L68N_0	E19				
0	IO_L68P_0	D19				
0	IO_L69N_0	L18				
0	IO_L69P_0/VREF_0	K18				
0	IO_L73N_0	G18				
0	IO_L73P_0	F18				
0	IO_L74N_0/GCLK7P	E18				
0	IO_L74P_0/GCLK6S	D18				
0	IO_L75N_0/GCLK5P	J18				
0	IO_L75P_0/GCLK4S	H18				
1	IO_L75N_1/GCLK3P	H17				
1	IO_L75P_1/GCLK2S	J17				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L18N_7	L25	NC			
7	IO_L17P_7	F34	NC			
7	IO_L17N_7	F33	NC			
7	IO_L16P_7	G30	NC			
7	IO_L16N_7/VREF_7	G29	NC			
7	IO_L15P_7	G32	NC			
7	IO_L15N_7	G31	NC			
7	IO_L06P_7	F31				
7	IO_L06N_7	F30				
7	IO_L05P_7	J28				
7	IO_L05N_7	J27				
7	IO_L04P_7	E34				
7	IO_L04N_7/VREF_7	E33				
7	IO_L03P_7	E32				
7	IO_L03N_7	E31				
7	IO_L02P_7	F28				
7	IO_L02N_7	F27				
7	IO_L01P_7/VRN_7	D34				
7	IO_L01N_7/VRP_7	D33				
0	VCCO_0	C29				
0	VCCO_0	E20				
0	VCCO_0	F25				
0	VCCO_0	L20				
0	VCCO_0	L21				
0	VCCO_0	L22				
0	VCCO_0	L23				
0	VCCO_0	M18				
0	VCCO_0	M19				
0	VCCO_0	M20				
0	VCCO_0	M21				
0	VCCO_0	M22				
1	VCCO_1	C6				
1	VCCO_1	E15				
1	VCCO_1	F10				
1	VCCO_1	L12				
1	VCCO_1	L13				
1	VCCO_1	L14				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	Y34		
N/A	GND	AU32		
N/A	GND	AN32		
N/A	GND	G32		
N/A	GND	C32		
N/A	GND	AH31		
N/A	GND	AD31		
N/A	GND	T31		
N/A	GND	M31		
N/A	GND	Y30		
N/A	GND	AU28		
N/A	GND	AN28		
N/A	GND	G28		
N/A	GND	C28		
N/A	GND	AT24		
N/A	GND	AN24		
N/A	GND	AJ24		
N/A	GND	AC24		
N/A	GND	AB24		
N/A	GND	AA24		
N/A	GND	Y24		
N/A	GND	W24		
N/A	GND	V24		
N/A	GND	U24		
N/A	GND	L24		
N/A	GND	G24		
N/A	GND	D24		
N/A	GND	AD23		
N/A	GND	AC23		
N/A	GND	AB23		
N/A	GND	AA23		
N/A	GND	Y23		
N/A	GND	W23		
N/A	GND	V23		
N/A	GND	U23		
N/A	GND	T23		
N/A	GND	AD22		
N/A	GND	AU39		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AA5		
N/A	GND		Y41		
N/A	GND		Y26		
N/A	GND		Y25		
N/A	GND		Y24		
N/A	GND		Y23		
N/A	GND		Y22		
N/A	GND		Y21		
N/A	GND		Y20		
N/A	GND		Y19		
N/A	GND		Y18		
N/A	GND		Y17		
N/A	GND		Y2		
N/A	GND		W26		
N/A	GND		W25		
N/A	GND		W24		
N/A	GND		W23		
N/A	GND		W22		
N/A	GND		W21		
N/A	GND		W20		
N/A	GND		W19		
N/A	GND		W18		
N/A	GND		W17		
N/A	GND		V37		
N/A	GND		V34		
N/A	GND		V26		
N/A	GND		V25		
N/A	GND		V24		
N/A	GND		V23		
N/A	GND		V22		
N/A	GND		V21		
N/A	GND		V20		
N/A	GND		V19		
N/A	GND		V18		
N/A	GND		V17		
N/A	GND		V9		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L52P_6	AF40	
6	IO_L52N_6	AF41	
6	IO_L53P_6	AC36	
6	IO_L53N_6	AC37	
6	IO_L54P_6	AE41	
6	IO_L54N_6	AE42	
6	IO_L55P_6	AE40	
6	IO_L55N_6	AD40	
6	IO_L56P_6	AC31	
6	IO_L56N_6	AC32	
6	IO_L57P_6	AE38	
6	IO_L57N_6/VREF_6	AE39	
6	IO_L58P_6	AD41	
6	IO_L58N_6	AD42	
6	IO_L59P_6	AB35	
6	IO_L59N_6	AB36	
6	IO_L60P_6	AD37	
6	IO_L60N_6	AD38	
6	IO_L85P_6	AC40	
6	IO_L85N_6	AC41	
6	IO_L86P_6	AB33	
6	IO_L86N_6	AB34	
6	IO_L87P_6	AC39	
6	IO_L87N_6/VREF_6	AB39	
6	IO_L88P_6	AB40	
6	IO_L88N_6	AB41	
6	IO_L89P_6	AB31	
6	IO_L89N_6	AB32	
6	IO_L90P_6	AB37	
6	IO_L90N_6	AB38	
7	IO_L90P_7	AA40	
7	IO_L90N_7	AA41	
7	IO_L89P_7	AA35	
7	IO_L89N_7	AA36	
7	IO_L88P_7	Y39	
7	IO_L88N_7/VREF_7	AA39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	VCCO_7	AA29	
7	VCCO_7	Y29	
7	VCCO_7	W29	
7	VCCO_7	V29	
7	VCCO_7	U29	
7	VCCO_7	T29	
7	VCCO_7	R29	
7	VCCO_7	AA28	
7	VCCO_7	Y28	
7	VCCO_7	W28	
7	VCCO_7	V28	
7	VCCO_7	U28	
7	VCCO_7	T28	
6	VCCO_6	AU39	
6	VCCO_6	AN39	
6	VCCO_6	AJ39	
6	VCCO_6	AD39	
6	VCCO_6	AW37	
6	VCCO_6	AN35	
6	VCCO_6	AJ35	
6	VCCO_6	AD35	
6	VCCO_6	AR33	
6	VCCO_6	AL33	
6	VCCO_6	AH29	
6	VCCO_6	AG29	
6	VCCO_6	AF29	
6	VCCO_6	AE29	
6	VCCO_6	AD29	
6	VCCO_6	AC29	
6	VCCO_6	AB29	
6	VCCO_6	AG28	
6	VCCO_6	AF28	
6	VCCO_6	AE28	
6	VCCO_6	AD28	
6	VCCO_6	AC28	
6	VCCO_6	AB28	
5	VCCO_5	AW33	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	VCCO_2	F4	
1	VCCO_1	R21	
1	VCCO_1	P21	
1	VCCO_1	R20	
1	VCCO_1	P20	
1	VCCO_1	R19	
1	VCCO_1	P19	
1	VCCO_1	R18	
1	VCCO_1	P18	
1	VCCO_1	H18	
1	VCCO_1	D18	
1	VCCO_1	P17	
1	VCCO_1	H14	
1	VCCO_1	D14	
1	VCCO_1	M13	
1	VCCO_1	D10	
0	VCCO_0	D33	
0	VCCO_0	M30	
0	VCCO_0	H29	
0	VCCO_0	D29	
0	VCCO_0	P26	
0	VCCO_0	R25	
0	VCCO_0	P25	
0	VCCO_0	H25	
0	VCCO_0	D25	
0	VCCO_0	R24	
0	VCCO_0	P24	
0	VCCO_0	R23	
0	VCCO_0	P23	
0	VCCO_0	R22	
0	VCCO_0	P22	
N/A	CCLK	AM10	
N/A	PROG_B	J33	
N/A	DONE	AN10	
N/A	M0	AP33	
N/A	M1	AN33	