AMD Xilinx - XC2VP50-5FFG1517C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	852
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-5ffg1517c

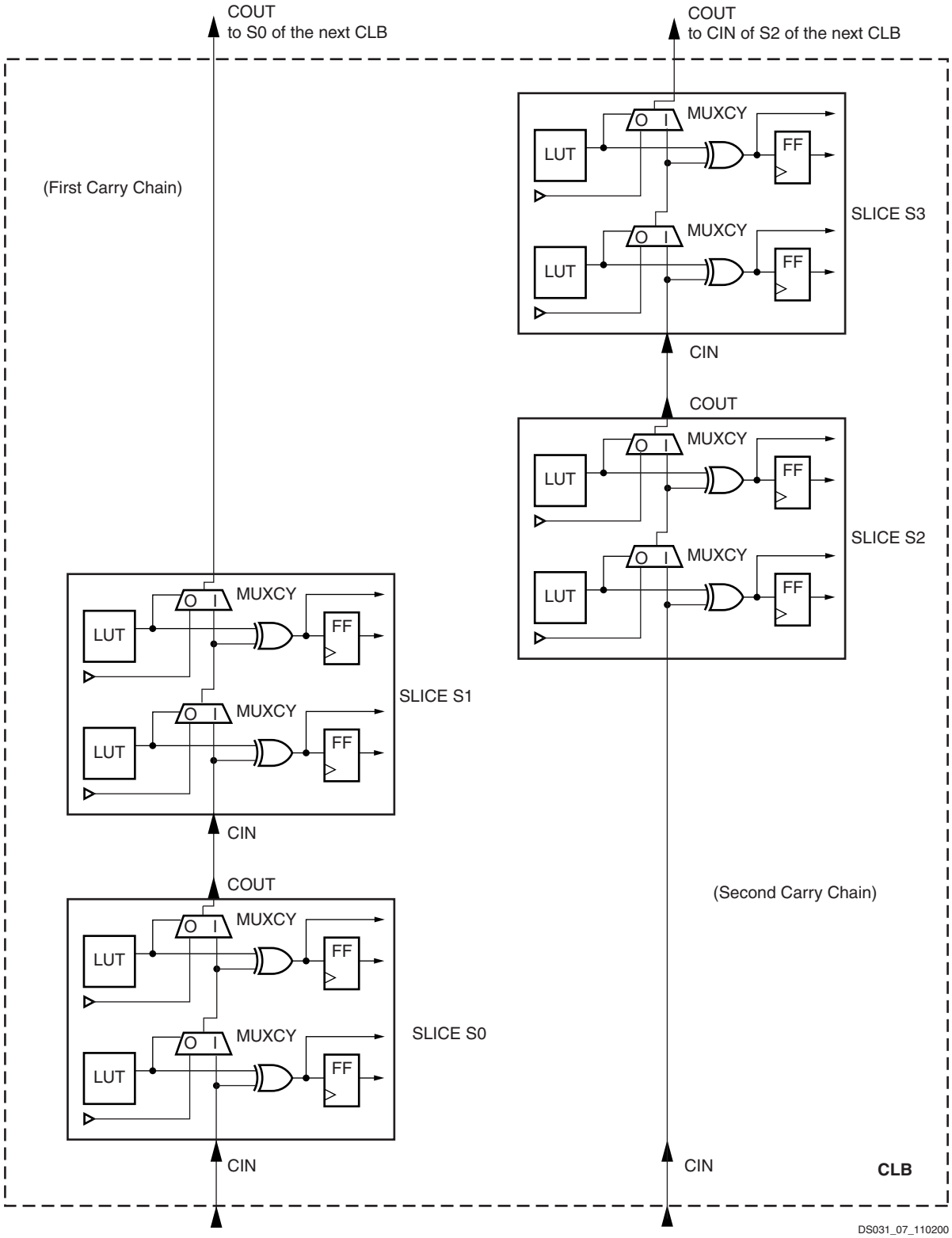

Figure 42: **Fast Carry Logic Path**

Table 2: **Recommended Operating Conditions**

Symbol	Description	Grade	Virtex-II Pro X		Virtex-II Pro		Units
			Min	Max	Min	Max	
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.425	1.575	1.425	1.575	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.425	1.575	1.425	1.575	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	2.375	2.625	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	2.375	2.625	2.375	2.625	V
V_{CCO}(2,3)	Supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.2	3.45(5)	1.2	3.45(5)	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.2	3.45(5)	1.2	3.45(5)	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	GND – 0.2	3.45(5)	GND – 0.2	3.45(5)	V
	3.3V supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	GND – 0.2	3.45(5)	GND – 0.2	3.45(5)	V
	2.5V and below supply voltage relative to GND, T_J = 0 °C to +85°C	Comm.	GND – 0.2	V_{CCO} + 0.2	GND – 0.2	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40°C to +100°C	Indus.	GND – 0.2	V_{CCO} + 0.2	GND – 0.2	V_{CCO} + 0.2	V
V_{BATT}(4)	Battery voltage relative to GND, T_J = 0 °C to +85°C	Comm.	1.0	3.6	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Indus.	1.0	3.6	1.0	3.6	V
AVCCAUXRX(6)	Auxilliary receive supply voltage relative to GNDA	Comm.	1.425(7)	1.575(7)	2.375	2.625	V
		Indus.	1.425(7)	1.575(7)	2.375	2.625	V
AVCCAUXTX(6)	Auxilliary transmit supply voltage relative to GNDA	Comm.	2.375	2.625	2.375	2.625	V
		Indus.	2.375	2.625	2.375	2.625	V
V_{TRX}	Terminal receive supply voltage relative to GND	Comm.	0	2.625	1.6	2.625	V
		Indus.	0	2.625	1.6	2.625	V
V_{TTX}	Terminal transmit supply voltage relative to GND	Comm.	1.425	1.575	1.6	2.625	V
		Indus.	1.425	1.575	1.6	2.625	V

Notes:
1. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. For 3.3V I/O operation, refer to **XAPP659**, available on the Xilinx website at **www.xilinx.com**.
4. If battery is not used, connect V_{BATT} to GND or V_{CCAUX}.
5. For PCI and PCI-X, refer to **XAPP653**, available on the Xilinx website at **www.xilinx.com**.
6. **IMPORTANT!** The RocketIO transceivers have certain power guidelines that must be met, even if unused in the design. Please refer to the section entitled “Powering the RocketIO Transceivers” in the ***RocketIO Transceiver User Guide*** or ***RocketIO X Transceiver User Guide*** for more details.
7. For non-8B/10B-encoded data, the specification for AVCCAUXRX is 1.8V ±5% (1.71 – 1.89V).

LVDS DC Specifications (LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.602	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.898			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	454	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100	350	600	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100		1000	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	V_{CCO} = 2.375V		V_{CCO} = 2.5V		V_{CCO} = 2.625V		Units
	Min	Max	Min	Max	Min	Max	
V_{OH}	1.35	1.495	1.475	1.62	1.6	1.745	V
V_{OL}	0.565	0.755	0.69	0.88	0.815	1.005	V
V_{IH}	0.8	2.0	0.8	2.0	0.8	2.0	V
V_{IL}	0.5	1.7	0.5	1.7	0.5	1.7	V
Differential Input Voltage	0.100	1.5	0.100	1.5	0.100	1.5	V

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Pro Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 38) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

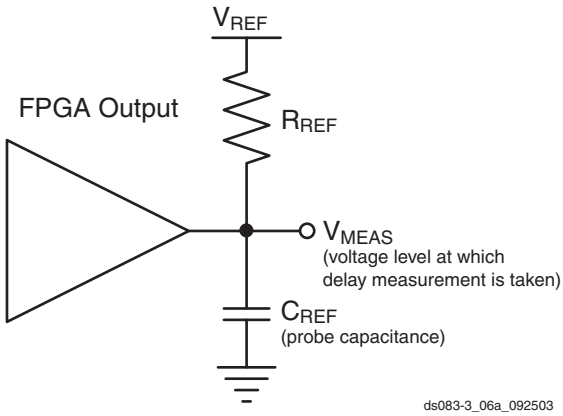

Figure 6: **Generalized Test Setup**

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.65	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	0
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–7		–6		–5		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 65: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2VP2FF672	104	ps
		XC2VP4FF672	102	ps
		XC2VP7FF672	92	ps
		XC2VP7FF896	101	ps
		XC2VP20FF896	93	ps
		XC2VPX20FF896	93	ps
		XC2VP20FF1152	106	ps
		XC2VP30FF896	86	ps
		XC2VP30FF1152	112	ps
		XC2VP40FF1152	92	ps
		XC2VP40FF1148	100	ps
		XC2VP50FF1152	88	ps
		XC2VP50FF1148	101	ps
		XC2VP50FF1517	97	ps
		XC2VP70FF1517	95	ps
		XC2VP70FF1704	101	ps
		XC2VPX70FF1704	101	ps
		XC2VP100FF1704	86	ps
		XC2VP100FF1696	100	ps

Notes:
1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Sampling Error at Receiver Pins(1)	T_{SAMP}	All	0.50	0.50	0.50	ns

Notes:
1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion, T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination *(Continued)***

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP70	Available User I/Os	-	-		-	-	-	-	964	996	-
	RocketIO MGT Pins	-	-		-	-	-	-	144	180	-
	Differential I/O Pairs	-	-		-	-	-	-	476	492	-
XC2VPX70	**Available User I/Os**	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**992**	**-**
	RocketIO X MGT Pins	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**180**	**-**
	Differential I/O Pairs	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**490**	**-**
XC2VP100	Available User I/Os	-	-		-	-	-	-	-	1040	1164
	RocketIO MGT Pins	-	-		-	-	-	-	-	180	0
	Differential I/O Pairs	-	-		-	-	-	-	-	512	572

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1)

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCAUX	L1			
N/A	VCCAUX	B21			
N/A	VCCAUX	B2			
N/A	VCCAUX	AB11			
N/A	VCCAUX	AA21			
N/A	VCCAUX	AA2			
N/A	VCCAUX	A12			
N/A	GND	Y3			
N/A	GND	Y20			
N/A	GND	W4			
N/A	GND	W19			
N/A	GND	V5			
N/A	GND	V18			
N/A	GND	P9			
N/A	GND	P14			
N/A	GND	P13			
N/A	GND	P12			
N/A	GND	P11			
N/A	GND	P10			
N/A	GND	N9			
N/A	GND	N14			
N/A	GND	N13			
N/A	GND	N12			
N/A	GND	N11			
N/A	GND	N10			
N/A	GND	M9			
N/A	GND	M14			
N/A	GND	M13			
N/A	GND	M12			
N/A	GND	M11			
N/A	GND	M10			
N/A	GND	M1			
N/A	GND	L9			
N/A	GND	L22			
N/A	GND	L14			
N/A	GND	L13			
N/A	GND	L12			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	H4			
N/A	GND	H23			
N/A	GND	K6			
N/A	GND	K21			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M3			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M24			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	R3			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L01N_0/VRP_0		E25			
0	IO_L01P_0/VRN_0		E24			
0	IO_L02N_0		F24			
0	IO_L02P_0		F23			
0	IO_L03N_0		E23			
0	IO_L03P_0/VREF_0		E22			
0	IO_L05_0/No_Pair		G23			
0	IO_L06N_0		H22			
0	IO_L06P_0		G22			
0	IO_L07N_0		F22			
0	IO_L07P_0		F21			
0	IO_L08N_0		D24			
0	IO_L08P_0		C24			
0	IO_L09N_0		H21			
0	IO_L09P_0/VREF_0		G21			
0	IO_L37N_0		E21			
0	IO_L37P_0		D21			
0	IO_L38N_0		D23			
0	IO_L38P_0		C23			
0	IO_L39N_0		H20			
0	IO_L39P_0		G20			
0	IO_L43N_0		E20			
0	IO_L43P_0		D20			
0	IO_L44N_0		B23			
0	IO_L44P_0		A23			
0	IO_L45N_0		H19			
0	IO_L45P_0/VREF_0		G19			
0	IO_L46N_0		E19	NC		
0	IO_L46P_0		E18	NC		
0	IO_L47N_0		C22	NC		
0	IO_L47P_0		B22	NC		
0	IO_L48N_0		F20	NC		
0	IO_L48P_0		F19	NC		
0	IO_L49N_0		G17	NC		
0	IO_L49P_0		F17	NC		
0	IO_L50_0/No_Pair		B21	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L41N_2		L8	NC		
2	IO_L41P_2		L7	NC		
2	IO_L42N_2		H4	NC		
2	IO_L42P_2		H3	NC		
2	IO_L43N_2		H2			
2	IO_L43P_2		J2			
2	IO_L44N_2		M8			
2	IO_L44P_2		M7			
2	IO_L45N_2		K6			
2	IO_L45P_2		K5			
2	IO_L46N_2/VREF_2		J1			
2	IO_L46P_2		K1			
2	IO_L47N_2		M6			
2	IO_L47P_2		M5			
2	IO_L48N_2		J4			
2	IO_L48P_2		J3			
2	IO_L49N_2		K2			
2	IO_L49P_2		L2			
2	IO_L50N_2		N8			
2	IO_L50P_2		N7			
2	IO_L51N_2		K4			
2	IO_L51P_2		K3			
2	IO_L52N_2/VREF_2		L1			
2	IO_L52P_2		M1			
2	IO_L53N_2		N6			
2	IO_L53P_2		N5			
2	IO_L54N_2		L5			
2	IO_L54P_2		L4			
2	IO_L55N_2		M2			
2	IO_L55P_2		N2			
2	IO_L56N_2		P9			
2	IO_L56P_2		R9			
2	IO_L57N_2		M4			
2	IO_L57P_2		M3			
2	IO_L58N_2/VREF_2		N1			
2	IO_L58P_2		P1			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L06P_3	AL2				
3	IO_L05N_3	AG7				
3	IO_L05P_3	AH8				
3	IO_L04N_3	AH5				
3	IO_L04P_3	AH6				
3	IO_L03N_3/VREF_3	AK3				
3	IO_L03P_3	AK4				
3	IO_L02N_3	AJ7				
3	IO_L02P_3	AJ8				
3	IO_L01N_3/VRP_3	AJ4				
3	IO_L01P_3/VRN_3	AJ5				
4	IO_L01N_4/BUSY/DOUT(1)	AL5				
4	IO_L01P_4/INIT_B	AL6				
4	IO_L02N_4/D0/DIN(1)	AG9				
4	IO_L02P_4/D1	AH9				
4	IO_L03N_4/D2	AK6				
4	IO_L03P_4/D3	AK7				
4	IO_L05_4/No_Pair	AF10				
4	IO_L06N_4/VRP_4	AL7				
4	IO_L06P_4/VRN_4	AM7				
4	IO_L07N_4	AE11				
4	IO_L07P_4/VREF_4	AF11				
4	IO_L08N_4	AG10				
4	IO_L08P_4	AH10				
4	IO_L09N_4	AK8				
4	IO_L09P_4/VREF_4	AL8				
4	IO_L19N_4	AE12	NC	NC		
4	IO_L19P_4	AF12	NC	NC		
4	IO_L20N_4	AJ9	NC	NC		
4	IO_L20P_4	AK9	NC	NC		
4	IO_L21N_4	AL9	NC	NC		
4	IO_L21P_4	AM9	NC	NC		
4	IO_L25N_4	AG11	NC	NC		
4	IO_L25P_4	AH11	NC	NC		
4	IO_L26N_4	AH12	NC	NC		
4	IO_L26P_4	AJ12	NC	NC		
4	IO_L27N_4	AK10	NC	NC		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L32P_7	N24		
7	IO_L32N_7	N25		
7	IO_L31P_7	G33		
7	IO_L31N_7	G34		
7	IO_L30P_7	H31		
7	IO_L30N_7	G32		
7	IO_L29P_7	N27		
7	IO_L29N_7	M28		
7	IO_L28P_7	G28		
7	IO_L28N_7/VREF_7	G29		
7	IO_L27P_7	F33		
7	IO_L27N_7	F34		
7	IO_L26P_7	M26		
7	IO_L26N_7	M27		
7	IO_L25P_7	F31		
7	IO_L25N_7	F32		
7	IO_L24P_7	F30		
7	IO_L24N_7	G30		
7	IO_L23P_7	L25		
7	IO_L23N_7	M25		
7	IO_L22P_7	F27		
7	IO_L22N_7/VREF_7	F28		
7	IO_L21P_7	E29		
7	IO_L21N_7	F29		
7	IO_L20P_7	L28		
7	IO_L20N_7	K28		
7	IO_L19P_7	D33		
7	IO_L19N_7	D34		
7	IO_L18P_7	D32		
7	IO_L18N_7	E32		
7	IO_L17P_7	K26		
7	IO_L17N_7	L26		
7	IO_L16P_7	D31		
7	IO_L16N_7/VREF_7	E31		
7	IO_L15P_7	D29		
7	IO_L15N_7	D30		
7	IO_L14P_7	J28		
7	IO_L14N_7	J29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L47P_3	AC10		
3	IO_L46N_3	AE7		
3	IO_L46P_3	AE8		
3	IO_L45N_3/VREF_3	AE5		
3	IO_L45P_3	AE6		
3	IO_L44N_3	AB13		
3	IO_L44P_3	AC13		
3	IO_L43N_3	AE3		
3	IO_L43P_3	AE4		
3	IO_L42N_3	AE1		
3	IO_L42P_3	AE2		
3	IO_L41N_3	AD10		
3	IO_L41P_3	AD11		
3	IO_L40N_3	AF6		
3	IO_L40P_3	AF7		
3	IO_L39N_3/VREF_3	AF4		
3	IO_L39P_3	AF5		
3	IO_L38N_3	AC12		
3	IO_L38P_3	AD12		
3	IO_L37N_3	AF1		
3	IO_L37P_3	AF2		
3	IO_L36N_3	AG6		
3	IO_L36P_3	AG7		
3	IO_L35N_3	AE9		
3	IO_L35P_3	AE10		
3	IO_L34N_3	AF3		
3	IO_L34P_3	AG3		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AE11		
3	IO_L32P_3	AE12		
3	IO_L31N_3	AH6		
3	IO_L31P_3	AH7		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AH4		
3	IO_L29N_3	AD13		
3	IO_L29P_3	AE13		
3	IO_L28N_3	AH2		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L59N_2	AA11	
2	IO_L59P_2	AA12	
2	IO_L60N_2	W1	
2	IO_L60P_2	W2	
2	IO_L85N_2	Y2	
2	IO_L85P_2	Y3	
2	IO_L86N_2	AA9	
2	IO_L86P_2	AA10	
2	IO_L87N_2	AA5	
2	IO_L87P_2	AA6	
2	IO_L88N_2/VREF_2	AA4	
2	IO_L88P_2	Y4	
2	IO_L89N_2	AA7	
2	IO_L89P_2	AA8	
2	IO_L90N_2	AA2	
2	IO_L90P_2	AA3	
3	IO_L90N_3	AB5	
3	IO_L90P_3	AB6	
3	IO_L89N_3	AB11	
3	IO_L89P_3	AB12	
3	IO_L88N_3	AB2	
3	IO_L88P_3	AB3	
3	IO_L87N_3/VREF_3	AB4	
3	IO_L87P_3	AC4	
3	IO_L86N_3	AB9	
3	IO_L86P_3	AB10	
3	IO_L85N_3	AC2	
3	IO_L85P_3	AC3	
3	IO_L60N_3	AD5	
3	IO_L60P_3	AD6	
3	IO_L59N_3	AB7	
3	IO_L59P_3	AB8	
3	IO_L58N_3	AD1	
3	IO_L58P_3	AD2	
3	IO_L57N_3/VREF_3	AE4	
3	IO_L57P_3	AE5	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L19N_3	AM3	
3	IO_L19P_3	AN3	
3	IO_L18N_3	AN1	
3	IO_L18P_3	AN2	
3	IO_L17N_3	AG12	
3	IO_L17P_3	AH12	
3	IO_L16N_3	AP6	
3	IO_L16P_3	AP7	
3	IO_L15N_3/VREF_3	AP3	
3	IO_L15P_3	AP4	
3	IO_L14N_3	AH10	
3	IO_L14P_3	AH11	
3	IO_L13N_3	AR6	
3	IO_L13P_3	AR7	
3	IO_L12N_3	AR4	
3	IO_L12P_3	AR5	
3	IO_L11N_3	AH8	
3	IO_L11P_3	AH9	
3	IO_L10N_3	AR2	
3	IO_L10P_3	AR3	
3	IO_L09N_3/VREF_3	AP2	
3	IO_L09P_3	AR1	
3	IO_L08N_3	AJ10	
3	IO_L08P_3	AJ11	
3	IO_L07N_3	AT7	
3	IO_L07P_3	AT8	
3	IO_L72N_3	AT3	
3	IO_L72P_3	AT4	
3	IO_L71N_3	AJ12	
3	IO_L71P_3	AK12	
3	IO_L70N_3	AT1	
3	IO_L70P_3	AT2	
3	IO_L69N_3/VREF_3	AT6	
3	IO_L69P_3	AU6	
3	IO_L68N_3	AK10	
3	IO_L68P_3	AK11	
3	IO_L67N_3	AT5	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	BB34	
N/A	GND	AV34	
N/A	GND	AP34	
N/A	GND	AK34	
N/A	GND	AF34	
N/A	GND	AC34	
N/A	GND	Y34	
N/A	GND	U34	
N/A	GND	N34	
N/A	GND	J34	
N/A	GND	E34	
N/A	GND	A34	
N/A	GND	AD31	
N/A	GND	W31	
N/A	GND	BB30	
N/A	GND	AV30	
N/A	GND	AP30	
N/A	GND	J30	
N/A	GND	E30	
N/A	GND	A30	
N/A	GND	BB26	
N/A	GND	AV26	
N/A	GND	AP26	
N/A	GND	AE26	
N/A	GND	AD26	
N/A	GND	AC26	
N/A	GND	AB26	
N/A	GND	AA26	
N/A	GND	Y26	
N/A	GND	W26	
N/A	GND	V26	
N/A	GND	J26	
N/A	GND	E26	
N/A	GND	A26	
N/A	GND	AF25	
N/A	GND	AE25	
N/A	GND	AD25	