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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	812
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-6ff1148c

implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test Boundary-Scan instructions. In test mode, Boundary-Scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II Pro / Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Enviornment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See **DS080**, *System ACE CompactFlash Solution* for more information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II Pro / Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops and latches, distributed SelectRAM+, and block SelectRAM+ memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro / Virtex-II Pro X by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to **www.xilinx.com/ipcenter** for the latest and most complete list of cores.

Hardware Cores

- Bus Infrastructure cores (arbiters, bridges, and more)
- Memory cores (DDR, Flash, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

Virtex-II Pro / Virtex-II Pro X Device/Package Combinations and Maximum I/Os

Offerings include ball grid array (BGA) packages with 1.0 mm pitch. In addition to traditional wire-bond interconnect (FG/FGG packages), flip-chip interconnect (FF packages) is used in some of the BGA offerings. Flip-chip interconnect construction supports more I/Os than are possible in wire-bond versions of similar packages, providing a high pin count and excellent power dissipation.

The device/package combination table (Table 3) details the maximum number of user I/Os and RocketIO / RocketIO X MGTs for each device and package using wire-bond or flip-chip technology.

The FF1148 and FF1696 packages have no RocketIO transceivers bonded out. Extra SelectIO-Ultra resources occupy available pins in these packages, resulting in a higher user I/O count. These packages are available for the XC2VP40, XC2VP50, and XC2VP100 devices only.

The I/Os per package count includes all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), VBATT, and the RocketIO / RocketIO X transceiver pins.

Table 3: **Virtex-II Pro Device/Package Combinations and Maximum Number of Available I/Os**

Package(1)	FG256/ FGG256	FG456/ FGG456	FG676	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**
Size (mm)	**17 x 17**	**23 x 23**	**26 x 26**	**27 x 27**	**31 x 31**	**35 x 35**	**35 x 35**	**40 x 40**	**42.5 x 42.5**	**42.5 x 42.5**
XC2VP2	140 / 4	156 / 4		204 / 4						
XC2VP4	140 / 4	248 / 4		348 / 4						
XC2VP7		248 / 8		396 / 8	396 / 8					
XC2VP20			404 / 8		556 / 8	564 / 8				
XC2VPX20					552 / 8(2)					
XC2VP30			416 / 8		556 / 8	644 / 8				
XC2VP40			416 / 8			692 / 12	804 / 0(3)			
XC2VP50						692 / 16	812 / 0(3)	852 / 16		
XC2VP70								964 / 16	996 / 20	
XC2VPX70									992 / 20(2)	
XC2VP100									1,040 / 20	1,164 / 0(3)

Notes:
1. Wirebond packages FG256, FG456, and FG676 are also available in Pb-free versions FGG256, FGG456, and FGG676. See Virtex-II Pro Ordering Examples for details on how to order.
2. Virtex-II Pro X device is equipped with RocketIO X transceiver cores.
3. The RocketIO transceivers in devices in the FF1148 and FF1696 packages are not bonded out to the package pins.

Maximum Performance

Maximum performance of the RocketIO / RocketIO X transceiver and the PowerPC processor block varies, depending on package style and speed grade. See Table 4 for details. Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics contains the rest of the FPGA fabric performance parameters.

Table 4: **Maximum RocketIO / RocketIO X Transceiver and Processor Block Performance**

Device	Speed Grade			Units
	-7(1)	-6	-5	
RocketIO X Transceiver FlipChip (FF)	N/A	6.25(3)	4.25(3)	Gb/s
RocketIO Transceiver FlipChip (FF)	3.125	3.125	2.0	Gb/s
RocketIO Transceiver Wirebond (FG)	2.5	2.5	2.0	Gb/s
PowerPC Processor Block	400(2)	350(2)	300	MHz

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1 to identify dual-processor devices.
3. XC2VPX70 is only available at fixed 4.25 Gb/s baud rate.

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

Sum of Products

Each Virtex-II Pro slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 43.

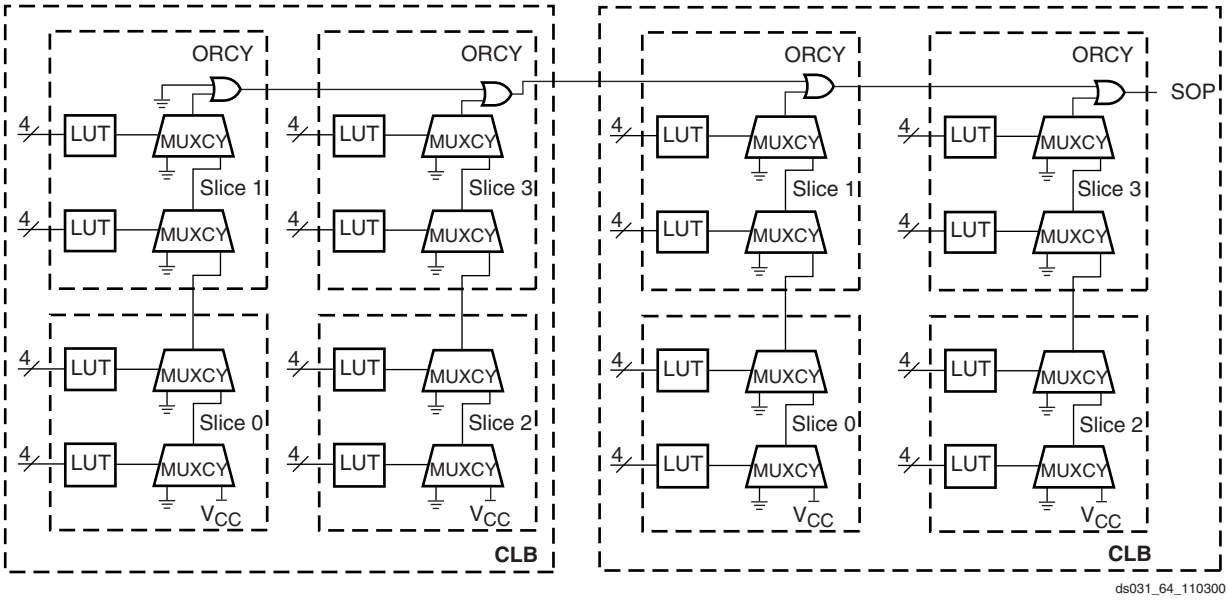

Figure 43: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 44 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

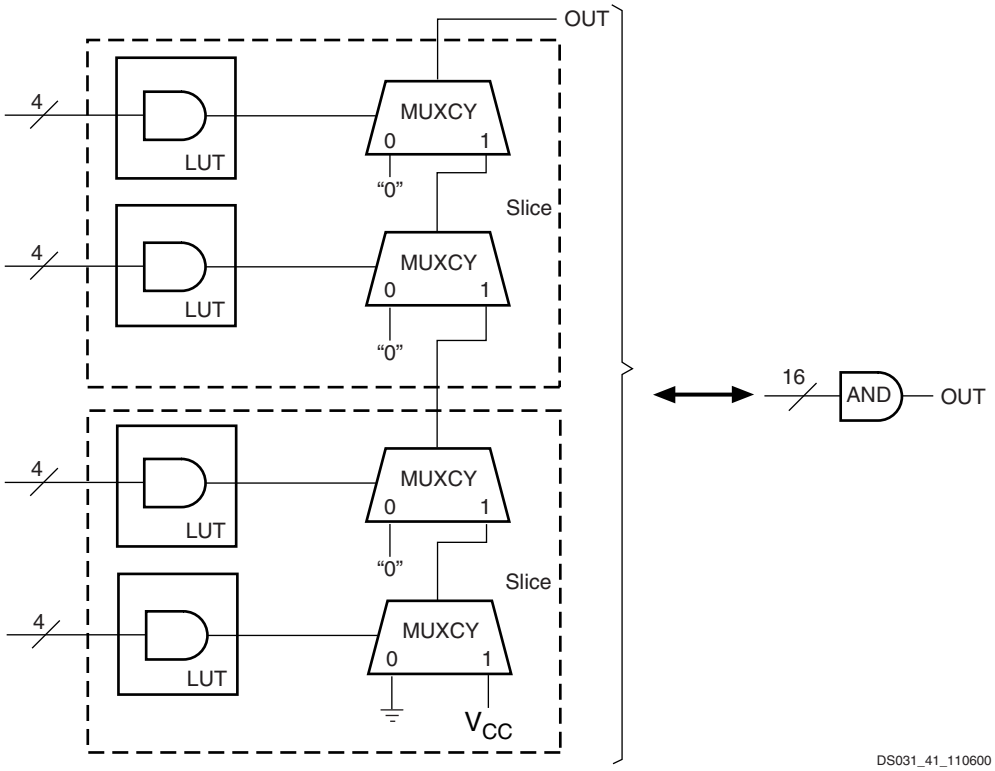

Figure 44: **Wide-Input AND Gate (16 Inputs)**

Date	Version	Revision
12/03/02	2.5	Updated parametric information in: • Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.5V to –0.3V for 3.3V. • Table 2: Add footnote (2) regarding V_{CCAUX} voltage droop. Renumbered other notes. • Table 12: Add waveform diagrams (Figure 1 and Figure 2) illustrating DV_{OUT} (single-ended) and DV_{PPOUT} (differential). • Table 23: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct T_{RCLK} and T_{FCLK} values and unit of measurement. • Table 60: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL.
01/20/03	2.6	Updated parametric information in: • Table 12: Correct DV_{IN} Min (200 mV to 175 mV) and DV_{IN} Max (1000 mV to 2000 mV). • Table 23: Correct T_{RCLK} /T_{FCLK} Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max T_{GJTT} parameter. • Table 59: Correct hyperlink in footnote (1) to point directly to Answer Record 13645. • Move clock parameters from Table 18, Table 19, Table 20, and Table 21 to Table 16.
03/24/03	2.7	• Added/updated timing parameters from speedsfile **v1.76**. • Table 2: Delete first table footnote and renumber all others. • Table 3: Add "sample-tested" to I_L. Remove "Device" column, unnecessary. • Table 8: Update V_{OCM} (Typ) to 1.250V. • Table 10: Update LVPECL_25 DC parameters. • Table 23: Update F_{GCLK} frequency ranges. Break out T_{GJTT} by operating speed. • Table 27: Update F_{GTX} frequency ranges. Correct T_{DJ} to 0.17 UI, T_{RJ} to o.18 UI. • Table 39: Update V_{REF} (Typ) for HSTL Class I/II from 1.08V to 0.90V. • Table 43, Table 44: Correct parameter name "CE input (WS)" to "SR input". • Table 64: Break out T_{DCD_CLK0} by device type.
05/27/03	2.8	• Updated time and frequency parameters as per speedsfile **v1.78**. • Table 3: Added values for I_{REF}, I_L, I_{RPU}, I_{RPD} • Corrected I_{CCINTQ} (Table 4) and $I_{CCINTMIN}$ (Table 5) for XC2VP20 to 600 mA. • Table 4: Updated/Added Typ and Max quiescent current values for XC2VP7 and XC2VP20. Added footnote specifying parameters are for Commercial Grade parts. • Table 5: Added footnote specifying parameters are for Commercial Grade parts. • Table 6: Corrected V_{IH} (Max) for LVTTL and LVCMOS33 standards from 3.6V to 3.45V. Changed V_{IL} (Min) for all standards to –0.2V. Corrected V_{IL} (Max) for LVCMOS15 and LVCMOS18 from 20% V_{CCO} to 30% V_{CCO}. • Table 10: Corrected LVPECL_25 Min and Max values for V_{IH} and V_{IL}. Added explanatory text above table. • Table 13 and Table 14 (pin-pin and reg-reg performance): Changed device specified from XC2VP7FF672-6 to XC2VP20FF1152-6. • Table 15: Updated to show devices XC2VP7 and XC2VP20 as Preliminary for the -6 speed grade and Production for the -5 speed grade. • Removed former Table 32, Standard Capacitive Loads. • Table 52: Updated T_{TAPTCK} from 4.0 ns to 5.5 ns. • Table 59: Modified footnote referenced at CLKFX/CLKFX180 to point to the online Jitter Calculator. • Added Figure 6 and accompanying procedure for measuring standard adjustments.
05/27/03 (cont'd)	2.8 (cont'd)	• Table 1: Footnote (2) rewritten to specify “one or more banks.” • Table 57: Some DCM parameters were erroneously missing from v2.8 (single-module version) due to a document compilation error. The concatenated full data sheet version was not affected. These parameters have been restored.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	IO_L85N_7	G2
7	IO_L06P_7	G3
7	IO_L06N_7	G4
7	IO_L04P_7	F1
7	IO_L04N_7/VREF_7	F2
7	IO_L03P_7	F3
7	IO_L03N_7	F4
7	IO_L02P_7	F5
7	IO_L02N_7	E4
7	IO_L01P_7/VRN_7	E2
7	IO_L01N_7/VRP_7	E3
0	VCCO_0	F8
0	VCCO_0	F7
0	VCCO_0	E8
1	VCCO_1	F9
1	VCCO_1	F10
1	VCCO_1	E9
2	VCCO_2	H12
2	VCCO_2	H11
2	VCCO_2	G11
3	VCCO_3	K11
3	VCCO_3	J12
3	VCCO_3	J11
4	VCCO_4	M9
4	VCCO_4	L9
4	VCCO_4	L10
5	VCCO_5	M8
5	VCCO_5	L8
5	VCCO_5	L7
6	VCCO_6	K6
6	VCCO_6	J6
6	VCCO_6	J5
7	VCCO_7	H6
7	VCCO_7	H5

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L88N_7/VREF_7	L5			
7	IO_L86P_7	L6			
7	IO_L86N_7	K6			
7	IO_L85P_7	K1			
7	IO_L85N_7	K2			
7	IO_L60P_7	K3	NC		
7	IO_L60N_7	K4	NC		
7	IO_L58P_7	K5	NC		
7	IO_L58N_7/VREF_7	J5	NC		
7	IO_L56P_7	J1	NC		
7	IO_L56N_7	J2	NC		
7	IO_L55P_7	J3	NC		
7	IO_L55N_7	J4	NC		
7	IO_L54P_7	J6	NC		
7	IO_L54N_7	H5	NC		
7	IO_L52P_7	H1	NC		
7	IO_L52N_7/VREF_7	H2	NC		
7	IO_L50P_7	H3	NC		
7	IO_L50N_7	H4	NC		
7	IO_L49P_7	G1	NC		
7	IO_L49N_7	G2	NC		
7	IO_L48P_7	G3	NC		
7	IO_L48N_7	G4	NC		
7	IO_L46P_7	G5	NC		
7	IO_L46N_7/VREF_7	F5	NC		
7	IO_L43P_7	F1	NC		
7	IO_L43N_7	F2	NC		
7	IO_L06P_7	F3			
7	IO_L06N_7	F4			
7	IO_L04P_7	E1			
7	IO_L04N_7/VREF_7	E2			
7	IO_L03P_7	E3			
7	IO_L03N_7	E4			
7	IO_L02P_7	D1			
7	IO_L02N_7	D2			
7	IO_L01P_7/VRN_7	C1			
7	IO_L01N_7/VRP_7	C2			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	VCCO_3	AB24			
4	VCCO_4	U14			
4	VCCO_4	U15			
4	VCCO_4	V16			
4	VCCO_4	V17			
4	VCCO_4	AC16			
4	VCCO_4	AD19			
4	VCCO_4	AD22			
5	VCCO_5	U12			
5	VCCO_5	U13			
5	VCCO_5	V10			
5	VCCO_5	V11			
5	VCCO_5	AC11			
5	VCCO_5	AD5			
5	VCCO_5	AD8			
6	VCCO_6	P10			
6	VCCO_6	R10			
6	VCCO_6	T4			
6	VCCO_6	T9			
6	VCCO_6	U9			
6	VCCO_6	W3			
6	VCCO_6	AB3			
7	VCCO_7	E3			
7	VCCO_7	H3			
7	VCCO_7	K9			
7	VCCO_7	L4			
7	VCCO_7	L9			
7	VCCO_7	M10			
7	VCCO_7	N10			
N/A	PROG_B	B1			
N/A	HSWAP_EN	B3			
N/A	DXP	A3			
N/A	DXN	C4			
N/A	AVCCAUXTX4	B5			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L48P_2	H1	NC		
2	IO_L49N_2	J7	NC		
2	IO_L49P_2	J6	NC		
2	IO_L50N_2	J5	NC		
2	IO_L50P_2	J4	NC		
2	IO_L51N_2	J3	NC		
2	IO_L51P_2	J2	NC		
2	IO_L52N_2/VREF_2	K6	NC		
2	IO_L52P_2	K5	NC		
2	IO_L53N_2	K4	NC		
2	IO_L53P_2	K3	NC		
2	IO_L54N_2	J1	NC		
2	IO_L54P_2	K1	NC		
2	IO_L55N_2	K7	NC		
2	IO_L55P_2	L8	NC		
2	IO_L56N_2	L7	NC		
2	IO_L56P_2	M7	NC		
2	IO_L57N_2	L6	NC		
2	IO_L57P_2	L5	NC		
2	IO_L58N_2/VREF_2	L4	NC		
2	IO_L58P_2	L3	NC		
2	IO_L59N_2	L2	NC		
2	IO_L59P_2	L1	NC		
2	IO_L60N_2	M8	NC		
2	IO_L60P_2	N8	NC		
2	IO_L85N_2	M6			
2	IO_L85P_2	M5			
2	IO_L86N_2	M4			
2	IO_L86P_2	M3			
2	IO_L87N_2	M2			
2	IO_L87P_2	M1			
2	IO_L88N_2/VREF_2	N7			
2	IO_L88P_2	N6			
2	IO_L89N_2	N5			
2	IO_L89P_2	N4			
2	IO_L90N_2	N3			
2	IO_L90P_2	N2			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	K15			
N/A	GND	K17			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M10			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M17			
N/A	GND	N10			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	N17			
N/A	GND	P10			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	P17			
N/A	GND	R10			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	VCCO_4		AA11			
4	VCCO_4		AA10			
5	VCCO_5		AB21			
5	VCCO_5		AB20			
5	VCCO_5		AB19			
5	VCCO_5		AB18			
5	VCCO_5		AA21			
5	VCCO_5		AA20			
5	VCCO_5		AA19			
5	VCCO_5		AA18			
5	VCCO_5		AA17			
5	VCCO_5		AA16			
6	VCCO_6		AB22			
6	VCCO_6		AA22			
6	VCCO_6		Y22			
6	VCCO_6		Y21			
6	VCCO_6		W22			
6	VCCO_6		W21			
6	VCCO_6		V22			
6	VCCO_6		V21			
6	VCCO_6		U21			
6	VCCO_6		T21			
7	VCCO_7		R21			
7	VCCO_7		P21			
7	VCCO_7		N22			
7	VCCO_7		N21			
7	VCCO_7		M22			
7	VCCO_7		M21			
7	VCCO_7		L22			
7	VCCO_7		L21			
7	VCCO_7		K22			
7	VCCO_7		J22			
N/A	CCLK		AC7			
N/A	PROG_B		G24			
N/A	DONE		AC8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	VCCINT		Y13			
N/A	VCCINT		Y12			
N/A	VCCINT		W20			
N/A	VCCINT		W11			
N/A	VCCINT		V20			
N/A	VCCINT		V11			
N/A	VCCINT		U20			
N/A	VCCINT		U11			
N/A	VCCINT		T20			
N/A	VCCINT		T11			
N/A	VCCINT		R20			
N/A	VCCINT		R11			
N/A	VCCINT		P20			
N/A	VCCINT		P11			
N/A	VCCINT		N20			
N/A	VCCINT		N11			
N/A	VCCINT		M20			
N/A	VCCINT		M11			
N/A	VCCINT		L19			
N/A	VCCINT		L18			
N/A	VCCINT		L17			
N/A	VCCINT		L16			
N/A	VCCINT		L15			
N/A	VCCINT		L14			
N/A	VCCINT		L13			
N/A	VCCINT		L12			
N/A	GND		AK22			
N/A	GND		AK9			
N/A	GND		AJ29			
N/A	GND		AJ2			
N/A	GND		AH28			
N/A	GND		AH17			
N/A	GND		AH14			
N/A	GND		AH3			
N/A	GND		AG27			
N/A	GND		AG22			

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L34P_0	E27	NC	
0	IO_L35N_0	L26	NC	
0	IO_L35P_0	L25	NC	
0	IO_L36N_0	G26	NC	
0	IO_L36P_0/VREF_0	H26	NC	
0	IO_L37N_0	E26		
0	IO_L37P_0	F26		
0	IO_L38N_0	K25		
0	IO_L38P_0	K24		
0	IO_L39N_0	C26		
0	IO_L39P_0	D26		
0	IO_L43N_0	H25		
0	IO_L43P_0	J25		
0	IO_L44N_0	M25		
0	IO_L44P_0	M24		
0	IO_L45N_0	F25		
0	IO_L45P_0/VREF_0	G25		
0	IO_L46N_0	C25		
0	IO_L46P_0	D25		
0	IO_L47N_0	L23		
0	IO_L47P_0	M22		
0	IO_L48N_0	H24		
0	IO_L48P_0	J24		
0	IO_L49N_0	E25		
0	IO_L49P_0	E24		
0	IO_L50_0/No_Pair	N23		
0	IO_L53_0/No_Pair	M23		
0	IO_L54N_0	H23		
0	IO_L54P_0	J23		
0	IO_L55N_0	F24		
0	IO_L55P_0	G23		
0	IO_L56N_0	K22		
0	IO_L56P_0	L22		
0	IO_L57N_0	C23		
0	IO_L57P_0/VREF_0	D23		
0	IO_L58N_0	H22		
0	IO_L58P_0	J22		
0	IO_L59N_0	N22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L29N_5	AK26	NC	
5	IO_L29P_5	AL26	NC	
5	IO_L28N_5	AL27	NC	
5	IO_L28P_5	AM27	NC	
5	IO_L27N_5/VREF_5	AR28		
5	IO_L27P_5	AT28		
5	IO_L26N_5	AH26		
5	IO_L26P_5	AH27		
5	IO_L25N_5	AL28		
5	IO_L25P_5	AM28		
5	IO_L21N_5	AT29		
5	IO_L21P_5	AU29		
5	IO_L20N_5	AJ27		
5	IO_L20P_5	AJ28		
5	IO_L19N_5	AP29		
5	IO_L19P_5	AR29		
5	IO_L09N_5/VREF_5	AM29		
5	IO_L09P_5	AN29		
5	IO_L08N_5	AK29		
5	IO_L08P_5	AL29		
5	IO_L07N_5/VREF_5	AT30		
5	IO_L07P_5	AU30		
5	IO_L06N_5/VRP_5	AP30		
5	IO_L06P_5/VRN_5	AR30		
5	IO_L05_5/No_Pair	AK28		
5	IO_L03N_5/D4	AM30		
5	IO_L03P_5/D5	AN30		
5	IO_L02N_5/D6	AL30		
5	IO_L02P_5/D7	AK30		
5	IO_L01N_5/RDWR_B	AR31		
5	IO_L01P_5/CS_B	AT31		
6	IO_L01P_6/VRN_6	AU33		
6	IO_L01N_6/VRP_6	AT33		
6	IO_L02P_6	AT32		
6	IO_L02N_6	AR32		
6	IO_L03P_6	AN31		
6	IO_L03N_6/VREF_6	AM31		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L86P_2		Y12		
2	IO_L87N_2		AA9		
2	IO_L87P_2		AA10		
2	IO_L88N_2/VREF_2		AA6		
2	IO_L88P_2		AA7		
2	IO_L89N_2		AA12		
2	IO_L89P_2		AB12		
2	IO_L90N_2		AA3		
2	IO_L90P_2		AA4		
3	IO_L90N_3		AB3		
3	IO_L90P_3		AB4		
3	IO_L89N_3		AB6		
3	IO_L89P_3		AB7		
3	IO_L88N_3		AB9		
3	IO_L88P_3		AB10		
3	IO_L87N_3/VREF_3		AC3		
3	IO_L87P_3		AC4		
3	IO_L86N_3		AC11		
3	IO_L86P_3		AC12		
3	IO_L85N_3		AC6		
3	IO_L85P_3		AC7		
3	IO_L60N_3		AC9		
3	IO_L60P_3		AC10		
3	IO_L59N_3		AD9		
3	IO_L59P_3		AD10		
3	IO_L58N_3		AD1		
3	IO_L58P_3		AD2		
3	IO_L57N_3/VREF_3		AD3		
3	IO_L57P_3		AD4		
3	IO_L56N_3		AD11		
3	IO_L56P_3		AD12		
3	IO_L55N_3		AD5		
3	IO_L55P_3		AD6		
3	IO_L54N_3		AD7		
3	IO_L54P_3		AD8		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L45N_7	T36	
7	IO_L44P_7	W32	
7	IO_L44N_7	W33	
7	IO_L43P_7	R41	
7	IO_L43N_7	R42	
7	IO_L42P_7	P40	
7	IO_L42N_7	R40	
7	IO_L41P_7	V36	
7	IO_L41N_7	V37	
7	IO_L40P_7	R38	
7	IO_L40N_7/VREF_7	R39	
7	IO_L39P_7	P38	
7	IO_L39N_7	R37	
7	IO_L38P_7	V34	
7	IO_L38N_7	V35	
7	IO_L37P_7	P41	
7	IO_L37N_7	P42	
7	IO_L36P_7	P36	
7	IO_L36N_7	P37	
7	IO_L35P_7	V32	
7	IO_L35N_7	V33	
7	IO_L34P_7	M41	
7	IO_L34N_7/VREF_7	N41	
7	IO_L33P_7	N39	
7	IO_L33N_7	N40	
7	IO_L32P_7	U35	
7	IO_L32N_7	U36	
7	IO_L31P_7	N36	
7	IO_L31N_7	N37	
7	IO_L30P_7	M39	
7	IO_L30N_7	M40	
7	IO_L29P_7	U32	
7	IO_L29N_7	U33	
7	IO_L28P_7	M37	
7	IO_L28N_7/VREF_7	M38	
7	IO_L27P_7	L37	
7	IO_L27N_7	M36	