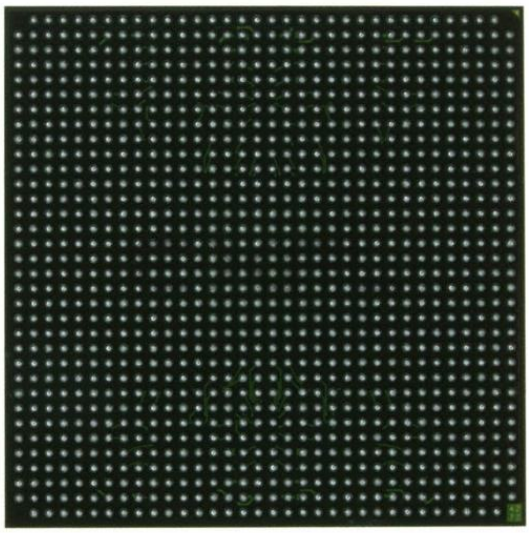
AMD Xilinx - XC2VP50-6FF1152C Datasheet



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Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-6ff1152c

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II Pro device configuration using Boundary-Scan is compatible with with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 32: **Virtex-II Pro Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 33 lists the default total number of bits required to configure each device.

Table 33: **Virtex-II Pro Default Bitstream Lengths**

Device	Number of Configuration Bits
XC2VP2	1,305,376
XC2VP4	3,006,496
XC2VP7	4,485,408
XC2VP20	8,214,560
XC2VPX20	8,214,560
XC2VP30	11,589,920
XC2VP40	15,868,192
XC2VP50	19,021,344
XC2VP70	26,098,976
XC2VPX70	26,098,976
XC2VP100	34,292,768

Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Table 19: **Processor Block JTAG Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	$T_{PCCK_}$JTAG/ $T_{PCKC_}$JTAG	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
JTAG reset input	$T_{PCCK_}$JTAGRST/ $T_{PCKC_}$JTAGRST	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
Clock to Out					
JTAG control outputs	$T_{PCKCO_}$JTAG	1.34	1.54	1.69	ns, max

Table 20: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMDSOCMCLK)					
Data-Side On-Chip Memory data bus inputs	$T_{PDCK_}$DSOCM/ $T_{PCKD_}$DSOCM	0.73/ 0.83	0.84/ 0.95	0.92/ 1.05	ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	$T_{PCKCO_}$DSOCM	1.58	1.82	1.99	ns, max
Data-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$DSOCM	1.46	1.68	1.84	ns, max
Data-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$DSOCM	0.90	1.03	1.13	ns, max

Table 21: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMISOCMCLK)					
Instruction-Side On-Chip Memory data bus inputs	$T_{PDCK_}$ISOCM/ $T_{PCKD_}$ISOCM	0.81/ 0.68	0.93/ 0.78	1.02/ 0.86	ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	$T_{PCKCO_}$ISOCM	1.33	1.53	1.68	ns, max
Instruction-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$ISOCM	1.52	1.75	1.92	ns, max
Instruction-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$ISOCM	1.35	1.55	1.70	ns, max

Table 24: **RocketIO X Receiver Switching Characteristics**(1)

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance using default equalization and PRBS-15 pattern	T_{JTOL}	2.488 Gb/s		0.80	0.65	UI(2)
		3.125 Gb/s		0.80	0.65	UI
		4.25 Gb/s		0.80	0.65	UI
		6.25 Gb/s		0.80	0.65	UI
Receive random jitter tolerance	T_{RJTOL}	2.488 Gb/s		0.30		UI
		3.125 Gb/s		0.30		UI
		4.25 Gb/s		0.30		UI
		6.25 Gb/s		0.30		UI
Receive sinusoidal jitter tolerance measured at 70 MHz	T_{SJTOL}	2.488 Gb/s		0.30	0.15	UI
		3.125 Gb/s		0.30	0.15	UI
		4.25 Gb/s		0.30	0.15	UI
		6.25 Gb/s		0.30	0.15	UI
Receive deterministic jitter tolerance	T_{DJTOL}	2.488 Gb/s		0.55	0.45	UI
		3.125 Gb/s		0.55	0.45	UI
		4.25 Gb/s		0.55	0.45	UI
		6.25 Gb/s		0.50	0.45	UI
Receive latency(3)	T_{RXLAT}			25	34(4)	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%
Differential receive input sensitivity	V_{EYE}			120	250	mV

Notes:
1. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.
2. UI = Unit Interval
3. Receive latency delay RXP/RXN to RXDATA. Refer to ***RocketIO X Transceiver User Guide*** for more information on calculating latency.
4. This maximum may occur when certain conditions are present and clock correction and channel bonding are enabled. If these functions are both disabled, the maximum will be near the typical values.

Table 27: **RocketIO Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	1.0		3.125(1)	Gb/s
		Wirebond packages	1.0		2.5(1)	Gb/s
Serial data rate, half-speed clock(3) (2X oversampling)		Flipchip packages	0.600		1.0	Gb/s
		Wirebond packages	0.600		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}	2.126 Gb/s – 3.125 Gb/s			0.17	UI(2)
		1.0626 Gb/s – 2.125 Gb/s			0.08	UI
		1.0 Gb/s – 1.0625 Gb/s			0.05	UI
		600 Mb/s – 999 Mb/s			0.08(4)	UI
Serial data output random jitter	T_{RJ}	2.126 Gb/s – 3.125 Gb/s			0.18	UI
		1.0626 Gb/s – 2.125 Gb/s			0.19	UI
		1.0 Gb/s – 1.0625 Gb/s			0.18	UI
		600 Mb/s – 999 Mb/s			0.18(4)	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(5)	T_{TXLAT}	Including CRC		14	17	TXUSR CLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

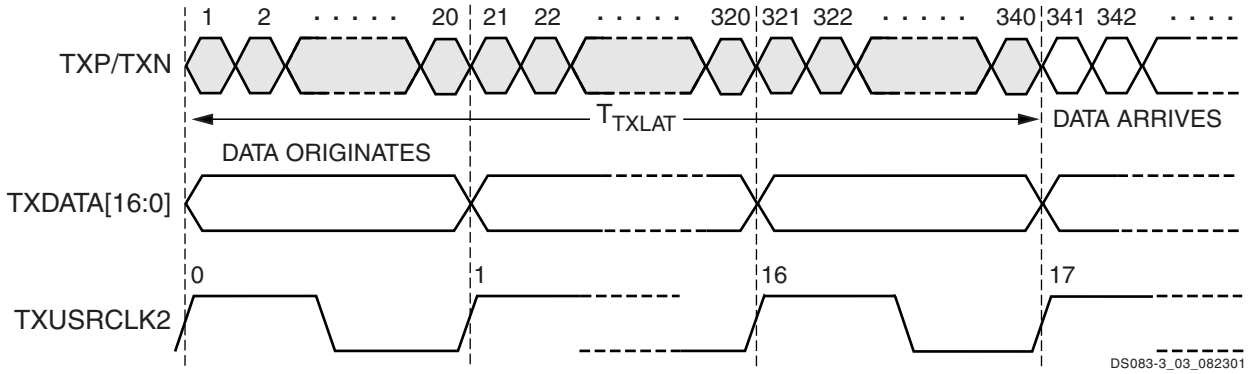

Figure 5: **RocketIO Transmit Latency (Maximum, Including CRC)**

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 39 shows the test setup parameters used for measuring Input standard adjustments (see Table 36, page 25).

Table 39: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.3	1.65	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Tnscvr Logic), Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1.15 – 0.3	1.15 + 0.3	1.15	

Notes:

1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See ***Virtex-II Pro Platform FPGA User Guide*** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Pro Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 38) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

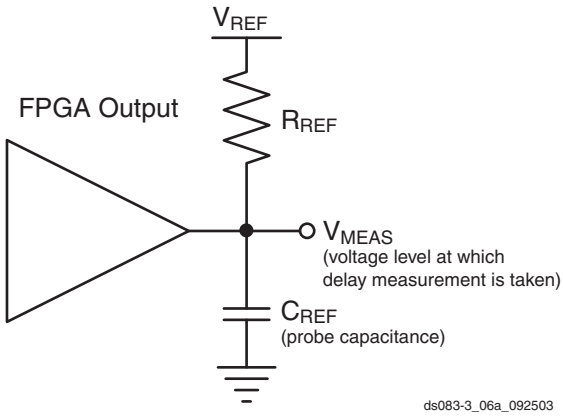

Figure 6: **Generalized Test Setup**

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.65	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	0
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Measured as per PCI specification.
3. Measured as per PCI-X specification.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	AVCCAUXRX21	AE7			
N/A	VTRXPAD21	AE6			
N/A	RXNPAD21	AF7			
N/A	RXPPAD21	AF6			
N/A	GNDA21	AD6			
N/A	TXPPAD21	AF5			
N/A	TXNPAD21	AF4			
N/A	VTTXPAD21	AE4			
N/A	AVCCAUXTX21	AE5			
N/A	M2	AD4			
N/A	M0	AF3			
N/A	M1	AE3			
N/A	TDI	D3			
N/A	VCCINT	G10			
N/A	VCCINT	G13			
N/A	VCCINT	G14			
N/A	VCCINT	G17			
N/A	VCCINT	J9			
N/A	VCCINT	J18			
N/A	VCCINT	K7			
N/A	VCCINT	K10			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K17			
N/A	VCCINT	K20			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	N7			
N/A	VCCINT	N20			
N/A	VCCINT	P7			
N/A	VCCINT	P20			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U7			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L48P_2	H1	NC		
2	IO_L49N_2	J7	NC		
2	IO_L49P_2	J6	NC		
2	IO_L50N_2	J5	NC		
2	IO_L50P_2	J4	NC		
2	IO_L51N_2	J3	NC		
2	IO_L51P_2	J2	NC		
2	IO_L52N_2/VREF_2	K6	NC		
2	IO_L52P_2	K5	NC		
2	IO_L53N_2	K4	NC		
2	IO_L53P_2	K3	NC		
2	IO_L54N_2	J1	NC		
2	IO_L54P_2	K1	NC		
2	IO_L55N_2	K7	NC		
2	IO_L55P_2	L8	NC		
2	IO_L56N_2	L7	NC		
2	IO_L56P_2	M7	NC		
2	IO_L57N_2	L6	NC		
2	IO_L57P_2	L5	NC		
2	IO_L58N_2/VREF_2	L4	NC		
2	IO_L58P_2	L3	NC		
2	IO_L59N_2	L2	NC		
2	IO_L59P_2	L1	NC		
2	IO_L60N_2	M8	NC		
2	IO_L60P_2	N8	NC		
2	IO_L85N_2	M6			
2	IO_L85P_2	M5			
2	IO_L86N_2	M4			
2	IO_L86P_2	M3			
2	IO_L87N_2	M2			
2	IO_L87P_2	M1			
2	IO_L88N_2/VREF_2	N7			
2	IO_L88P_2	N6			
2	IO_L89N_2	N5			
2	IO_L89P_2	N4			
2	IO_L90N_2	N3			
2	IO_L90P_2	N2			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L43P_0	E22				
0	IO_L44N_0	E25				
0	IO_L44P_0	D25				
0	IO_L45N_0	H21				
0	IO_L45P_0/VREF_0	G21				
0	IO_L46N_0	D22				
0	IO_L46P_0	D23				
0	IO_L47N_0	D24				
0	IO_L47P_0	C24				
0	IO_L48N_0	K20				
0	IO_L48P_0	J20				
0	IO_L49N_0	F21				
0	IO_L49P_0	E21				
0	IO_L50_0/No_Pair	C21				
0	IO_L53_0/No_Pair	C22				
0	IO_L54N_0	L19				
0	IO_L54P_0	K19				
0	IO_L55N_0	G20				
0	IO_L55P_0	F20				
0	IO_L56N_0	D21				
0	IO_L56P_0	D20				
0	IO_L57N_0	J19				
0	IO_L57P_0/VREF_0	H19				
0	IO_L67N_0	G19				
0	IO_L67P_0	F19				
0	IO_L68N_0	E19				
0	IO_L68P_0	D19				
0	IO_L69N_0	L18				
0	IO_L69P_0/VREF_0	K18				
0	IO_L73N_0	G18				
0	IO_L73P_0	F18				
0	IO_L74N_0/GCLK7P	E18				
0	IO_L74P_0/GCLK6S	D18				
0	IO_L75N_0/GCLK5P	J18				
0	IO_L75P_0/GCLK4S	H18				
1	IO_L75N_1/GCLK3P	H17				
1	IO_L75P_1/GCLK2S	J17				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
5	IO_L44N_5	AK22				
5	IO_L44P_5	AJ22				
5	IO_L43N_5	AF21				
5	IO_L43P_5	AE21				
5	IO_L39N_5	AK24				
5	IO_L39P_5	AJ24				
5	IO_L38N_5	AH22				
5	IO_L38P_5	AG22				
5	IO_L37N_5	AF22				
5	IO_L37P_5	AE22				
5	IO_L27N_5/VREF_5	AL25	NC	NC		
5	IO_L27P_5	AK25	NC	NC		
5	IO_L26N_5	AJ23	NC	NC		
5	IO_L26P_5	AH23	NC	NC		
5	IO_L25N_5	AH24	NC	NC		
5	IO_L25P_5	AG24	NC	NC		
5	IO_L21N_5	AM26	NC	NC		
5	IO_L21P_5	AL26	NC	NC		
5	IO_L20N_5	AK26	NC	NC		
5	IO_L20P_5	AJ26	NC	NC		
5	IO_L19N_5	AF23	NC	NC		
5	IO_L19P_5	AE23	NC	NC		
5	IO_L09N_5/VREF_5	AL27				
5	IO_L09P_5	AK27				
5	IO_L08N_5	AH25				
5	IO_L08P_5	AG25				
5	IO_L07N_5/VREF_5	AF24				
5	IO_L07P_5	AE24				
5	IO_L06N_5/VRP_5	AM28				
5	IO_L06P_5/VRN_5	AL28				
5	IO_L05_5/No_Pair	AF25				
5	IO_L03N_5/D4	AK28				
5	IO_L03P_5/D5	AK29				
5	IO_L02N_5/D6	AH26				
5	IO_L02P_5/D7	AG26				
5	IO_L01N_5/RDWR_B	AL29				
5	IO_L01P_5/CS_B	AL30				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L53P_6	W25				
6	IO_L53N_6	W26				
6	IO_L54P_6	AB33				
6	IO_L54N_6	AA33				
6	IO_L55P_6	Y28				
6	IO_L55N_6	Y29				
6	IO_L56P_6	W27				
6	IO_L56N_6	W28				
6	IO_L57P_6	Y31				
6	IO_L57N_6/VREF_6	Y32				
6	IO_L58P_6	W29				
6	IO_L58N_6	W30				
6	IO_L59P_6	W24				
6	IO_L59N_6	V24				
6	IO_L60P_6	AA34				
6	IO_L60N_6	Y34				
6	IO_L85P_6	W31				
6	IO_L85N_6	W32				
6	IO_L86P_6	V25				
6	IO_L86N_6	V26				
6	IO_L87P_6	Y33				
6	IO_L87N_6/VREF_6	W33				
6	IO_L88P_6	V29				
6	IO_L88N_6	V30				
6	IO_L89P_6	V27				
6	IO_L89N_6	V28				
6	IO_L90P_6	V31				
6	IO_L90N_6	V32				
7	IO_L90P_7	U32				
7	IO_L90N_7	U31				
7	IO_L89P_7	U28				
7	IO_L89N_7	U27				
7	IO_L88P_7	V33				
7	IO_L88N_7/VREF_7	U33				
7	IO_L87P_7	U30				
7	IO_L87N_7	U29				
7	IO_L86P_7	U26				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L32P_7	N24		
7	IO_L32N_7	N25		
7	IO_L31P_7	G33		
7	IO_L31N_7	G34		
7	IO_L30P_7	H31		
7	IO_L30N_7	G32		
7	IO_L29P_7	N27		
7	IO_L29N_7	M28		
7	IO_L28P_7	G28		
7	IO_L28N_7/VREF_7	G29		
7	IO_L27P_7	F33		
7	IO_L27N_7	F34		
7	IO_L26P_7	M26		
7	IO_L26N_7	M27		
7	IO_L25P_7	F31		
7	IO_L25N_7	F32		
7	IO_L24P_7	F30		
7	IO_L24N_7	G30		
7	IO_L23P_7	L25		
7	IO_L23N_7	M25		
7	IO_L22P_7	F27		
7	IO_L22N_7/VREF_7	F28		
7	IO_L21P_7	E29		
7	IO_L21N_7	F29		
7	IO_L20P_7	L28		
7	IO_L20N_7	K28		
7	IO_L19P_7	D33		
7	IO_L19N_7	D34		
7	IO_L18P_7	D32		
7	IO_L18N_7	E32		
7	IO_L17P_7	K26		
7	IO_L17N_7	L26		
7	IO_L16P_7	D31		
7	IO_L16N_7/VREF_7	E31		
7	IO_L15P_7	D29		
7	IO_L15N_7	D30		
7	IO_L14P_7	J28		
7	IO_L14N_7	J29		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L02P_2		D7		
2	IO_L03N_2		E6		
2	IO_L03P_2		D6		
2	IO_L04N_2/VREF_2		G6		
2	IO_L04P_2		F7		
2	IO_L05N_2		D3		
2	IO_L05P_2		E3		
2	IO_L06N_2		D1		
2	IO_L06P_2		D2		
2	IO_L73N_2		E1		
2	IO_L73P_2		E2		
2	IO_L74N_2		F4		
2	IO_L74P_2		F3		
2	IO_L75N_2		F1		
2	IO_L75P_2		F2		
2	IO_L76N_2/VREF_2		G3		
2	IO_L76P_2		G4		
2	IO_L77N_2		G2		
2	IO_L77P_2		G1		
2	IO_L78N_2		G5		
2	IO_L78P_2		H6		
2	IO_L79N_2		H4		
2	IO_L79P_2		H5		
2	IO_L80N_2		H3		
2	IO_L80P_2		H2		
2	IO_L81N_2		H7		
2	IO_L81P_2		J8		
2	IO_L82N_2/VREF_2		J6		
2	IO_L82P_2		J7		
2	IO_L83N_2		J5		
2	IO_L83P_2		J4		
2	IO_L84N_2		J1		
2	IO_L84P_2		J2		
2	IO_L07N_2		K9		
2	IO_L07P_2		L10		
2	IO_L08N_2		K6		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L35N_3		AH11		
3	IO_L35P_3		AH12		
3	IO_L34N_3		AH5		
3	IO_L34P_3		AH6		
3	IO_L33N_3/VREF_3		AH9		
3	IO_L33P_3		AH10		
3	IO_L32N_3		AJ11		
3	IO_L32P_3		AJ12		
3	IO_L31N_3		AJ1		
3	IO_L31P_3		AJ2		
3	IO_L30N_3		AJ5		
3	IO_L30P_3		AJ6		
3	IO_L29N_3		AJ9		
3	IO_L29P_3		AJ10		
3	IO_L28N_3		AJ7		
3	IO_L28P_3		AJ8		
3	IO_L27N_3/VREF_3		AK1		
3	IO_L27P_3		AK2		
3	IO_L26N_3		AK11		
3	IO_L26P_3		AK12		
3	IO_L25N_3		AK3		
3	IO_L25P_3		AK4		
3	IO_L24N_3		AK5		
3	IO_L24P_3		AK6		
3	IO_L23N_3		AK9		
3	IO_L23P_3		AK10		
3	IO_L22N_3		AK7		
3	IO_L22P_3		AK8		
3	IO_L21N_3/VREF_3		AL2		
3	IO_L21P_3		AL3		
3	IO_L20N_3		AL11		
3	IO_L20P_3		AL12		
3	IO_L19N_3		AL4		
3	IO_L19P_3		AL5		
3	IO_L18N_3		AL7		
3	IO_L18P_3		AL8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L87P_4/VREF_4		AP15	NC	
4	IO_L37N_4		AV15		
4	IO_L37P_4		AU15		
4	IO_L38N_4		AY14		
4	IO_L38P_4		AY15		
4	IO_L39N_4		AM16		
4	IO_L39P_4		AL16		
4	IO_L43N_4		AP16		
4	IO_L43P_4		AN16		
4	IO_L44N_4		AR16		
4	IO_L44P_4		AT16		
4	IO_L45N_4		AV16		
4	IO_L45P_4/VREF_4		AU16		
4	IO_L46N_4		AL18		
4	IO_L46P_4		AL17		
4	IO_L47N_4		AM17		
4	IO_L47P_4		AN17		
4	IO_L48N_4		AR17		
4	IO_L48P_4		AP17		
4	IO_L49N_4		AU17		
4	IO_L49P_4		AT17		
4	IO_L50_4/No_Pair		AW16		
4	IO_L53_4/No_Pair		AW17		
4	IO_L54N_4		AN18		
4	IO_L54P_4		AM18		
4	IO_L55N_4		AT18		
4	IO_L55P_4		AR18		
4	IO_L56N_4		AV17		
4	IO_L56P_4		AV18		
4	IO_L57N_4		AY18		
4	IO_L57P_4/VREF_4		AY17		
4	IO_L58N_4		AM19		
4	IO_L58P_4		AL19		
4	IO_L59N_4		AP19		
4	IO_L59P_4		AN19		
4	IO_L60N_4		AT19		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	VCCO_3	AF14	
3	VCCO_3	AE14	
3	VCCO_3	AD14	
3	VCCO_3	AC14	
3	VCCO_3	AB14	
3	VCCO_3	AR10	
3	VCCO_3	AL10	
3	VCCO_3	AN8	
3	VCCO_3	AJ8	
3	VCCO_3	AD8	
3	VCCO_3	AW6	
3	VCCO_3	AU4	
3	VCCO_3	AN4	
3	VCCO_3	AJ4	
3	VCCO_3	AD4	
2	VCCO_2	AA15	
2	VCCO_2	Y15	
2	VCCO_2	W15	
2	VCCO_2	V15	
2	VCCO_2	U15	
2	VCCO_2	T15	
2	VCCO_2	AA14	
2	VCCO_2	Y14	
2	VCCO_2	W14	
2	VCCO_2	V14	
2	VCCO_2	U14	
2	VCCO_2	T14	
2	VCCO_2	R14	
2	VCCO_2	M10	
2	VCCO_2	H10	
2	VCCO_2	W8	
2	VCCO_2	P8	
2	VCCO_2	K8	
2	VCCO_2	D6	
2	VCCO_2	W4	
2	VCCO_2	P4	
2	VCCO_2	K4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	W16	
N/A	VCCINT	V16	
N/A	VCCINT	U16	
N/A	VCCINT	T16	
N/A	VCCINT	R16	
N/A	VCCINT	P16	
N/A	VCCINT	AJ15	
N/A	VCCINT	AH15	
N/A	VCCINT	R15	
N/A	VCCINT	P15	
N/A	VCCINT	AJ14	
N/A	VCCINT	P14	
N/A	VCCINT	AK13	
N/A	VCCINT	N13	
N/A	VCCAUX	BA42	
N/A	VCCAUX	AY42	
N/A	VCCAUX	AL42	
N/A	VCCAUX	AB42	
N/A	VCCAUX	AA42	
N/A	VCCAUX	M42	
N/A	VCCAUX	C42	
N/A	VCCAUX	B42	
N/A	VCCAUX	BB41	
N/A	VCCAUX	A41	
N/A	VCCAUX	BB40	
N/A	VCCAUX	A40	
N/A	VCCAUX	BB31	
N/A	VCCAUX	A31	
N/A	VCCAUX	BB22	
N/A	VCCAUX	A22	
N/A	VCCAUX	BB21	
N/A	VCCAUX	A21	
N/A	VCCAUX	BB12	
N/A	VCCAUX	A12	
N/A	VCCAUX	BB3	
N/A	VCCAUX	A3	
N/A	VCCAUX	BB2	