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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	812
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1148-BBGA, FCBGA
Supplier Device Package	1148-FCPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-6ffg1148c

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

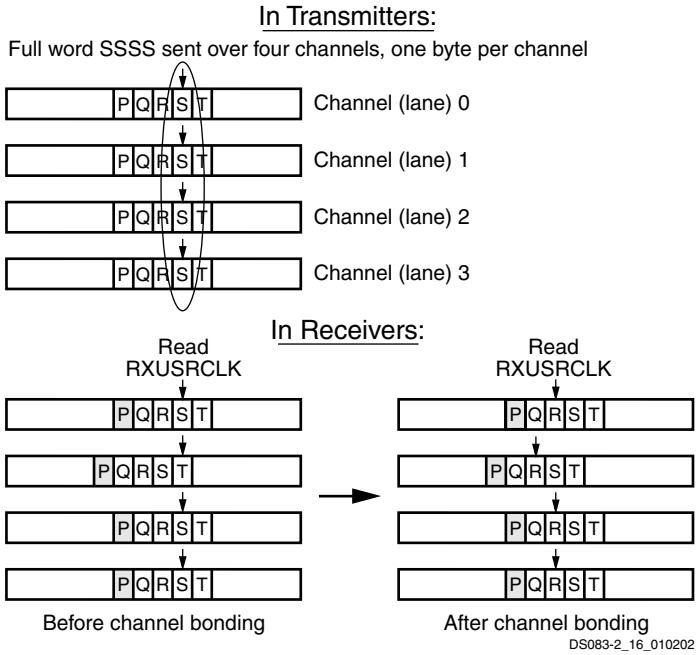


Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

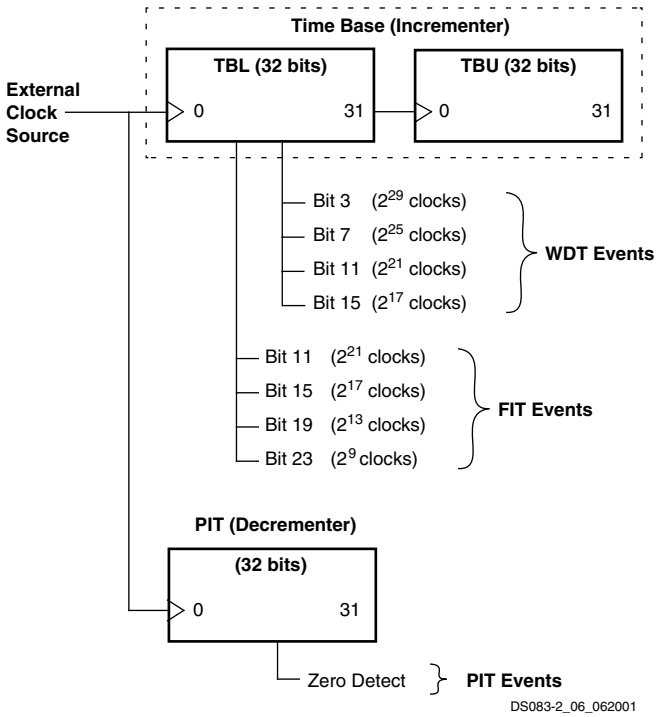


Figure 17: **Relationship of Timer Facilities to Base Clock**

Interrupts

The PPC405 provides an interface to an interrupt controller that is logically outside the PPC405 core. This controller combines the asynchronous interrupt inputs and presents them to the embedded core as a single interrupt signal. The sources of asynchronous interrupts are external signals, the JTAG/debug unit, and any implemented peripherals.

Debug Logic

All architected resources on the embedded PPC405 core can be accessed through the debug logic. Upon a debug event, the PPC405 core provides debug information to an external debug tool. Three different types of tools are supported depending on the debug mode: ROM monitors, JTAG debuggers, and instruction trace tools.

In internal debug mode, a debug event enables exception-handling software at a dedicated interrupt vector to take over the CPU core and communicate with a debug tool. The debug tool has read-write access to all registers and can set hardware or software breakpoints. ROM monitors typically use the internal debug mode.

In external debug mode, the CPU core enters stop state (stops instruction execution) when a debug event occurs. This mode offers a debug tool read-write access to all registers in the PPC405 core. Once the CPU core is in stop state, the debug tool can start the CPU core, step an instruction, freeze the timers, or set hardware or software break points. In addition to CPU core control, the debug logic is capable of writing instructions into the instruction cache, eliminating the need for external memory during initial board bring-up. Communication to a debug tool using external debug mode is through the JTAG port.

Debug wait mode offers the same functionality as external debug mode with one exception. In debug wait mode, the CPU core goes into wait state instead of stop state after a debug event. Wait state is identical to stop state until an interrupt occurs. In wait state, the PPC405 core can vector to an exception handler, service an interrupt and return to wait state. This mode is particularly useful when debugging real time control systems.

Real-time trace debug mode is always enabled. The debug logic continuously broadcasts instruction trace information to the trace port. When a debug event occurs, the debug logic signals an external debug tool to save instruction trace information before and after the event. The number of instructions traced depends on the trace tool.

Debug events signal the debug logic to stop the CPU core, put the CPU core in debug wait state, cause a debug exception or save instruction trace information.

Big Endian and Little Endian Support

The embedded PPC405 core supports big endian or little endian byte ordering for instructions stored in external memory. Since the PowerPC architecture is big endian internally, the ICU rearranges the instructions stored as little endian into the big endian format. Therefore, the instruction cache always contains instructions in big endian format so that the byte ordering is correct for the execution unit. This feature allows the 405 core to be used in systems designed to function in a little endian environment.

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

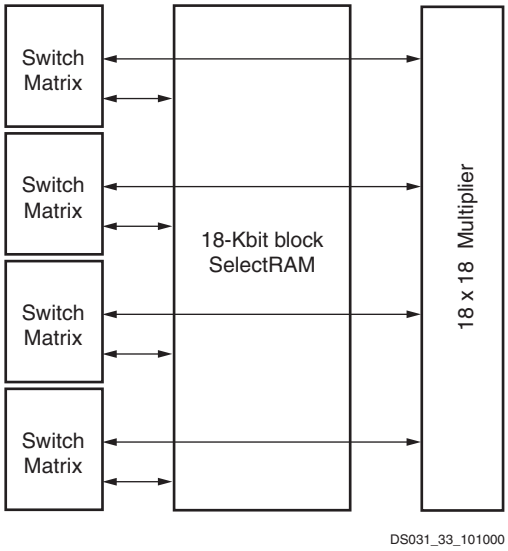


Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

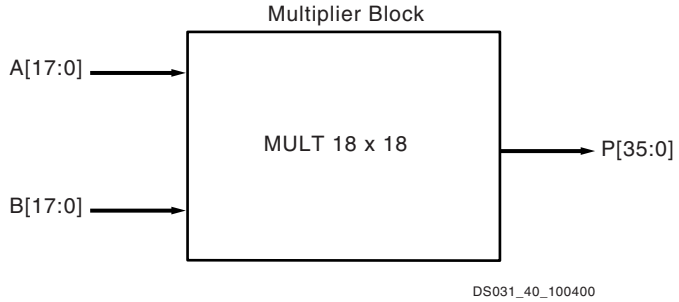


Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

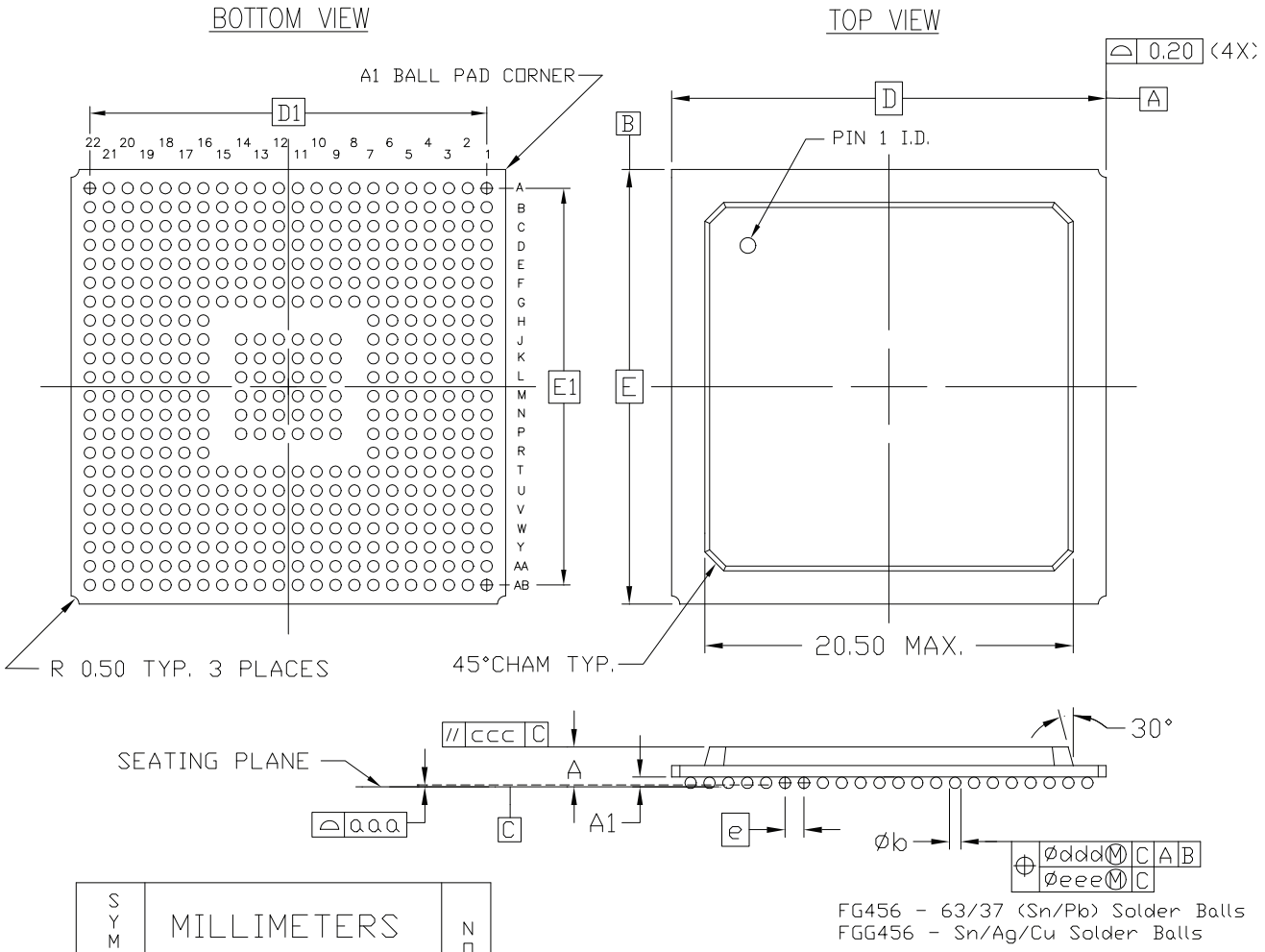
In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.60	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. NOMINAL 'A' DIMENSION IS TYPICALLY 2.20mm.
4. CONFORMS TO JEDEC MS-034-AAJ-1 (DEPOPULATED)

Figure 2: **FG456/FGG456 Fine-Pitch BGA Package Specifications**

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
1	IO_L45N_1/VREF_1	C18			
1	IO_L45P_1	D18			
1	IO_L43N_1	E18			
1	IO_L43P_1	F18			
1	IO_L39N_1	G18			
1	IO_L39P_1	H18			
1	IO_L37N_1	A19			
1	IO_L37P_1	B19			
1	IO_L09N_1/VREF_1	E19			
1	IO_L09P_1	F19			
1	IO_L07N_1	G19			
1	IO_L07P_1	H19			
1	IO_L06N_1	C20			
1	IO_L06P_1	D20			
1	IO_L05_1/No_Pair	E20			
1	IO_L03N_1/VREF_1	F20			
1	IO_L03P_1	G20			
1	IO_L02N_1	D21			
1	IO_L02P_1	E21			
1	IO_L01N_1/VRP_1	D22			
1	IO_L01P_1/VRN_1	E22			
2	IO_L01N_2/VRP_2	C25			
2	IO_L01P_2/VRN_2	C26			
2	IO_L02N_2	D25			
2	IO_L02P_2	D26			
2	IO_L03N_2	E23			
2	IO_L03P_2	F22			
2	IO_L04N_2/VREF_2	E25			
2	IO_L04P_2	E26			
2	IO_L06N_2	F21			
2	IO_L06P_2	G21			
2	IO_L24N_2	F23	NC		
2	IO_L24P_2	F24	NC		
2	IO_L31N_2	F25			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L55P_6	T2			
6	IO_L55N_6	T1			
6	IO_L57P_6	R9			
6	IO_L57N_6/VREF_6	R8			
6	IO_L59P_6	R6			
6	IO_L59N_6	P6			
6	IO_L60P_6	R5			
6	IO_L60N_6	R4			
6	IO_L85P_6	R2			
6	IO_L85N_6	R1			
6	IO_L87P_6	P9			
6	IO_L87N_6/VREF_6	P8			
6	IO_L89P_6	P5			
6	IO_L89N_6	P4			
6	IO_L90P_6	P3			
6	IO_L90N_6	P2			
7	IO_L90P_7	N2			
7	IO_L90N_7	N3			
7	IO_L88P_7	N4			
7	IO_L88N_7/VREF_7	N5			
7	IO_L86P_7	N8			
7	IO_L86N_7	N9			
7	IO_L85P_7	M1			
7	IO_L85N_7	M2			
7	IO_L60P_7	M4			
7	IO_L60N_7	M5			
7	IO_L58P_7	N6			
7	IO_L58N_7/VREF_7	M6			
7	IO_L56P_7	M8			
7	IO_L56N_7	M9			
7	IO_L55P_7	L1			
7	IO_L55N_7	L2			
7	IO_L54P_7	L5			
7	IO_L54N_7	L6			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L05_4/No_Pair	Y8			
4	IO_L06N_4/VRP_4	AB8			
4	IO_L06P_4/VRN_4	AB9			
4	IO_L07N_4	AC8			
4	IO_L07P_4/VREF_4	AD8			
4	IO_L08N_4	AE8			
4	IO_L08P_4	AF8			
4	IO_L09N_4	Y9			
4	IO_L09P_4/VREF_4	AA9			
4	IO_L37N_4	AC9	NC	NC	
4	IO_L37P_4	AD9	NC	NC	
4	IO_L38N_4	Y10	NC	NC	
4	IO_L38P_4	W11	NC	NC	
4	IO_L39N_4	AA10	NC	NC	
4	IO_L39P_4	AA11	NC	NC	
4	IO_L43N_4	AB10	NC	NC	
4	IO_L43P_4	AC10	NC	NC	
4	IO_L44N_4	Y11	NC	NC	
4	IO_L44P_4	Y12	NC	NC	
4	IO_L45N_4	AB11	NC	NC	
4	IO_L45P_4/VREF_4	AC11	NC	NC	
4	IO_L67N_4	AA12			
4	IO_L67P_4	AB12			
4	IO_L68N_4	AC12			
4	IO_L68P_4	AD12			
4	IO_L69N_4	W12			
4	IO_L69P_4/VREF_4	W13			
4	IO_L73N_4	Y13			
4	IO_L73P_4	AA13			
4	IO_L74N_4/GCLK3S	AB13			
4	IO_L74P_4/GCLK2P	AC13			
4	IO_L75N_4/GCLK1S	AD13			
4	IO_L75P_4/GCLK0P	AE13			
5	IO_L75N_5/GCLK7S	AE14			
5	IO_L75P_5/GCLK6P	AD14			
5	IO_L74N_5/GCLK5S	AC14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	M0		AD24			
N/A	M1		AC24			
N/A	M2		AC23			
N/A	TCK		G7			
N/A	TDI		F26			
N/A	TDO		F5			
N/A	TMS		H8			
N/A	PWRDWN_B		AD7			
N/A	HSWAP_EN		H23			
N/A	RSVD		D6			
N/A	VBATT		H7			
N/A	DXP		H24			
N/A	DXN		D25			
N/A	AVCCAUXTX4		B26			
N/A	VTTXPAD4		B27			
N/A	TXNPAD4		A27			
N/A	TXPPAD4		A26			
N/A	GNDA4		C25			
N/A	RXPPAD4		A25			
N/A	RXNPAD4		A24			
N/A	VTRXPAD4		B25			
N/A	AVCCAUXRX4		B24			
N/A	AVCCAUXTX6		B19			
N/A	VTTXPAD6		B20			
N/A	TXNPAD6		A20			
N/A	TXPPAD6		A19			
N/A	GNDA6		C19			
N/A	RXPPAD6		A18			
N/A	RXNPAD6		A17			
N/A	VTRXPAD6		B18			
N/A	AVCCAUXRX6		B17			
N/A	AVCCAUXTX7		B13			
N/A	VTTXPAD7		B14			
N/A	TXNPAD7		A14			
N/A	TXPPAD7		A13			
N/A	GNDA7		C12			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	RXPPAD7		A12			
N/A	RXNPAD7		A11			
N/A	VTRXPAD7		B12			
N/A	AVCCAUXRX7		B11			
N/A	AVCCAUXTX9		B6			
N/A	VTTXPAD9		B7			
N/A	TXNPAD9		A7			
N/A	TXPPAD9		A6			
N/A	GNDA9		C6			
N/A	RXPPAD9		A5			
N/A	RXNPAD9		A4			
N/A	VTRXPAD9		B5			
N/A	AVCCAUXRX9		B4			
N/A	AVCCAUXRX16		AJ4			
N/A	VTRXPAD16		AJ5			
N/A	RXNPAD16		AK4			
N/A	RXPPAD16		AK5			
N/A	GNDA16		AH6			
N/A	TXPPAD16		AK6			
N/A	TXNPAD16		AK7			
N/A	VTTXPAD16		AJ7			
N/A	AVCCAUXTX16		AJ6			
N/A	AVCCAUXRX18		AJ11			
N/A	VTRXPAD18		AJ12			
N/A	RXNPAD18		AK11			
N/A	RXPPAD18		AK12			
N/A	GNDA18		AH12			
N/A	TXPPAD18		AK13			
N/A	TXNPAD18		AK14			
N/A	VTTXPAD18		AJ14			
N/A	AVCCAUXTX18		AJ13			
N/A	AVCCAUXRX19		AJ17			
N/A	VTRXPAD19		AJ18			
N/A	RXNPAD19		AK17			
N/A	RXPPAD19		AK18			
N/A	GNDA19		AH19			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	TXPPAD19		AK19			
N/A	TXNPAD19		AK20			
N/A	VTTXPAD19		AJ20			
N/A	AVCCAUXTX19		AJ19			
N/A	AVCCAUXRX21		AJ24			
N/A	VTRXPAD21		AJ25			
N/A	RXNPAD21		AK24			
N/A	RXPPAD21		AK25			
N/A	GNDA21		AH25			
N/A	TXPPAD21		AK26			
N/A	TXNPAD21		AK27			
N/A	VTTXPAD21		AJ27			
N/A	AVCCAUXTX21		AJ26			
N/A	VCCAUX		AK29			
N/A	VCCAUX		AK16			
N/A	VCCAUX		AK15			
N/A	VCCAUX		AK2			
N/A	VCCAUX		AJ30			
N/A	VCCAUX		AJ1			
N/A	VCCAUX		T30			
N/A	VCCAUX		T1			
N/A	VCCAUX		R30			
N/A	VCCAUX		R1			
N/A	VCCAUX		B30			
N/A	VCCAUX		B1			
N/A	VCCAUX		A29			
N/A	VCCAUX		A16			
N/A	VCCAUX		A15			
N/A	VCCAUX		A2			
N/A	VCCINT		Y19			
N/A	VCCINT		Y18			
N/A	VCCINT		Y17			
N/A	VCCINT		Y16			
N/A	VCCINT		Y15			
N/A	VCCINT		Y14			

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L87N_6/VREF_6	V33		
6	IO_L88P_6	V30		
6	IO_L88N_6	V31		
6	IO_L89P_6	V24		
6	IO_L89N_6	V25		
6	IO_L90P_6	V28		
6	IO_L90N_6	V29		
7	IO_L90P_7	U32		
7	IO_L90N_7	V32		
7	IO_L89P_7	U28		
7	IO_L89N_7	U29		
7	IO_L88P_7	U30		
7	IO_L88N_7/VREF_7	U31		
7	IO_L87P_7	T33		
7	IO_L87N_7	U33		
7	IO_L86P_7	U26		
7	IO_L86N_7	U27		
7	IO_L85P_7	T31		
7	IO_L85N_7	T32		
7	IO_L60P_7	R33		
7	IO_L60N_7	R34		
7	IO_L59P_7	U24		
7	IO_L59N_7	U25		
7	IO_L58P_7	R29		
7	IO_L58N_7/VREF_7	R30		
7	IO_L57P_7	P33		
7	IO_L57N_7	P34		
7	IO_L56P_7	T28		
7	IO_L56N_7	T29		
7	IO_L55P_7	P32		
7	IO_L55N_7	R32		
7	IO_L54P_7	P29		
7	IO_L54N_7	P30		
7	IO_L53P_7	T24		
7	IO_L53N_7	T25		
7	IO_L52P_7	N32		
7	IO_L52N_7/VREF_7	N33		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L59P_0	N21		
0	IO_L60N_0	E23		
0	IO_L60P_0	F22		
0	IO_L64N_0	D22		
0	IO_L64P_0	E22		
0	IO_L65N_0	H21		
0	IO_L65P_0	H20		
0	IO_L66N_0	G22		
0	IO_L66P_0/VREF_0	G21		
0	IO_L67N_0	D21		
0	IO_L67P_0	E21		
0	IO_L68N_0	J21		
0	IO_L68P_0	K21		
0	IO_L69N_0	C22		
0	IO_L69P_0/VREF_0	C21		
0	IO_L73N_0	F21		
0	IO_L73P_0	F20		
0	IO_L74N_0/GCLK7P	L21		
0	IO_L74P_0/GCLK6S	M21		
0	IO_L75N_0/GCLK5P	D20		
0	IO_L75P_0/GCLK4S	E20		
1	IO_L75N_1/GCLK3P	K20		
1	IO_L75P_1/GCLK2S	J20		
1	IO_L74N_1/GCLK1P	N20		
1	IO_L74P_1/GCLK0S	M20		
1	IO_L73N_1	E19		
1	IO_L73P_1	D19		
1	IO_L69N_1/VREF_1	G19		
1	IO_L69P_1	F19		
1	IO_L68N_1	L19		
1	IO_L68P_1	K19		
1	IO_L67N_1	J19		
1	IO_L67P_1	H19		
1	IO_L66N_1/VREF_1	C19		
1	IO_L66P_1	C18		
1	IO_L65N_1	N19		
1	IO_L65P_1	M19		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GNDA18	AU16		
N/A	TXPPAD18	AW18		
N/A	TXNPAD18	AW19		
N/A	VTTXPAD18	AV19		
N/A	AVCCAUXTX18	AV18		
N/A	AVCCAUXRX19	AV21		
N/A	VTRXPAD19	AV22		
N/A	RXNPAD19	AW21		
N/A	RXPPAD19	AW22		
N/A	GNDA19	AU24		
N/A	TXPPAD19	AW23		
N/A	TXNPAD19	AW24		
N/A	VTTXPAD19	AV24		
N/A	AVCCAUXTX19	AV23		
N/A	AVCCAUXRX20	AV25		
N/A	VTRXPAD20	AV26		
N/A	RXNPAD20	AW25		
N/A	RXPPAD20	AW26		
N/A	GNDA20	AU27		
N/A	TXPPAD20	AW27		
N/A	TXNPAD20	AW28		
N/A	VTTXPAD20	AV28		
N/A	AVCCAUXTX20	AV27		
N/A	AVCCAUXRX21	AV29		
N/A	VTRXPAD21	AV30		
N/A	RXNPAD21	AW29		
N/A	RXPPAD21	AW30		
N/A	GNDA21	AU31		
N/A	TXPPAD21	AW31		
N/A	TXNPAD21	AW32		
N/A	VTTXPAD21	AV32		
N/A	AVCCAUXTX21	AV31		
N/A	AVCCAUXRX23	AV33		
N/A	VTRXPAD23	AV34		
N/A	RXNPAD23	AW33		
N/A	RXPPAD23	AW34		
N/A	GNDA23	AU34		
N/A	TXPPAD23	AW35		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L44P_2		U10		
2	IO_L45N_2		U3		
2	IO_L45P_2		U4		
2	IO_L46N_2/VREF_2		U1		
2	IO_L46P_2		U2		
2	IO_L47N_2		T12		
2	IO_L47P_2		U12		
2	IO_L48N_2		V10		
2	IO_L48P_2		V11		
2	IO_L49N_2		V7		
2	IO_L49P_2		V8		
2	IO_L50N_2		U11		
2	IO_L50P_2		V12		
2	IO_L51N_2		V4		
2	IO_L51P_2		V5		
2	IO_L52N_2/VREF_2		V1		
2	IO_L52P_2		V2		
2	IO_L53N_2		W9		
2	IO_L53P_2		W10		
2	IO_L54N_2		W7		
2	IO_L54P_2		W8		
2	IO_L55N_2		W5		
2	IO_L55P_2		W6		
2	IO_L56N_2		W11		
2	IO_L56P_2		W12		
2	IO_L57N_2		W3		
2	IO_L57P_2		W4		
2	IO_L58N_2/VREF_2		W1		
2	IO_L58P_2		W2		
2	IO_L59N_2		Y9		
2	IO_L59P_2		Y10		
2	IO_L60N_2		Y6		
2	IO_L60P_2		Y7		
2	IO_L85N_2		Y3		
2	IO_L85P_2		Y4		
2	IO_L86N_2		Y11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L21P_1	H13	
1	IO_L20N_1	L12	
1	IO_L20P_1	K12	
1	IO_L19N_1	B11	
1	IO_L19P_1	A11	
1	IO_L09N_1/VREF_1	E11	
1	IO_L09P_1	D11	
1	IO_L08N_1	J11	
1	IO_L08P_1	H11	
1	IO_L07N_1	G11	
1	IO_L07P_1	F11	
1	IO_L06N_1	B10	
1	IO_L06P_1	A10	
1	IO_L05_1/No_Pair	G10	
1	IO_L03N_1/VREF_1	C10	
1	IO_L03P_1	C11	
1	IO_L02N_1	L11	
1	IO_L02P_1	K11	
1	IO_L01N_1/VRP_1	F10	
1	IO_L01P_1/VRN_1	E10	
2	IO_L01N_2/VRP_2	B8	
2	IO_L01P_2/VRN_2	A8	
2	IO_L02N_2	C9	
2	IO_L02P_2	B9	
2	IO_L03N_2	B7	
2	IO_L03P_2	A7	
2	IO_L04N_2/VREF_2	B6	
2	IO_L04P_2	A6	
2	IO_L05N_2	D8	
2	IO_L05P_2	D9	
2	IO_L06N_2	B4	
2	IO_L06P_2	A4	
2	IO_L73N_2	C7	
2	IO_L73P_2	C8	
2	IO_L74N_2	G9	
2	IO_L74P_2	F9	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L69P_2	F6	
2	IO_L70N_2/VREF_2	G5	
2	IO_L70P_2	F5	
2	IO_L71N_2	P10	
2	IO_L71P_2	P11	
2	IO_L72N_2	G3	
2	IO_L72P_2	G4	
2	IO_L07N_2	G1	
2	IO_L07P_2	G2	
2	IO_L08N_2	N8	
2	IO_L08P_2	P9	
2	IO_L09N_2	H6	
2	IO_L09P_2	H7	
2	IO_L10N_2/VREF_2	H4	
2	IO_L10P_2	H5	
2	IO_L11N_2	R12	
2	IO_L11P_2	T12	
2	IO_L12N_2	H2	
2	IO_L12P_2	H3	
2	IO_L13N_2	J6	
2	IO_L13P_2	J7	
2	IO_L14N_2	R10	
2	IO_L14P_2	R11	
2	IO_L15N_2	J3	
2	IO_L15P_2	J4	
2	IO_L16N_2/VREF_2	J2	
2	IO_L16P_2	H1	
2	IO_L17N_2	R8	
2	IO_L17P_2	R9	
2	IO_L18N_2	K5	
2	IO_L18P_2	K6	
2	IO_L19N_2	K1	
2	IO_L19P_2	K2	
2	IO_L20N_2	T10	
2	IO_L20P_2	T11	
2	IO_L21N_2	L7	
2	IO_L21P_2	K7	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
08/14/02	2.0	Added package and pinout information for new devices.
08/27/02	2.1	• Updated SelectIO-Ultra information in Table 4. (Table deleted in v2.3.) • Corrected direction for RXNPAD and TXPPAD in Table 4 (formerly Table 5).
09/27/02	2.2	Corrected Table 2 and Table 3 entries for XC2VP30, FF1152 package, maximum I/Os from 692 to 644.
11/20/02	2.3	Added Number of Differential Pairs data to Table 3. Removed former Table 4.
12/03/02	2.4	Corrections in Table 4: • Reclassified GCLKx (S/P) pins as Input/Output, since these pins can be used as normal I/Os if not used as clocks. • Added cautionary note to PWRDWN_B pin, indicating that this function is not supported.
01/20/03	2.5	Added and removed package/pinout information for existing devices: • In Table 1, added FG676 package information. • In Table 3, added FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • In Table 12, removed FF1517 package option for XC2VP40. • Added FG676 package pinouts (Table 7) for XC2VP20, XC2VP30, and XC2VP40. • Added package diagram (Figure 3) for FG676 package.
05/19/03	2.5.1	• Added section **BREFCLK Pin Definitions**, page 5. • Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	2.5.3	• Added notation of "open-drain" to TDO pin in Table 4. • The final GND pin in each of six pinout tables was inadvertently deleted in v2.5.1. This revision restores the deleted GND pins as follows: - Pin A1, Table 6, page 16 (FG456) - Pin AF26, Table 7, page 30 (FG676) - Pin AN34, Table 10, page 98 (FF1152) - Pin E1, Table 11, page 130 (FF1148) - Pin C38, Table 12, page 162 (FF1517) - Pin E1, Table 14, page 253 (FF1696)
08/25/03	2.5.5	• Table 4: Deleted Note 2, obsolete. There is only one GNDA pin per MGT. • Table 4: Deleted pins ALT_VRP and ALT_VRN. Not used in Virtex-II Pro FPGAs.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 4, signal descriptions column: - For signals TDI, TMS, and TCK, added: Pins are 3.3V-compatible. - For signals M2, M1, M0, added: Tie to 3.3V only with 100Ω series resistor. No toggling during or after configuration. - For signal TDO, added: No internal pull-up. External pull-up to 3.3V OK with resistor greater than 200Ω.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-4 (Module 4 of Virtex-II Pro X data sheet). Added data on available Pb-free packages and updated package diagrams for affected devices.