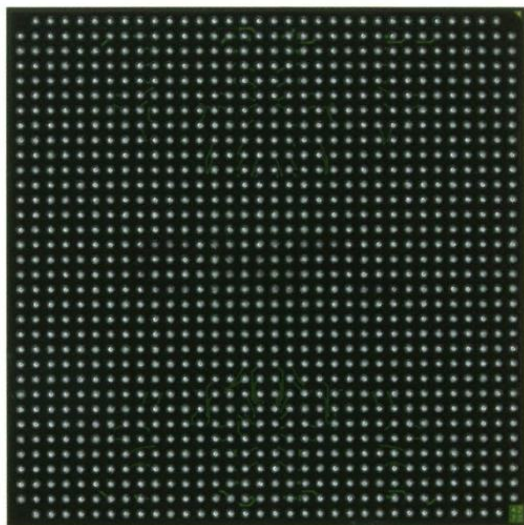




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Details

Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-6ffg1152c

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Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)



Figure 34: Virtex-II Pro Slice (Top Half)

Figure 57 shows clock distribution in Virtex-II Pro devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). To reduce power consumption, any unused clock branches remain static.

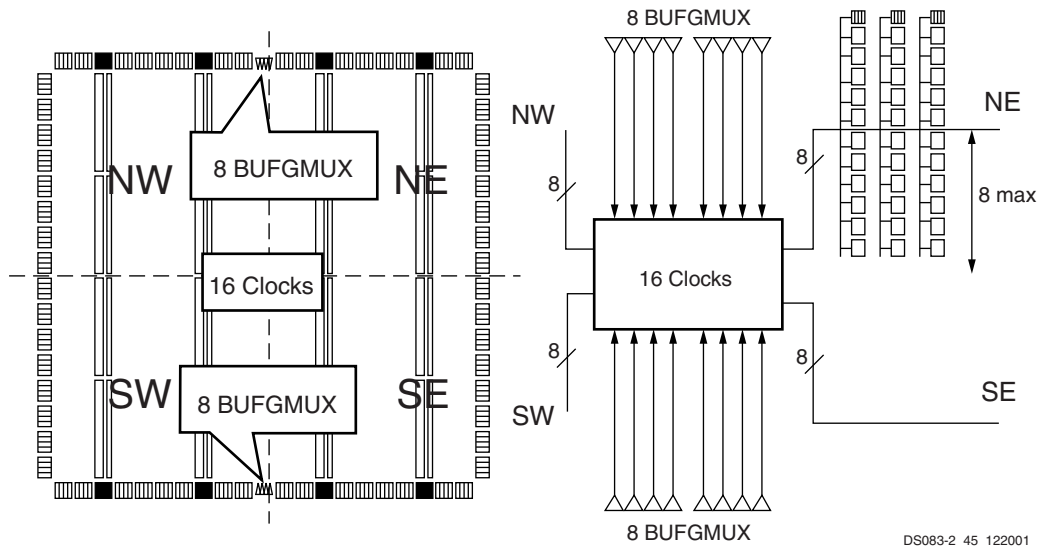


Figure 57: Virtex-II Pro Clock Distribution

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 58.

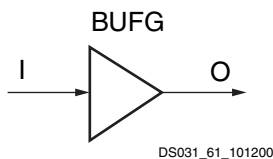


Figure 58: Virtex-II Pro BUFG Function

The Virtex-II Pro global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 59), as well as a two-input clock multiplexer (Figure 60). A functional description of these two options is provided below. Each of them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE and S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

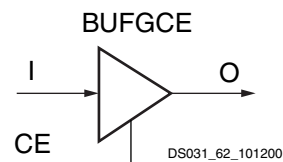


Figure 59: Virtex-II Pro BUFGCE Function

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I₀ input, a High on S selects the I₁ input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect.

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
N/A	AVCCAUXRX7	B13
N/A	AVCCAUXRX18	R13
N/A	VTRXPAD18	R12
N/A	RXNPAD18	T13
N/A	RXPPAD18	T12
N/A	GNDA18	P11
N/A	TXPPAD18	T11
N/A	TXNPAD18	T10
N/A	VTTXPAD18	R10
N/A	AVCCAUXTX18	R11
N/A	AVCCAUXRX19	R7
N/A	VTRXPAD19	R6
N/A	RXNPAD19	T7
N/A	RXPPAD19	T6
N/A	GNDA19	P6
N/A	TXPPAD19	T5
N/A	TXNPAD19	T4
N/A	VTTXPAD19	R4
N/A	AVCCAUXTX19	R5
N/A	VCCINT	N4
N/A	VCCINT	N13
N/A	VCCINT	M5
N/A	VCCINT	M12
N/A	VCCINT	E5
N/A	VCCINT	E12
N/A	VCCINT	D4
N/A	VCCINT	D13
N/A	VCCAUX	R16
N/A	VCCAUX	R1
N/A	VCCAUX	B16
N/A	VCCAUX	B1
N/A	GND	T16
N/A	GND	T1
N/A	GND	R2

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
N/A	GND	R15
N/A	GND	L6
N/A	GND	L11
N/A	GND	K9
N/A	GND	K8
N/A	GND	K7
N/A	GND	K10
N/A	GND	J9
N/A	GND	J8
N/A	GND	J7
N/A	GND	J10
N/A	GND	H9
N/A	GND	H8
N/A	GND	H7
N/A	GND	H10
N/A	GND	G9
N/A	GND	G8
N/A	GND	G7
N/A	GND	G10
N/A	GND	F6
N/A	GND	F11
N/A	GND	B2
N/A	GND	B15
N/A	GND	A16
N/A	GND	A1

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)

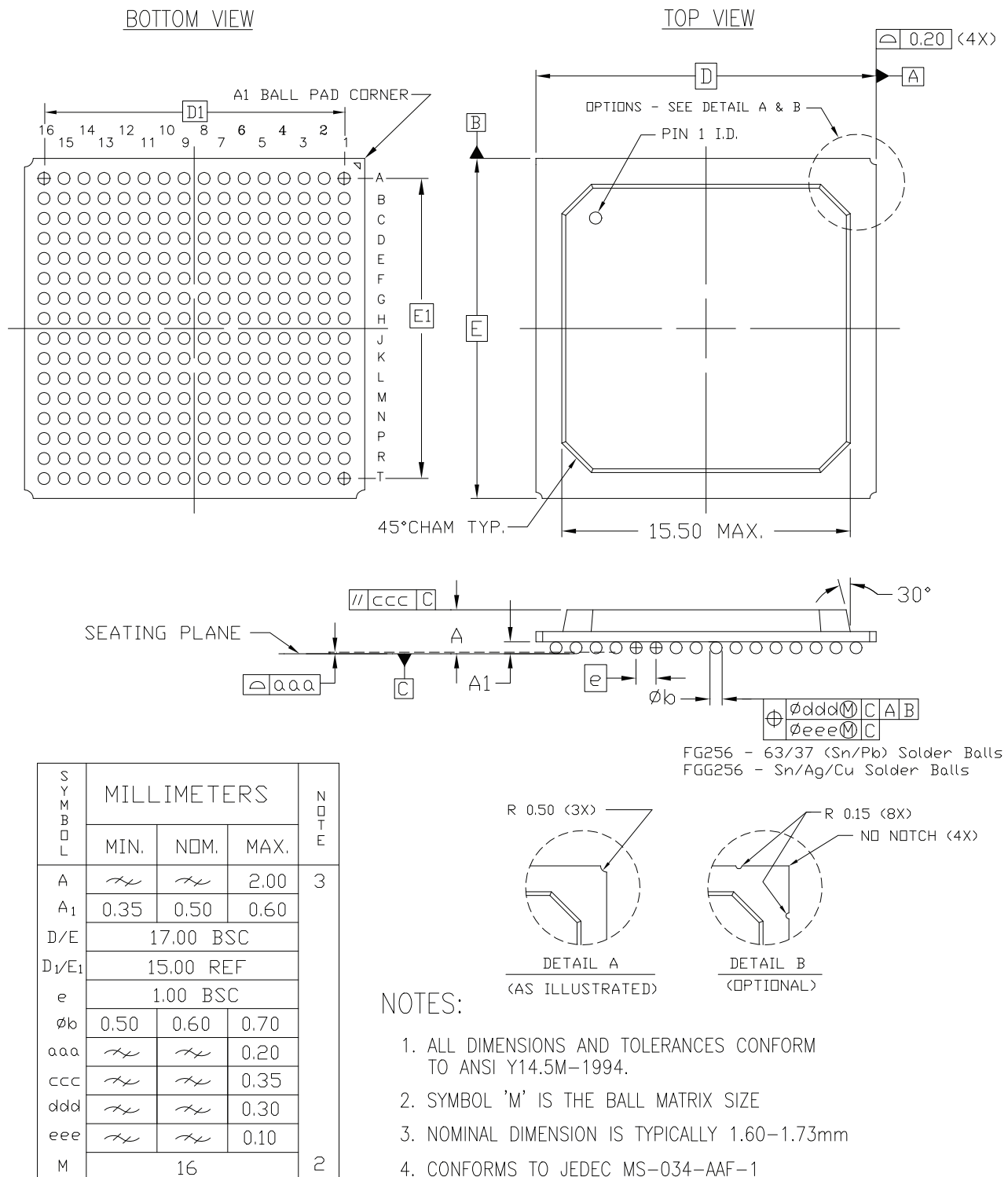


Figure 1: FG256/FGG256 Fine-Pitch BGA Package Specifications

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

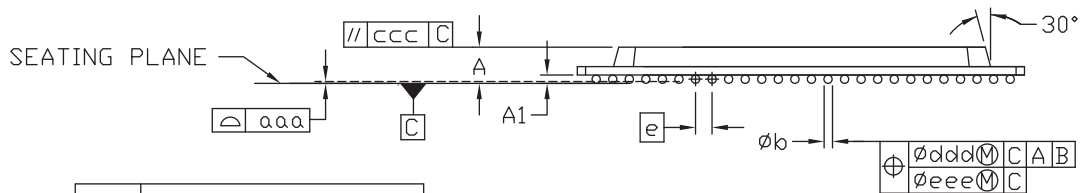
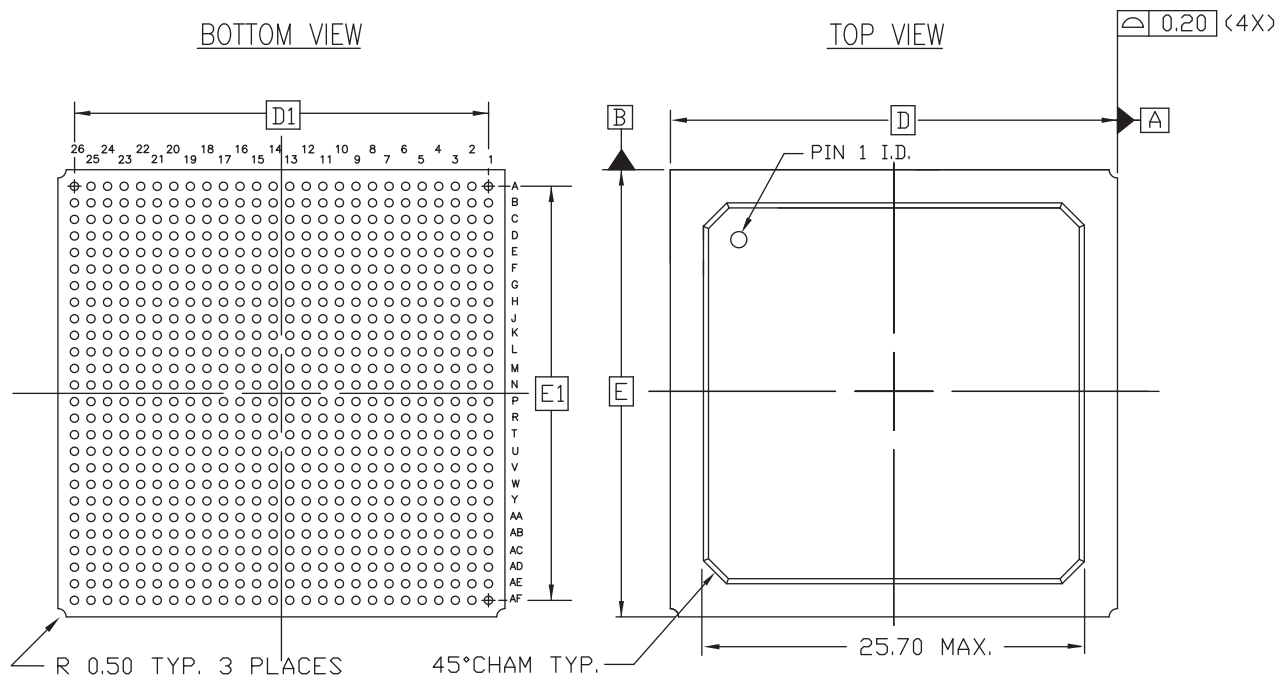
Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A ₁	0.40	0.50	0.60
D/E	27.00 BSC		
D ₁ /E ₁	25.00 REF		
e	1.00 BSC		
ϕb	0.50	0.60	0.70
aaa	$\sim$	$\sim$	0.20
ccc	$\sim$	$\sim$	0.35
ddd	$\sim$	$\sim$	0.30
eee	$\sim$	$\sim$	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: FG676/FGG676 Fine-Pitch BGA Package Specifications

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L39P_3	AD4				
3	IO_L38N_3	AB9				
3	IO_L38P_3	AB10				
3	IO_L37N_3	AD5				
3	IO_L37P_3	AD6				
3	IO_L36N_3	AE2				
3	IO_L36P_3	AF2				
3	IO_L35N_3	AD7				
3	IO_L35P_3	AD8				
3	IO_L34N_3	AE4				
3	IO_L34P_3	AE5				
3	IO_L33N_3/VREF_3	AG1				
3	IO_L33P_3	AG2				
3	IO_L32N_3	AC9				
3	IO_L32P_3	AC10				
3	IO_L31N_3	AF3				
3	IO_L31P_3	AF4				
3	IO_L24N_3	AH1	NC			
3	IO_L24P_3	AH2	NC			
3	IO_L23N_3	AE7	NC			
3	IO_L23P_3	AE8	NC			
3	IO_L22N_3	AF5	NC			
3	IO_L22P_3	AF6	NC			
3	IO_L21N_3/VREF_3	AG3	NC			
3	IO_L21P_3	AG4	NC			
3	IO_L20N_3	AD9	NC			
3	IO_L20P_3	AD10	NC			
3	IO_L19N_3	AH3	NC			
3	IO_L19P_3	AH4	NC			
3	IO_L18N_3	AJ1	NC			
3	IO_L18P_3	AJ2	NC			
3	IO_L17N_3	AF7	NC			
3	IO_L17P_3	AF8	NC			
3	IO_L16N_3	AK1	NC			
3	IO_L16P_3	AK2	NC			
3	IO_L15N_3/VREF_3	AG5	NC			
3	IO_L15P_3	AG6	NC			
3	IO_L06N_3	AL1				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AG8				
N/A	GND	AG12				
N/A	GND	AG15				
N/A	GND	AG20				
N/A	GND	AG23				
N/A	GND	AG27				
N/A	GND	J34				
N/A	GND	AH7				
N/A	GND	AH28				
N/A	GND	AJ6				
N/A	GND	AJ29				
N/A	GND	AK5				
N/A	GND	AK12				
N/A	GND	AK23				
N/A	GND	AK30				
N/A	GND	AL4				
N/A	GND	AL31				
N/A	GND	AM1				
N/A	GND	AM2				
N/A	GND	AM10				
N/A	GND	AM16				
N/A	GND	AM19				
N/A	GND	AM25				
N/A	GND	AM33				
N/A	GND	AM34				
N/A	GND	AN1				
N/A	GND	AN34				

Notes:

1. See [Table 4](#) for an explanation of the signals available on this pin.

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L40P_2	K3		
2	IO_L41N_2	R9		
2	IO_L41P_2	P9		
2	IO_L42N_2	K1		
2	IO_L42P_2	K2		
2	IO_L43N_2	L5		
2	IO_L43P_2	L6		
2	IO_L44N_2	P7		
2	IO_L44P_2	P8		
2	IO_L45N_2	L1		
2	IO_L45P_2	L2		
2	IO_L46N_2/VREF_2	M5		
2	IO_L46P_2	M6		
2	IO_L47N_2	R10		
2	IO_L47P_2	R11		
2	IO_L48N_2	M3		
2	IO_L48P_2	M4		
2	IO_L49N_2	M1		
2	IO_L49P_2	M2		
2	IO_L50N_2	R7		
2	IO_L50P_2	T8		
2	IO_L51N_2	P4		
2	IO_L51P_2	N4		
2	IO_L52N_2/VREF_2	N2		
2	IO_L52P_2	N3		
2	IO_L53N_2	T10		
2	IO_L53P_2	T11		
2	IO_L54N_2	P5		
2	IO_L54P_2	P6		
2	IO_L55N_2	R3		
2	IO_L55P_2	P3		
2	IO_L56N_2	T6		
2	IO_L56P_2	T7		
2	IO_L57N_2	P1		
2	IO_L57P_2	P2		
2	IO_L58N_2/VREF_2	R5		
2	IO_L58P_2	R6		
2	IO_L59N_2	U10		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L27P_5	AL23		
5	IO_L26N_5	AD22		
5	IO_L26P_5	AE22		
5	IO_L25N_5	AJ23		
5	IO_L25P_5	AK23		
5	IO_L21N_5	AN24		
5	IO_L21P_5	AP24		
5	IO_L20N_5	AE23		
5	IO_L20P_5	AF23		
5	IO_L19N_5	AM23		
5	IO_L19P_5	AM24		
5	IO_L09N_5/VREF_5	AJ24		
5	IO_L09P_5	AK24		
5	IO_L08N_5	AG22		
5	IO_L08P_5	AG23		
5	IO_L07N_5/VREF_5	AH23		
5	IO_L07P_5	AH24		
5	IO_L06N_5/VRP_5	AN25		
5	IO_L06P_5/VRN_5	AP25		
5	IO_L05_5/No_Pair	AH25		
5	IO_L03N_5/D4	AL25		
5	IO_L03P_5/D5	AM25		
5	IO_L02N_5/D6	AE24		
5	IO_L02P_5/D7	AF24		
5	IO_L01N_5/RDWR_B	AJ25		
5	IO_L01P_5/CS_B	AK25		
6	IO_L01P_6/VRN_6	AP32		
6	IO_L01N_6/VRP_6	AN32		
6	IO_L02P_6	AP28		
6	IO_L02N_6	AN28		
6	IO_L03P_6	AP31		
6	IO_L03N_6/VREF_6	AN31		
6	IO_L04P_6	AP29		
6	IO_L04N_6	AN29		
6	IO_L05P_6	AN26		
6	IO_L05N_6	AN27		
6	IO_L06P_6	AM33		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	VCCO_7	U23		
7	VCCO_7	T23		
7	VCCO_7	R23		
7	VCCO_7	P23		
7	VCCO_7	N23		
6	VCCO_6	AK33		
6	VCCO_6	AM31		
6	VCCO_6	AH31		
6	VCCO_6	AD31		
6	VCCO_6	Y31		
6	VCCO_6	AM27		
6	VCCO_6	AH27		
6	VCCO_6	AD27		
6	VCCO_6	Y27		
6	VCCO_6	AF26		
6	VCCO_6	AC24		
6	VCCO_6	AB23		
6	VCCO_6	AA23		
6	VCCO_6	Y23		
6	VCCO_6	W23		
6	VCCO_6	V23		
5	VCCO_5	AL24		
5	VCCO_5	AG24		
5	VCCO_5	AD23		
5	VCCO_5	AC22		
5	VCCO_5	AC21		
5	VCCO_5	AL20		
5	VCCO_5	AG20		
5	VCCO_5	AC20		
5	VCCO_5	AC19		
5	VCCO_5	AC18		
4	VCCO_4	AC17		
4	VCCO_4	AC16		
4	VCCO_4	AL15		
4	VCCO_4	AG15		
4	VCCO_4	AC15		
4	VCCO_4	AC14		
4	VCCO_4	AC13		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	VCCO_1	H15		
1	VCCO_1	D15		
1	VCCO_1	M14		
1	VCCO_1	M13		
1	VCCO_1	L12		
1	VCCO_1	H11		
1	VCCO_1	D11		
0	VCCO_0	H24		
0	VCCO_0	D24		
0	VCCO_0	L23		
0	VCCO_0	M22		
0	VCCO_0	M21		
0	VCCO_0	M20		
0	VCCO_0	H20		
0	VCCO_0	D20		
0	VCCO_0	M19		
0	VCCO_0	M18		
N/A	CCLK	AG9		
N/A	PROG_B	G26		
N/A	DONE	AF10		
N/A	M0	AG25		
N/A	M1	AG26		
N/A	M2	AF25		
N/A	TCK	G9		
N/A	TDI	F26		
N/A	TDO	F9		
N/A	TMS	H10		
N/A	PWRDWN_B	AG10		
N/A	HSWAP_EN	H25		
N/A	RSVD	H9		
N/A	VBATT	J10		
N/A	DXP	J25		
N/A	DXN	H26		
N/A	VCCINT	AD24		
N/A	VCCINT	L24		
N/A	VCCINT	AC23		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L09P_3	AM3		
3	IO_L08N_3	AK8		
3	IO_L08P_3	AK9		
3	IO_L07N_3	AN6		
3	IO_L07P_3	AN7		
3	IO_L84N_3	AN3	NC	
3	IO_L84P_3	AN4	NC	
3	IO_L82N_3	AN1	NC	
3	IO_L82P_3	AN2	NC	
3	IO_L81N_3/VREF_3	AN5	NC	
3	IO_L81P_3	AP5	NC	
3	IO_L79N_3	AP3	NC	
3	IO_L79P_3	AP4	NC	
3	IO_L78N_3	AP1	NC	
3	IO_L78P_3	AP2	NC	
3	IO_L76N_3	AR2	NC	
3	IO_L76P_3	AR3	NC	
3	IO_L75N_3/VREF_3	AT1	NC	
3	IO_L75P_3	AT2	NC	
3	IO_L73N_3	AT5	NC	
3	IO_L73P_3	AU5	NC	
3	IO_L06N_3	AR6		
3	IO_L06P_3	AT6		
3	IO_L05N_3	AL9		
3	IO_L05P_3	AM8		
3	IO_L04N_3	AP7		
3	IO_L04P_3	AR7		
3	IO_L03N_3/VREF_3	AM9		
3	IO_L03P_3	AN9		
3	IO_L02N_3	AR8		
3	IO_L02P_3	AT8		
3	IO_L01N_3/VRP_3	AT7		
3	IO_L01P_3/VRN_3	AU7		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AT9		
4	IO_L01P_4/INIT_B	AR9		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AK11		
4	IO_L02P_4/D1	AK12		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	AU3		
N/A	GND	AT3		
N/A	GND	D3		
N/A	GND	C3		
N/A	GND	B3		
N/A	GND	AN12		
N/A	GND	G12		
N/A	GND	C12		
N/A	GND	Y10		
N/A	GND	AH9		
N/A	GND	AD9		
N/A	GND	T9		
N/A	GND	M9		
N/A	GND	AU8		
N/A	GND	AN8		
N/A	GND	G8		
N/A	GND	C8		
N/A	GND	Y6		
N/A	GND	AM5		
N/A	GND	AH5		
N/A	GND	T17		
N/A	GND	AT16		
N/A	GND	AN16		
N/A	GND	AJ16		
N/A	GND	AC16		
N/A	GND	AB16		
N/A	GND	AA16		
N/A	GND	Y16		
N/A	GND	W16		
N/A	GND	V16		
N/A	GND	U16		
N/A	GND	L16		
N/A	GND	G16		
N/A	GND	D16		
N/A	GND	AU12		
N/A	GND	AB18		
N/A	GND	AA18		
N/A	GND	Y18		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L77N_3		AT3		
3	IO_L77P_3		AT4		
3	IO_L76N_3		AU1		
3	IO_L76P_3		AU2		
3	IO_L75N_3/VREF_3		AU3		
3	IO_L75P_3		AU4		
3	IO_L74N_3		AV3		
3	IO_L74P_3		AW3		
3	IO_L73N_3		AV1		
3	IO_L73P_3		AV2		
3	IO_L06N_3		AW1		
3	IO_L06P_3		AW2		
3	IO_L05N_3		AT8		
3	IO_L05P_3		AU8		
3	IO_L04N_3		AT6		
3	IO_L04P_3		AU7		
3	IO_L03N_3/VREF_3		AY5		
3	IO_L03P_3		AY6		
3	IO_L02N_3		AV7		
3	IO_L02P_3		AW7		
3	IO_L01N_3/VRP_3		AV6		
3	IO_L01P_3/VRN_3		AW6		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾		AT9		
4	IO_L01P_4/INIT_B		AR9		
4	IO_L02N_4/D0/DIN ⁽¹⁾		AU9		
4	IO_L02P_4/D1		AV9		
4	IO_L03N_4/D2		AY9		
4	IO_L03P_4/D3		AW9		
4	IO_L05_4/No_Pair		AN11		
4	IO_L06N_4/VRP_4		AR10		
4	IO_L06P_4/VRN_4		AP10		
4	IO_L07N_4		AU10		
4	IO_L07P_4/VREF_4		AT10		
4	IO_L08N_4		AV10		
4	IO_L08P_4		AW10		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L52N_6		AE42		
6	IO_L53P_6		AE32		
6	IO_L53N_6		AE33		
6	IO_L54P_6		AD35		
6	IO_L54N_6		AD36		
6	IO_L55P_6		AD37		
6	IO_L55N_6		AD38		
6	IO_L56P_6		AD31		
6	IO_L56N_6		AD32		
6	IO_L57P_6		AD39		
6	IO_L57N_6/VREF_6		AD40		
6	IO_L58P_6		AD41		
6	IO_L58N_6		AD42		
6	IO_L59P_6		AD33		
6	IO_L59N_6		AD34		
6	IO_L60P_6		AC33		
6	IO_L60N_6		AC34		
6	IO_L85P_6		AC36		
6	IO_L85N_6		AC37		
6	IO_L86P_6		AC31		
6	IO_L86N_6		AC32		
6	IO_L87P_6		AC39		
6	IO_L87N_6/VREF_6		AC40		
6	IO_L88P_6		AB33		
6	IO_L88N_6		AB34		
6	IO_L89P_6		AB36		
6	IO_L89N_6		AB37		
6	IO_L90P_6		AB39		
6	IO_L90N_6		AB40		
7	IO_L90P_7		AA39		
7	IO_L90N_7		AA40		
7	IO_L89P_7		AB31		
7	IO_L89N_7		AA31		
7	IO_L88P_7		AA36		
7	IO_L88N_7/VREF_7		AA37		

FF1696 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 14](#), XC2VP100 Virtex-II Pro devices are available in the FF1696 flip-chip fine-pitch BGA package. Following this table are the **FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L01N_0/VRP_0	E33	
0	IO_L01P_0/VRN_0	F33	
0	IO_L02N_0	K32	
0	IO_L02P_0	L32	
0	IO_L03N_0	C32	
0	IO_L03P_0/VREF_0	C33	
0	IO_L05_0/No_Pair	G33	
0	IO_L06N_0	A33	
0	IO_L06P_0	B33	
0	IO_L07N_0	F32	
0	IO_L07P_0	G32	
0	IO_L08N_0	H32	
0	IO_L08P_0	J32	
0	IO_L09N_0	D32	
0	IO_L09P_0/VREF_0	E32	
0	IO_L19N_0	A32	
0	IO_L19P_0	B32	
0	IO_L20N_0	K31	
0	IO_L20P_0	L31	
0	IO_L21N_0	H30	
0	IO_L21P_0	G31	
0	IO_L25N_0	E31	
0	IO_L25P_0	F31	
0	IO_L26N_0	H31	
0	IO_L26P_0	J31	
0	IO_L27N_0	D30	
0	IO_L27P_0/VREF_0	D31	
0	IO_L28N_0	B31	
0	IO_L28P_0	C31	
0	IO_L29N_0	K30	
0	IO_L29P_0	L30	
0	IO_L30N_0	F30	
0	IO_L30P_0	G30	
0	IO_L34N_0	B30	