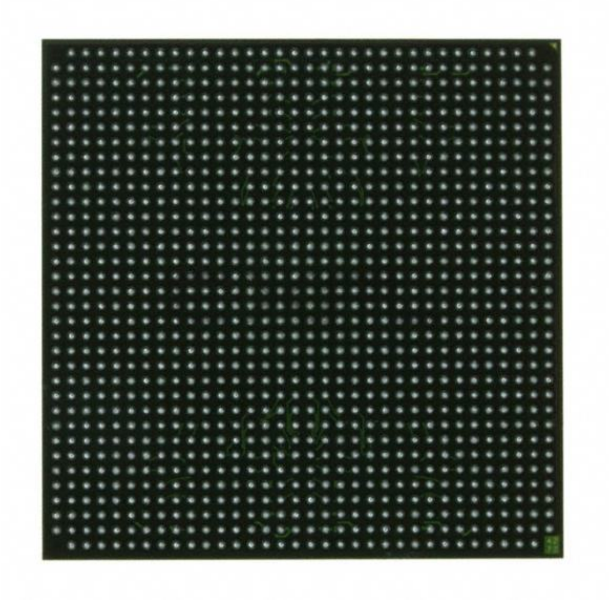


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-6ffg1152i

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

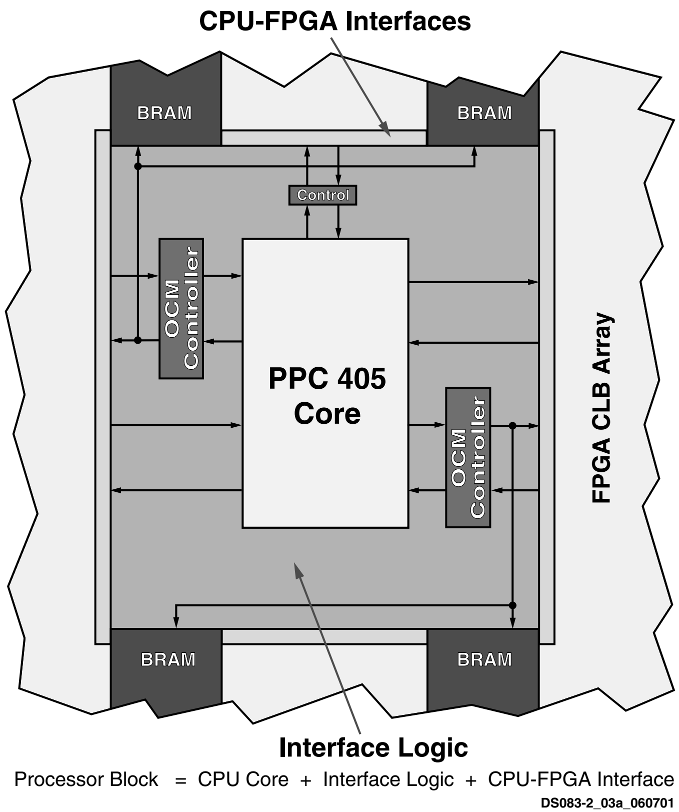


Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 μm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 7; corresponding timing characteristics are listed in Table 49.

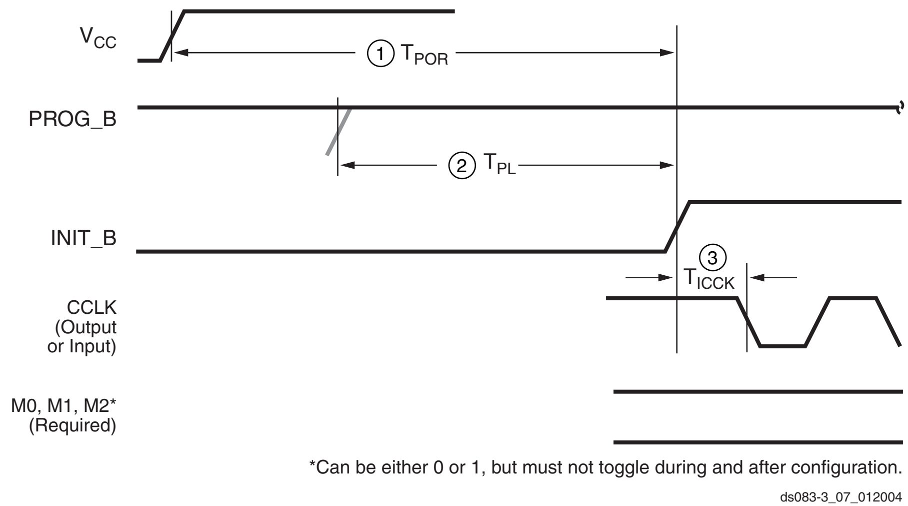


Figure 7: **Configuration Power-Up Timing**

Table 49: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.25	µs, min
			4.00	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:

1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 56: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2	1.80/–0.44	1.85/–0.41	1.96/–0.43	ns
		XC2VP4	1.82/–0.53	1.83/–0.31	1.90/–0.29	ns
		XC2VP7	1.80/–0.34	1.81/–0.24	1.88/–0.19	ns
		XC2VP20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VPX20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VP30	1.75/–0.22	1.92/–0.26	1.99/–0.23	ns
		XC2VP40	2.25/–0.54	2.40/–0.56	2.49/–0.54	ns
		XC2VP50	2.93/–1.02	2.98/–0.93	3.00/–0.83	ns
		XC2VP70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VPX70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VP100	N/A	5.58/–2.35	5.60/–2.35	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade –7 Min	–7 Max	–6 Min	–6 Max	–5 Min	–5 Max	Units
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN[3]	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)[1]	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)[2]	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)[1]	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)[2]	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)[1]	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)[2]	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)[1]	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)[2]	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

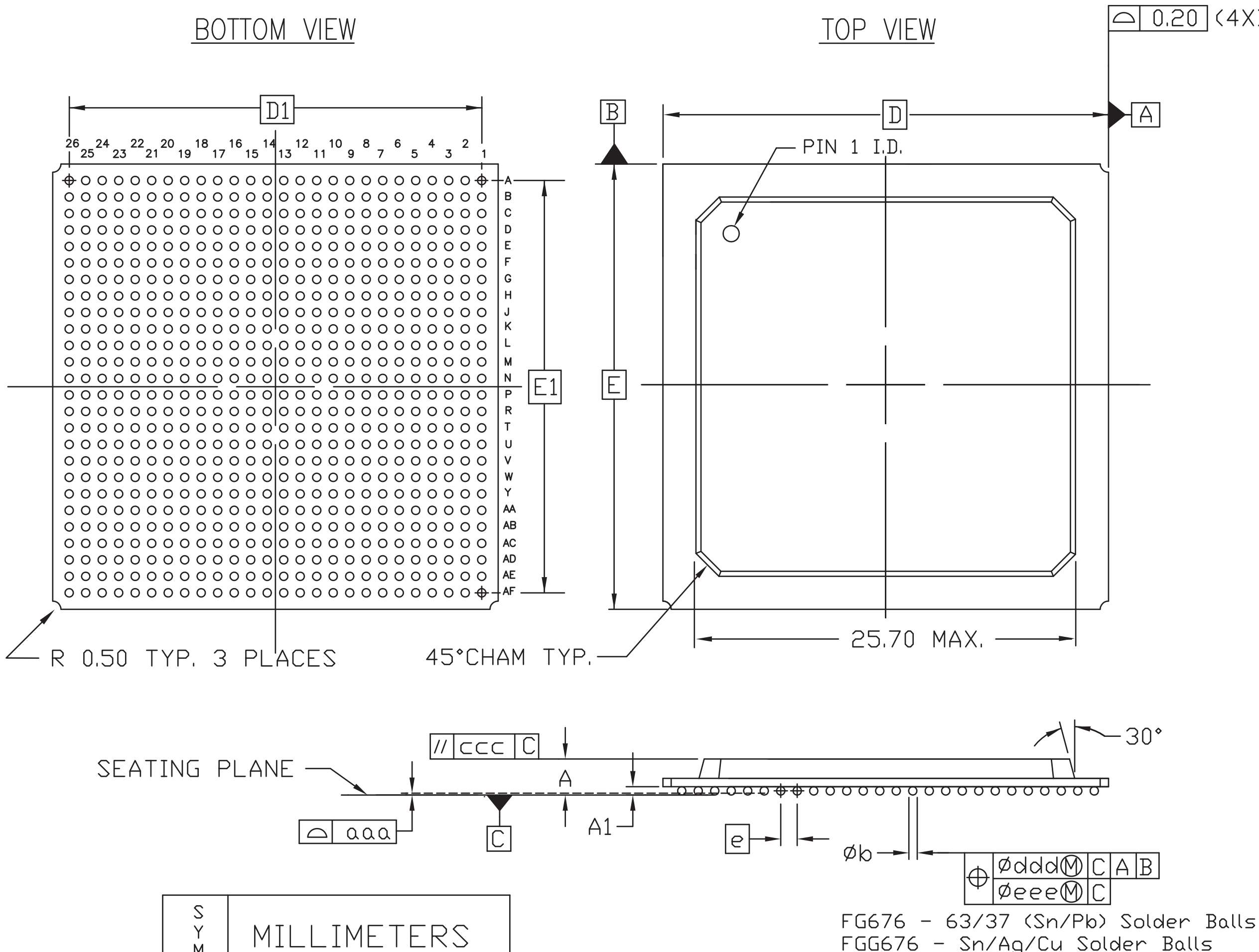
Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCAUX	L1			
N/A	VCCAUX	B21			
N/A	VCCAUX	B2			
N/A	VCCAUX	AB11			
N/A	VCCAUX	AA21			
N/A	VCCAUX	AA2			
N/A	VCCAUX	A12			
N/A	GND	Y3			
N/A	GND	Y20			
N/A	GND	W4			
N/A	GND	W19			
N/A	GND	V5			
N/A	GND	V18			
N/A	GND	P9			
N/A	GND	P14			
N/A	GND	P13			
N/A	GND	P12			
N/A	GND	P11			
N/A	GND	P10			
N/A	GND	N9			
N/A	GND	N14			
N/A	GND	N13			
N/A	GND	N12			
N/A	GND	N11			
N/A	GND	N10			
N/A	GND	M9			
N/A	GND	M14			
N/A	GND	M13			
N/A	GND	M12			
N/A	GND	M11			
N/A	GND	M10			
N/A	GND	M1			
N/A	GND	L9			
N/A	GND	L22			
N/A	GND	L14			
N/A	GND	L13			
N/A	GND	L12			

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A1	0.40	0.50	0.60
D/E	27.00 BSC		
D1/E1	25.00 REF		
e	1.00 BSC		
Øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ds083_4_03_053111

Figure 3: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	IO_L54N_1		G13	NC		
1	IO_L54P_1		H13	NC		
1	IO_L53_1/No_Pair		A10	NC		
1	IO_L50_1/No_Pair		B10	NC		
1	IO_L49N_1		F14	NC		
1	IO_L49P_1		G14	NC		
1	IO_L48N_1		F12	NC		
1	IO_L48P_1		F11	NC		
1	IO_L47N_1		B9	NC		
1	IO_L47P_1		C9	NC		
1	IO_L46N_1		E13	NC		
1	IO_L46P_1		E12	NC		
1	IO_L45N_1/VREF_1		G12			
1	IO_L45P_1		H12			
1	IO_L44N_1		A8			
1	IO_L44P_1		B8			
1	IO_L43N_1		D11			
1	IO_L43P_1		E11			
1	IO_L39N_1		G11			
1	IO_L39P_1		H11			
1	IO_L38N_1		C8			
1	IO_L38P_1		D8			
1	IO_L37N_1		D10			
1	IO_L37P_1		E10			
1	IO_L09N_1/VREF_1		G10			
1	IO_L09P_1		H10			
1	IO_L08N_1		C7			
1	IO_L08P_1		D7			
1	IO_L07N_1		F10			
1	IO_L07P_1		F9			
1	IO_L06N_1		G9			
1	IO_L06P_1		H9			
1	IO_L05_1/No_Pair		G8			
1	IO_L03N_1/VREF_1		E9			
1	IO_L03P_1		E8			
1	IO_L02N_1		F8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L41N_2		L8	NC		
2	IO_L41P_2		L7	NC		
2	IO_L42N_2		H4	NC		
2	IO_L42P_2		H3	NC		
2	IO_L43N_2		H2			
2	IO_L43P_2		J2			
2	IO_L44N_2		M8			
2	IO_L44P_2		M7			
2	IO_L45N_2		K6			
2	IO_L45P_2		K5			
2	IO_L46N_2/VREF_2		J1			
2	IO_L46P_2		K1			
2	IO_L47N_2		M6			
2	IO_L47P_2		M5			
2	IO_L48N_2		J4			
2	IO_L48P_2		J3			
2	IO_L49N_2		K2			
2	IO_L49P_2		L2			
2	IO_L50N_2		N8			
2	IO_L50P_2		N7			
2	IO_L51N_2		K4			
2	IO_L51P_2		K3			
2	IO_L52N_2/VREF_2		L1			
2	IO_L52P_2		M1			
2	IO_L53N_2		N6			
2	IO_L53P_2		N5			
2	IO_L54N_2		L5			
2	IO_L54P_2		L4			
2	IO_L55N_2		M2			
2	IO_L55P_2		N2			
2	IO_L56N_2		P9			
2	IO_L56P_2		R9			
2	IO_L57N_2		M4			
2	IO_L57P_2		M3			
2	IO_L58N_2/VREF_2		N1			
2	IO_L58P_2		P1			

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	TXNPAD11	A7		
N/A	TXPPAD11	A6		
N/A	GNDA11	C6		
N/A	RXPPAD11	A5		
N/A	RXNPAD11	A4		
N/A	VTRXPAD11	B5		
N/A	AVCCAUXRX11	B4		
N/A	AVCCAUXRX14	AV4		
N/A	VTRXPAD14	AV5		
N/A	RXNPAD14	AW4		
N/A	RXPPAD14	AW5		
N/A	GNDA14	AU6		
N/A	TXPPAD14	AW6		
N/A	TXNPAD14	AW7		
N/A	VTTXPAD14	AV7		
N/A	AVCCAUXTX14	AV6		
N/A	AVCCAUXRX16	AV8		
N/A	VTRXPAD16	AV9		
N/A	RXNPAD16	AW8		
N/A	RXPPAD16	AW9		
N/A	GNDA16	AU9		
N/A	TXPPAD16	AW10		
N/A	TXNPAD16	AW11		
N/A	VTTXPAD16	AV11		
N/A	AVCCAUXTX16	AV10		
N/A	AVCCAUXRX17	AV12		
N/A	VTRXPAD17	AV13		
N/A	RXNPAD17	AW12		
N/A	RXPPAD17	AW13		
N/A	GNDA17	AU13		
N/A	TXPPAD17	AW14		
N/A	TXNPAD17	AW15		
N/A	VTTXPAD17	AV15		
N/A	AVCCAUXTX17	AV14		
N/A	AVCCAUXRX18	AV16		
N/A	VTRXPAD18	AV17		
N/A	RXNPAD18	AW16		
N/A	RXPPAD18	AW17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L86P_2		Y12		
2	IO_L87N_2		AA9		
2	IO_L87P_2		AA10		
2	IO_L88N_2/VREF_2		AA6		
2	IO_L88P_2		AA7		
2	IO_L89N_2		AA12		
2	IO_L89P_2		AB12		
2	IO_L90N_2		AA3		
2	IO_L90P_2		AA4		
3	IO_L90N_3		AB3		
3	IO_L90P_3		AB4		
3	IO_L89N_3		AB6		
3	IO_L89P_3		AB7		
3	IO_L88N_3		AB9		
3	IO_L88P_3		AB10		
3	IO_L87N_3/VREF_3		AC3		
3	IO_L87P_3		AC4		
3	IO_L86N_3		AC11		
3	IO_L86P_3		AC12		
3	IO_L85N_3		AC6		
3	IO_L85P_3		AC7		
3	IO_L60N_3		AC9		
3	IO_L60P_3		AC10		
3	IO_L59N_3		AD9		
3	IO_L59P_3		AD10		
3	IO_L58N_3		AD1		
3	IO_L58P_3		AD2		
3	IO_L57N_3/VREF_3		AD3		
3	IO_L57P_3		AD4		
3	IO_L56N_3		AD11		
3	IO_L56P_3		AD12		
3	IO_L55N_3		AD5		
3	IO_L55P_3		AD6		
3	IO_L54N_3		AD7		
3	IO_L54P_3		AD8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L09N_4		AR11		
4	IO_L09P_4/VREF_4		AP11		
4	IO_L19N_4		AV11		
4	IO_L19P_4		AU11		
4	IO_L20N_4		AY10		
4	IO_L20P_4		AY11		
4	IO_L21N_4		AN12		
4	IO_L21P_4		AM12		
4	IO_L25N_4		AR12		
4	IO_L25P_4		AP12		
4	IO_L26N_4		AT12		
4	IO_L26P_4		AU12		
4	IO_L27N_4		AW12		
4	IO_L27P_4/VREF_4		AV12		
4	IO_L28N_4		AM13		
4	IO_L28P_4		AL13		
4	IO_L29N_4		AP13		
4	IO_L29P_4		AN13		
4	IO_L30N_4		AT13		
4	IO_L30P_4		AR13		
4	IO_L34N_4		AV13		
4	IO_L34P_4		AU13		
4	IO_L35N_4		AW13		
4	IO_L35P_4		AY13		
4	IO_L36N_4		AL15		
4	IO_L36P_4/VREF_4		AL14		
4	IO_L78N_4		AN14	NC	
4	IO_L78P_4		AM14	NC	
4	IO_L83_4/No_Pair		AR14	NC	
4	IO_L84N_4		AU14	NC	
4	IO_L84P_4		AT14	NC	
4	IO_L85N_4		AW14	NC	
4	IO_L85P_4		AV14	NC	
4	IO_L86N_4		AM15	NC	
4	IO_L86P_4		AN15	NC	
4	IO_L87N_4		AR15	NC	

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	VCCO_5		AH22		
6	VCCO_6		AU38		
6	VCCO_6		AP40		
6	VCCO_6		AL37		
6	VCCO_6		AJ39		
6	VCCO_6		AH29		
6	VCCO_6		AG34		
6	VCCO_6		AG29		
6	VCCO_6		AG28		
6	VCCO_6		AF29		
6	VCCO_6		AF28		
6	VCCO_6		AE40		
6	VCCO_6		AE29		
6	VCCO_6		AE28		
6	VCCO_6		AD29		
6	VCCO_6		AD28		
6	VCCO_6		AC38		
6	VCCO_6		AC35		
6	VCCO_6		AC29		
6	VCCO_6		AC28		
6	VCCO_6		AB29		
6	VCCO_6		AB28		
7	VCCO_7		AA29		
7	VCCO_7		AA28		
7	VCCO_7		Y38		
7	VCCO_7		Y35		
7	VCCO_7		Y29		
7	VCCO_7		Y28		
7	VCCO_7		W29		
7	VCCO_7		W28		
7	VCCO_7		V40		
7	VCCO_7		V29		
7	VCCO_7		V28		
7	VCCO_7		U29		
7	VCCO_7		U28		
7	VCCO_7		T34		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L69P_2	F6	
2	IO_L70N_2/VREF_2	G5	
2	IO_L70P_2	F5	
2	IO_L71N_2	P10	
2	IO_L71P_2	P11	
2	IO_L72N_2	G3	
2	IO_L72P_2	G4	
2	IO_L07N_2	G1	
2	IO_L07P_2	G2	
2	IO_L08N_2	N8	
2	IO_L08P_2	P9	
2	IO_L09N_2	H6	
2	IO_L09P_2	H7	
2	IO_L10N_2/VREF_2	H4	
2	IO_L10P_2	H5	
2	IO_L11N_2	R12	
2	IO_L11P_2	T12	
2	IO_L12N_2	H2	
2	IO_L12P_2	H3	
2	IO_L13N_2	J6	
2	IO_L13P_2	J7	
2	IO_L14N_2	R10	
2	IO_L14P_2	R11	
2	IO_L15N_2	J3	
2	IO_L15P_2	J4	
2	IO_L16N_2/VREF_2	J2	
2	IO_L16P_2	H1	
2	IO_L17N_2	R8	
2	IO_L17P_2	R9	
2	IO_L18N_2	K5	
2	IO_L18P_2	K6	
2	IO_L19N_2	K1	
2	IO_L19P_2	K2	
2	IO_L20N_2	T10	
2	IO_L20P_2	T11	
2	IO_L21N_2	L7	
2	IO_L21P_2	K7	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L56N_3	AC11	
3	IO_L56P_3	AC12	
3	IO_L55N_3	AD3	
3	IO_L55P_3	AE3	
3	IO_L54N_3	AE1	
3	IO_L54P_3	AE2	
3	IO_L53N_3	AC6	
3	IO_L53P_3	AC7	
3	IO_L52N_3	AF2	
3	IO_L52P_3	AF3	
3	IO_L51N_3/VREF_3	AF6	
3	IO_L51P_3	AG6	
3	IO_L50N_3	AD10	
3	IO_L50P_3	AD11	
3	IO_L49N_3	AG4	
3	IO_L49P_3	AG5	
3	IO_L48N_3	AF4	
3	IO_L48P_3	AG3	
3	IO_L47N_3	AC10	
3	IO_L47P_3	AD9	
3	IO_L46N_3	AG1	
3	IO_L46P_3	AG2	
3	IO_L45N_3/VREF_3	AG7	
3	IO_L45P_3	AH7	
3	IO_L44N_3	AC8	
3	IO_L44P_3	AD7	
3	IO_L43N_3	AH4	
3	IO_L43P_3	AH5	
3	IO_L42N_3	AH1	
3	IO_L42P_3	AH2	
3	IO_L41N_3	AE10	
3	IO_L41P_3	AE11	
3	IO_L40N_3	AJ6	
3	IO_L40P_3	AJ7	
3	IO_L39N_3/VREF_3	AH6	
3	IO_L39P_3	AJ5	
3	IO_L38N_3	AE8	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L39N_4	AM16	
4	IO_L39P_4	AL16	
4	IO_L43N_4	AR17	
4	IO_L43P_4	AR16	
4	IO_L44N_4	AV16	
4	IO_L44P_4	AU16	
4	IO_L45N_4	AP16	
4	IO_L45P_4/VREF_4	AN16	
4	IO_L10N_4	AW17	NC
4	IO_L10P_4	AW16	NC
4	IO_L11N_4	BB16	NC
4	IO_L11P_4	BA16	NC
4	IO_L12N_4	AL18	NC
4	IO_L12P_4	AL17	NC
4	IO_L16N_4	AU17	NC
4	IO_L16P_4	AT17	NC
4	IO_L18N_4	BA17	NC
4	IO_L18P_4/VREF_4	AY17	NC
4	IO_L46N_4	AT19	
4	IO_L46P_4	AT18	
4	IO_L47N_4	AN17	
4	IO_L47P_4	AM17	
4	IO_L48N_4	AV18	
4	IO_L48P_4	AU18	
4	IO_L49N_4	AY19	
4	IO_L49P_4	AY18	
4	IO_L50_4/No_Pair	AM19	
4	IO_L53_4/No_Pair	AM18	
4	IO_L54N_4	BB18	
4	IO_L54P_4	BA18	
4	IO_L55N_4	AR20	
4	IO_L55P_4	AR19	
4	IO_L56N_4	AP18	
4	IO_L56P_4	AN18	
4	IO_L57N_4	AV19	
4	IO_L57P_4/VREF_4	AU19	
4	IO_L58N_4	AW20	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	AG26	
N/A	VCCINT	AF26	
N/A	VCCINT	U26	
N/A	VCCINT	T26	
N/A	VCCINT	R26	
N/A	VCCINT	AG25	
N/A	VCCINT	T25	
N/A	VCCINT	AG24	
N/A	VCCINT	T24	
N/A	VCCINT	AG23	
N/A	VCCINT	T23	
N/A	VCCINT	AG22	
N/A	VCCINT	T22	
N/A	VCCINT	AG21	
N/A	VCCINT	T21	
N/A	VCCINT	AG20	
N/A	VCCINT	T20	
N/A	VCCINT	AG19	
N/A	VCCINT	T19	
N/A	VCCINT	AG18	
N/A	VCCINT	T18	
N/A	VCCINT	AH17	
N/A	VCCINT	AG17	
N/A	VCCINT	AF17	
N/A	VCCINT	U17	
N/A	VCCINT	T17	
N/A	VCCINT	R17	
N/A	VCCINT	AJ16	
N/A	VCCINT	AH16	
N/A	VCCINT	AG16	
N/A	VCCINT	AF16	
N/A	VCCINT	AE16	
N/A	VCCINT	AD16	
N/A	VCCINT	AC16	
N/A	VCCINT	AB16	
N/A	VCCINT	AA16	
N/A	VCCINT	Y16	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AF1	
N/A	GND	AC1	
N/A	GND	Y1	
N/A	GND	U1	
N/A	GND	N1	
N/A	GND	J1	
N/A	GND	E1	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.