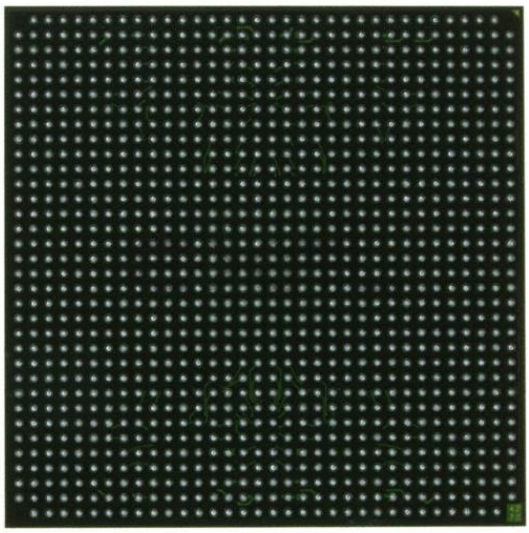

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	692
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-7ff1152c

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

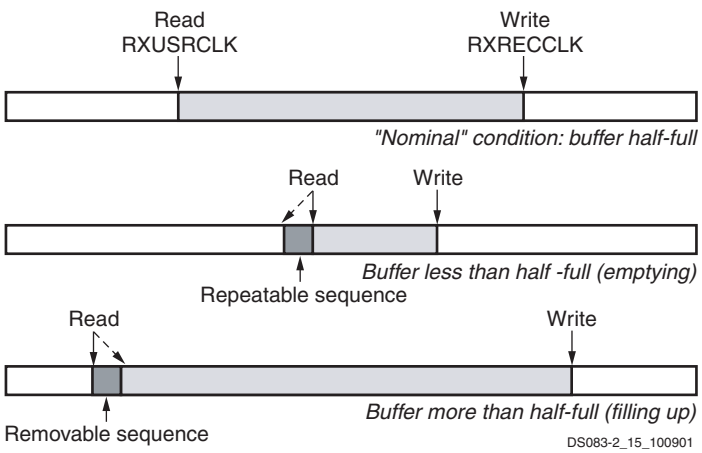

Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

memory protection. Working with appropriate system-level software, the MMU provides the following functions:

- Translation of the 4 GB effective address space into physical addresses
- Independent enabling of instruction and data translation/protection
- Page-level access control using the translation mechanism
- Software control of page replacement strategy
- Additional control over protection using zones
- Storage attributes for cache policy and speculative memory access control

The MMU can be disabled under software control. If the MMU is not used, the PPC405 core provides other storage control mechanisms.

Translation Look-Aside Buffer (TLB)

The Translation Look-Aside Buffer (TLB) is the hardware resource that controls translation and protection. It consists of 64 entries, each specifying a page to be translated. The TLB is fully associative; a given page entry can be placed anywhere in the TLB. The translation function of the MMU occurs pre-cache. Cache tags and indexing use physical addresses.

Software manages the establishment and replacement of TLB entries. This gives system software significant flexibility in implementing a custom page replacement strategy. For example, to reduce TLB thrashing or translation delays, software can reserve several TLB entries in the TLB for globally accessible static mappings. The instruction set provides several instructions used to manage TLB entries. These instructions are privileged and require the software to be executing in supervisor state. Additional TLB instructions are provided to move TLB entry fields to and from GPRs.

The MMU divides logical storage into pages. Eight page sizes (1 KB, 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB) are simultaneously supported, such that, at any given time, the TLB can contain entries for any combination of page sizes. In order for a logical to physical translation to exist, a valid entry for the page containing the logical address must be in the TLB. Addresses for which no TLB entry exists cause TLB-Miss exceptions.

To improve performance, four instruction-side and eight data-side TLB entries are kept in shadow arrays. The shadow arrays allow single-cycle address translation and also help to avoid TLB contention between load/store and instruction fetch operations. Hardware manages the replacement and invalidation of shadow-TLB entries; no system software action is required.

Memory Protection

When address translation is enabled, the translation mechanism provides a basic level of protection.

The Zone Protection Register (ZPR) enables the system software to override the TLB access controls. For example, the ZPR provides a way to deny read access to application programs. The ZPR can be used to classify storage by type; access by type can be changed without manipulating individual TLB entries.

The PowerPC Architecture provides WIU0GE (write-back / write-through, cacheability, user-defined 0, guarded, endian) storage attributes that control memory accesses, using bits in the TLB or, when address translation is disabled, storage attribute control registers.

When address translation is enabled, storage attribute control bits in the TLB control the storage attributes associated with the current page. When address translation is disabled, bits in each storage attribute control register control the storage attributes associated with storage regions. Each storage attribute control register contains 32 fields. Each field sets the associated storage attribute for a 128 MB memory region.

Timers

The embedded PPC405 core contains a 64-bit time base and three timers, as shown in Figure 17:

- Programmable Interval Timer (PIT)
- Fixed Interval Timer (FIT)
- Watchdog Timer (WDT)

The time base counter increments either by an internal signal equal to the CPU clock rate or by a separate external timer clock signal. No interrupts are generated when the time base rolls over. The three timers are synchronous with the time base.

The PIT is a 32-bit register that decrements at the same rate as the time base is incremented. The user loads the PIT register with a value to create the desired delay. When the register reaches zero, the timer stops decrementing and generates a PIT interrupt. Optionally, the PIT can be programmed to auto-reload the last value written to the PIT register, after which the PIT continues to decrement.

The FIT generates periodic interrupts based on one of four selectable bits in the time base. When the selected bit changes from 0 to 1, the PPC405 core generates a FIT interrupt.

The WDT provides a periodic critical-class interrupt based on a selected bit in the time base. This interrupt can be used for system error recovery in the event of software or system lockups. Users may select one of four time periods for the interval and the type of reset generated if the WDT expires twice without an intervening clear from software. If enabled, the watchdog timer generates a reset unless an exception handler updates the WDT status bit before the timer has completed two of the selected timer intervals.

Table 9: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LDT_25	2.5	N/R	N/R	0.500 – 0.740
LVDS_25	2.5	N/R	N/R	0.247 – 0.454
LVDSEXT_25	2.5	N/R	N/R	0.440 – 0.820
BLVDS_25	2.5	N/R	N/R	0.250 – 0.450
ULVDS_25	2.5	N/R	N/R	0.500 – 0.740
LVPECL_25	2.5	N/R	N/R	0.345 – 1.185
LDT_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740
LVDS_25_DT(1)	2.5	2.5	N/R	0.247 – 0.454
LVDSEXT_25_DT(1)	2.5	2.5	N/R	0.330 – 0.700
ULVDS_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740

Notes:
1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

Table 10: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R	Series
LVDCI_25	2.5	2.5	N/R	Series
LVDCI_DV2_25	2.5	2.5	N/R	Series
LVDCI_18	1.8	1.8	N/R	Series
LVDCI_DV2_18	1.8	1.8	N/R	Series
LVDCI_15	1.5	1.5	N/R	Series
LVDCI_DV2_15	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL18_I_DCI (3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split

Table 10: **Supported DCI I/O Standards *(Continued)***

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

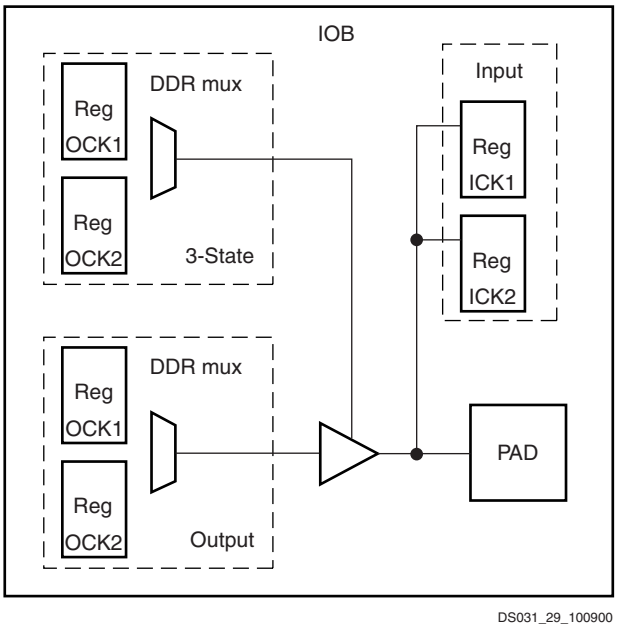

Figure 19: **Virtex-II Pro IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 27: **RocketIO Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	1.0		3.125(1)	Gb/s
		Wirebond packages	1.0		2.5(1)	Gb/s
Serial data rate, half-speed clock(3) (2X oversampling)		Flipchip packages	0.600		1.0	Gb/s
		Wirebond packages	0.600		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}	2.126 Gb/s – 3.125 Gb/s			0.17	UI(2)
		1.0626 Gb/s – 2.125 Gb/s			0.08	UI
		1.0 Gb/s – 1.0625 Gb/s			0.05	UI
		600 Mb/s – 999 Mb/s			0.08(4)	UI
Serial data output random jitter	T_{RJ}	2.126 Gb/s – 3.125 Gb/s			0.18	UI
		1.0626 Gb/s – 2.125 Gb/s			0.19	UI
		1.0 Gb/s – 1.0625 Gb/s			0.18	UI
		600 Mb/s – 999 Mb/s			0.18(4)	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(5)	T_{TXLAT}	Including CRC		14	17	TXUSR CLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

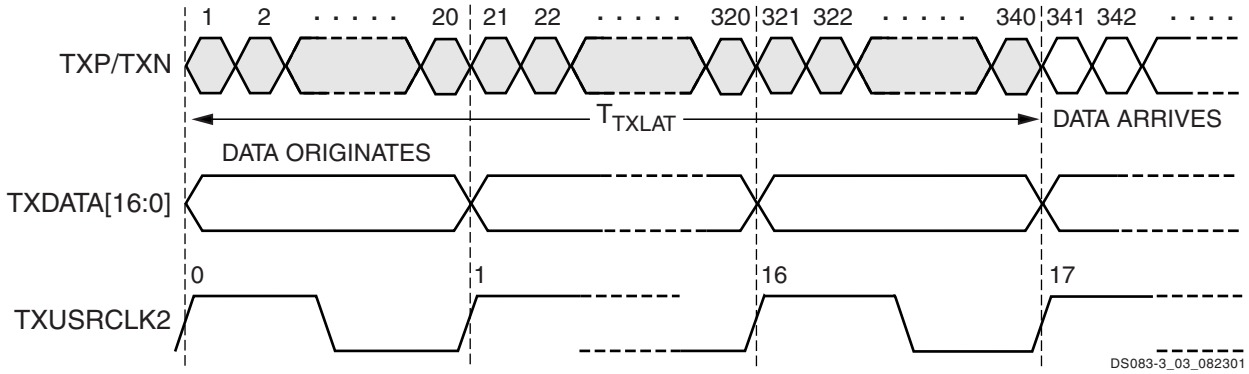

Figure 5: **RocketIO Transmit Latency (Maximum, Including CRC)**

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

Table 37: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.58	1.68	1.85	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.65	1.82	1.99	ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}	1.23	1.35	1.51	ns, max
T input to valid data on Pad	T_{IOTP}	1.51	1.63	1.78	ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$	1.08	1.22	1.36	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.56	1.69	1.85	ns, max
GTS to Pad high-impedance(2)	T_{GTS}	4.11	4.73	5.20	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.59	1.76	1.93	ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}	1.39	1.55	1.73	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.67	1.82	2.00	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
Set/Reset Delays					
Minimum Pulse Width, SR inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
SR input to Pad (asynchronous)	T_{IOSRP}	2.33	2.56	2.83	ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}	1.97	2.16	2.41	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.24	2.44	2.69	ns, max
GSR to Pad	T_{IOGSRQ}	5.87	6.75	7.43	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

Virtex-II Pro Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [TSAMP^{(1)} + TCKSKEW^{(2)} + TPKGSKEW^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/17/02	2.0	• Added new Virtex-II Pro family members. • Added timing parameters from speedsfile **v1.62**. • Added Table 46, Pipelined Multiplier Switching Characteristics. • Added 3.3V-vs-2.5V table entries for some parameters.
09/03/02	2.1	• Added Source-Synchronous Switching Characteristics section. • Added absolute max ratings for 3.3V-vs-2.5V parameters in Table 1. • Added recommended operating conditions for V_{IN} and RocketIO footnote to Table 2. • Updated SSTL2 values in Table 6. Added SSTL18 values: Table 6, Table 39, Table 32. [Table 32 removed in v2.8.] • Added Table 10, which contains LVPECL DC specifications.
09/27/02	2.2	Added section General Power Supply Requirements.
11/20/02	2.3	Updated parametric information in: • Table 1: Increase Absolute Max Rating for V_{CCO}, V_{REF}, V_{IN}, and V_{TS} from 3.6V to 3.75V. Delete cautionary footnotes related to voltage overshoot/undershoot. • Table 2: Delete V_{CCO} specifications for 2.5V and below operation. Delete footnote referencing special information for 3.3V operation. Add footnote for PCI/PCI-X. • Table 3: Add I_{BATT}. Delete I_L specifications for 2.5V and below operation. • Table 4: Add Typical Quiescent Supply Currents for XC2VP4 and XC2VP7 only • Table 6: Correct I_{OL} and I_{OH} for SSTL2 I. Add rows for LVTTL, LVCMOS33, and PCI-X. Correct max V_{IH} from V_{CCO} to 3.6V. • Table 7: Correct Min/Max V_{OD}, V_{OCM}, and V_{ICM} • Table 10: Reformat LVPECL DC Specifications to match Virtex-II data sheet format • Table 12: Correct parameter name from Differential Output Voltage to Single-Ended Output Voltage Swing. • Table 16: Add CPMC405CLOCK max frequencies • Table 27: Add footnote regarding serial data rate limitation in -5 part. • Table 39: Add rows for LVTTL, LVCMOS33, and PCI-X. • Table 32: Add LVTTL, LVCMOS33, and PCI-X. Correct all capacitive load values (except PCI/PCI-X) to 0 pF. [Table 32 removed in v2.8.] • Table 51: Correct CCLK max frequencies
11/25/02	2.4	Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.3V to –0.5V for 3.3V.

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 5, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L56N_2	J21	NC		
2	IO_L56P_2	J22	NC		
2	IO_L58N_2/VREF_2	J18	NC		
2	IO_L58P_2	K18	NC		
2	IO_L60N_2	K19	NC		
2	IO_L60P_2	K20	NC		
2	IO_L85N_2	K21			
2	IO_L85P_2	K22			
2	IO_L86N_2	K17			
2	IO_L86P_2	L17			
2	IO_L88N_2/VREF_2	L18			
2	IO_L88P_2	L19			
2	IO_L90N_2	L20			
2	IO_L90P_2	L21			
3	IO_L90N_3	M21			
3	IO_L90P_3	M20			
3	IO_L89N_3	M19			
3	IO_L89P_3	M18			
3	IO_L87N_3/VREF_3	M17			
3	IO_L87P_3	N17			
3	IO_L85N_3	N22			
3	IO_L85P_3	N21			
3	IO_L60N_3	N20	NC		
3	IO_L60P_3	N19	NC		
3	IO_L59N_3	N18	NC		
3	IO_L59P_3	P18	NC		
3	IO_L57N_3/VREF_3	P22	NC		
3	IO_L57P_3	P21	NC		
3	IO_L55N_3	P20	NC		
3	IO_L55P_3	P19	NC		
3	IO_L54N_3	P17	NC		
3	IO_L54P_3	R18	NC		
3	IO_L53N_3	R22	NC		
3	IO_L53P_3	R21	NC		
3	IO_L51N_3/VREF_3	R20	NC		
3	IO_L51P_3	R19	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXRX19	AE15			
N/A	VTRXPAD19	AE16			
N/A	RXNPAD19	AF15			
N/A	RXPPAD19	AF16			
N/A	GNDA19	AD16			
N/A	TXPPAD19	AF17			
N/A	TXNPAD19	AF18			
N/A	VTTXPAD19	AE18			
N/A	AVCCAUXTX19	AE17			
N/A	AVCCAUXRX21	AE20	NC	NC	
N/A	VTRXPAD21	AE21	NC	NC	
N/A	RXNPAD21	AF20	NC	NC	
N/A	RXPPAD21	AF21	NC	NC	
N/A	GNDA21	AD22	NC	NC	
N/A	TXPPAD21	AF22	NC	NC	
N/A	TXNPAD21	AF23	NC	NC	
N/A	VTTXPAD21	AE23	NC	NC	
N/A	AVCCAUXTX21	AE22	NC	NC	
N/A	VCCINT	H8			
N/A	VCCINT	J9			
N/A	VCCINT	K9			
N/A	VCCINT	U9			
N/A	VCCINT	V9			
N/A	VCCINT	W8			
N/A	VCCINT	H19			
N/A	VCCINT	J10			
N/A	VCCINT	J17			
N/A	VCCINT	J18			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K18			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U11			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AF34				
N/A	GND	B34				
N/A	GND	C1				
N/A	GND	C2				
N/A	GND	C10				
N/A	GND	C16				
N/A	GND	C19				
N/A	GND	C25				
N/A	GND	C33				
N/A	GND	C34				
N/A	GND	D4				
N/A	GND	D31				
N/A	GND	E5				
N/A	GND	E12				
N/A	GND	E23				
N/A	GND	E30				
N/A	GND	F6				
N/A	GND	F29				
N/A	GND	G7				
N/A	GND	G28				
N/A	GND	B1				
N/A	GND	H8				
N/A	GND	H12				
N/A	GND	H15				
N/A	GND	H20				
N/A	GND	J1				
N/A	GND	H27				
N/A	GND	AF1				
N/A	GND	K3				
N/A	GND	K32				
N/A	GND	M5				
N/A	GND	M8				
N/A	GND	M27				
N/A	GND	M30				
N/A	GND	P14				
N/A	GND	P15				
N/A	GND	P16				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L75N_1/GCLK3P	C17		
1	IO_L75P_1/GCLK2S	B17		
1	IO_L74N_1/GCLK1P	L17		
1	IO_L74P_1/GCLK0S	K17		
1	IO_L73N_1	E17		
1	IO_L73P_1	D17		
1	IO_L69N_1/VREF_1	G17		
1	IO_L69P_1	F17		
1	IO_L68N_1	J17		
1	IO_L68P_1	H17		
1	IO_L67N_1	C16		
1	IO_L67P_1	B16		
1	IO_L66N_1/VREF_1	G16	NC	
1	IO_L66P_1	F16	NC	
1	IO_L57N_1/VREF_1	B15		
1	IO_L57P_1	A15		
1	IO_L56N_1	L16		
1	IO_L56P_1	K16		
1	IO_L55N_1	D16		
1	IO_L55P_1	C15		
1	IO_L54N_1	F15		
1	IO_L54P_1	E15		
1	IO_L53_1/No_Pair	H16		
1	IO_L50_1/No_Pair	G15		
1	IO_L49N_1	B14		
1	IO_L49P_1	A14		
1	IO_L48N_1	D14		
1	IO_L48P_1	C14		
1	IO_L47N_1	L15		
1	IO_L47P_1	K15		
1	IO_L46N_1	F14		
1	IO_L46P_1	E14		
1	IO_L45N_1/VREF_1	H14		
1	IO_L45P_1	G14		
1	IO_L44N_1	L14		
1	IO_L44P_1	K14		
1	IO_L43N_1	C13		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AP5		
N/A	GND	AK5		
N/A	GND	AF5		
N/A	GND	AB5		
N/A	GND	W5		
N/A	GND	T5		
N/A	GND	N5		
N/A	GND	J5		
N/A	GND	E5		
N/A	GND	A5		
N/A	GND	AM3		
N/A	GND	C3		
N/A	GND	AN2		
N/A	GND	B2		
N/A	GND	AK1		
N/A	GND	AF1		
N/A	GND	AB1		
N/A	GND	W1		
N/A	GND	V1		
N/A	GND	T1		
N/A	GND	N1		
N/A	GND	J1		
N/A	GND	E1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L43N_7	R37		
7	IO_L42P_7	R34		
7	IO_L42N_7	R35		
7	IO_L41P_7	U28		
7	IO_L41N_7	T28		
7	IO_L40P_7	R32		
7	IO_L40N_7/VREF_7	R33		
7	IO_L39P_7	P38		
7	IO_L39N_7	P39		
7	IO_L38P_7	T29		
7	IO_L38N_7	T30		
7	IO_L37P_7	N37		
7	IO_L37N_7	P37		
7	IO_L36P_7	P35		
7	IO_L36N_7	P36		
7	IO_L35P_7	T27		
7	IO_L35N_7	R27		
7	IO_L34P_7	P33		
7	IO_L34N_7/VREF_7	P34		
7	IO_L33P_7	N38		
7	IO_L33N_7	N39		
7	IO_L32P_7	R28		
7	IO_L32N_7	R29		
7	IO_L31P_7	N35		
7	IO_L31N_7	M36		
7	IO_L30P_7	N33		
7	IO_L30N_7	N34		
7	IO_L29P_7	R30		
7	IO_L29N_7	R31		
7	IO_L28P_7	M37		
7	IO_L28N_7/VREF_7	M38		
7	IO_L27P_7	M33		
7	IO_L27N_7	M34		
7	IO_L26P_7	P28		
7	IO_L26N_7	P29		
7	IO_L25P_7	L38		
7	IO_L25N_7	L39		
7	IO_L24P_7	L36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	VCCINT	R17		
N/A	VCCINT	AE16		
N/A	VCCINT	AD16		
N/A	VCCINT	T16		
N/A	VCCINT	R16		
N/A	VCCINT	AE15		
N/A	VCCINT	AD15		
N/A	VCCINT	AC15		
N/A	VCCINT	AB15		
N/A	VCCINT	AA15		
N/A	VCCINT	Y15		
N/A	VCCINT	W15		
N/A	VCCINT	V15		
N/A	VCCINT	U15		
N/A	VCCINT	T15		
N/A	VCCINT	R15		
N/A	VCCINT	AF14		
N/A	VCCINT	P14		
N/A	VCCINT	AG13		
N/A	VCCINT	N13		
N/A	VCCINT	AH12		
N/A	VCCINT	M12		
N/A	VCCAUX	AV39		
N/A	VCCAUX	AA39		
N/A	VCCAUX	Y39		
N/A	VCCAUX	W39		
N/A	VCCAUX	B39		
N/A	VCCAUX	AW38		
N/A	VCCAUX	Y38		
N/A	VCCAUX	A38		
N/A	VCCAUX	AR35		
N/A	VCCAUX	E35		
N/A	VCCAUX	AP34		
N/A	VCCAUX	F34		
N/A	VCCAUX	AW20		
N/A	VCCAUX	AV20		
N/A	VCCAUX	B20		
N/A	VCCAUX	A20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AA5		
N/A	GND		Y41		
N/A	GND		Y26		
N/A	GND		Y25		
N/A	GND		Y24		
N/A	GND		Y23		
N/A	GND		Y22		
N/A	GND		Y21		
N/A	GND		Y20		
N/A	GND		Y19		
N/A	GND		Y18		
N/A	GND		Y17		
N/A	GND		Y2		
N/A	GND		W26		
N/A	GND		W25		
N/A	GND		W24		
N/A	GND		W23		
N/A	GND		W22		
N/A	GND		W21		
N/A	GND		W20		
N/A	GND		W19		
N/A	GND		W18		
N/A	GND		W17		
N/A	GND		V37		
N/A	GND		V34		
N/A	GND		V26		
N/A	GND		V25		
N/A	GND		V24		
N/A	GND		V23		
N/A	GND		V22		
N/A	GND		V21		
N/A	GND		V20		
N/A	GND		V19		
N/A	GND		V18		
N/A	GND		V17		
N/A	GND		V9		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCAUX	A2	
N/A	VCCAUX	BA1	
N/A	VCCAUX	AY1	
N/A	VCCAUX	AL1	
N/A	VCCAUX	AB1	
N/A	VCCAUX	AA1	
N/A	VCCAUX	M1	
N/A	VCCAUX	C1	
N/A	VCCAUX	B1	
N/A	GND	AV42	
N/A	GND	AP42	
N/A	GND	AK42	
N/A	GND	AF42	
N/A	GND	AC42	
N/A	GND	Y42	
N/A	GND	U42	
N/A	GND	N42	
N/A	GND	J42	
N/A	GND	E42	
N/A	GND	BA41	
N/A	GND	AY41	
N/A	GND	C41	
N/A	GND	B41	
N/A	GND	BA40	
N/A	GND	B40	
N/A	GND	BB38	
N/A	GND	AV38	
N/A	GND	AP38	
N/A	GND	AK38	
N/A	GND	AF38	
N/A	GND	AC38	
N/A	GND	Y38	
N/A	GND	U38	
N/A	GND	N38	
N/A	GND	J38	
N/A	GND	E38	
N/A	GND	A38	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	E13	
N/A	GND	A13	
N/A	GND	AD12	
N/A	GND	W12	
N/A	GND	BB9	
N/A	GND	AV9	
N/A	GND	AP9	
N/A	GND	AK9	
N/A	GND	AF9	
N/A	GND	AC9	
N/A	GND	Y9	
N/A	GND	U9	
N/A	GND	N9	
N/A	GND	J9	
N/A	GND	E9	
N/A	GND	A9	
N/A	GND	BB5	
N/A	GND	AV5	
N/A	GND	AP5	
N/A	GND	AK5	
N/A	GND	AF5	
N/A	GND	AC5	
N/A	GND	Y5	
N/A	GND	U5	
N/A	GND	N5	
N/A	GND	J5	
N/A	GND	E5	
N/A	GND	A5	
N/A	GND	BA3	
N/A	GND	B3	
N/A	GND	BA2	
N/A	GND	AY2	
N/A	GND	C2	
N/A	GND	B2	
N/A	GND	AV1	
N/A	GND	AP1	
N/A	GND	AK1	