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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5904
Number of Logic Elements/Cells	53136
Total RAM Bits	4276224
Number of I/O	852
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp50-7ffg1517c

memory protection. Working with appropriate system-level software, the MMU provides the following functions:

- Translation of the 4 GB effective address space into physical addresses
- Independent enabling of instruction and data translation/protection
- Page-level access control using the translation mechanism
- Software control of page replacement strategy
- Additional control over protection using zones
- Storage attributes for cache policy and speculative memory access control

The MMU can be disabled under software control. If the MMU is not used, the PPC405 core provides other storage control mechanisms.

Translation Look-Aside Buffer (TLB)

The Translation Look-Aside Buffer (TLB) is the hardware resource that controls translation and protection. It consists of 64 entries, each specifying a page to be translated. The TLB is fully associative; a given page entry can be placed anywhere in the TLB. The translation function of the MMU occurs pre-cache. Cache tags and indexing use physical addresses.

Software manages the establishment and replacement of TLB entries. This gives system software significant flexibility in implementing a custom page replacement strategy. For example, to reduce TLB thrashing or translation delays, software can reserve several TLB entries in the TLB for globally accessible static mappings. The instruction set provides several instructions used to manage TLB entries. These instructions are privileged and require the software to be executing in supervisor state. Additional TLB instructions are provided to move TLB entry fields to and from GPRs.

The MMU divides logical storage into pages. Eight page sizes (1 KB, 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB) are simultaneously supported, such that, at any given time, the TLB can contain entries for any combination of page sizes. In order for a logical to physical translation to exist, a valid entry for the page containing the logical address must be in the TLB. Addresses for which no TLB entry exists cause TLB-Miss exceptions.

To improve performance, four instruction-side and eight data-side TLB entries are kept in shadow arrays. The shadow arrays allow single-cycle address translation and also help to avoid TLB contention between load/store and instruction fetch operations. Hardware manages the replacement and invalidation of shadow-TLB entries; no system software action is required.

Memory Protection

When address translation is enabled, the translation mechanism provides a basic level of protection.

The Zone Protection Register (ZPR) enables the system software to override the TLB access controls. For example, the ZPR provides a way to deny read access to application programs. The ZPR can be used to classify storage by type; access by type can be changed without manipulating individual TLB entries.

The PowerPC Architecture provides WIU0GE (write-back / write-through, cacheability, user-defined 0, guarded, endian) storage attributes that control memory accesses, using bits in the TLB or, when address translation is disabled, storage attribute control registers.

When address translation is enabled, storage attribute control bits in the TLB control the storage attributes associated with the current page. When address translation is disabled, bits in each storage attribute control register control the storage attributes associated with storage regions. Each storage attribute control register contains 32 fields. Each field sets the associated storage attribute for a 128 MB memory region.

Timers

The embedded PPC405 core contains a 64-bit time base and three timers, as shown in Figure 17:

- Programmable Interval Timer (PIT)
- Fixed Interval Timer (FIT)
- Watchdog Timer (WDT)

The time base counter increments either by an internal signal equal to the CPU clock rate or by a separate external timer clock signal. No interrupts are generated when the time base rolls over. The three timers are synchronous with the time base.

The PIT is a 32-bit register that decrements at the same rate as the time base is incremented. The user loads the PIT register with a value to create the desired delay. When the register reaches zero, the timer stops decrementing and generates a PIT interrupt. Optionally, the PIT can be programmed to auto-reload the last value written to the PIT register, after which the PIT continues to decrement.

The FIT generates periodic interrupts based on one of four selectable bits in the time base. When the selected bit changes from 0 to 1, the PPC405 core generates a FIT interrupt.

The WDT provides a periodic critical-class interrupt based on a selected bit in the time base. This interrupt can be used for system error recovery in the event of software or system lockups. Users may select one of four time periods for the interval and the type of reset generated if the WDT expires twice without an intervening clear from software. If enabled, the watchdog timer generates a reset unless an exception handler updates the WDT status bit before the timer has completed two of the selected timer intervals.

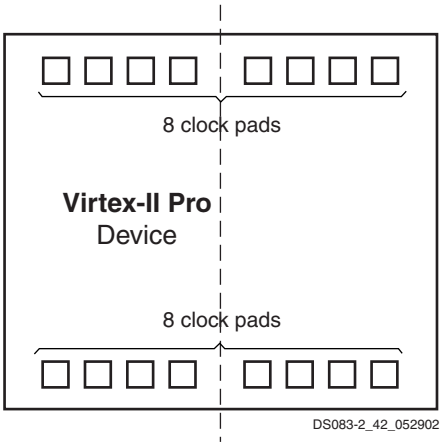

Figure 55: **Virtex-II Pro Clock Pads**

Each global clock multiplexer buffer can be driven either by the clock pad to distribute a clock directly to the device, or by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 51. Each global clock multiplexer buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock multiplexer buffer inputs, as shown in Figure 56.

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM+ blocks.

Eight global clocks can be used in each quadrant of the Virtex-II Pro device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning. (See the *Virtex-II Pro Platform FPGA User Guide*.)

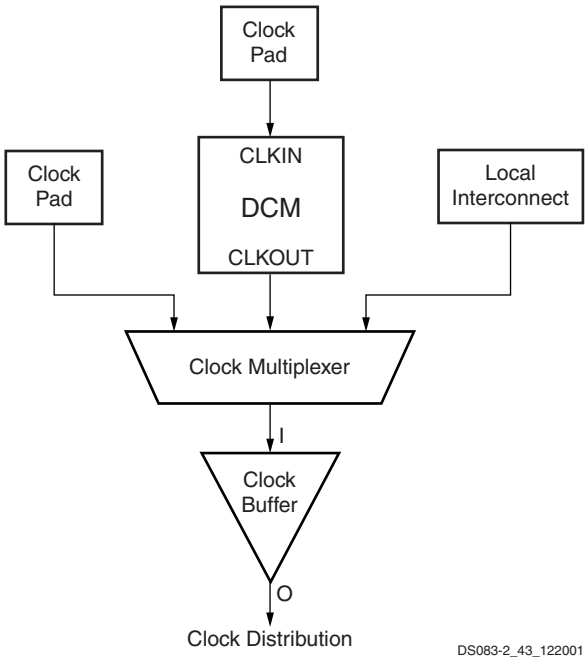

Figure 56: **Virtex-II Pro Clock Multiplexer Buffer Configuration**

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 27.

Table 27: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, connect the CLKFB input to CLK0. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$\mathrm{FREQ}_{\mathrm{CLKFX}} = (M/D) \bullet \mathrm{FREQ}_{\mathrm{CLKIN}}$$

where M and D are two integers. Specifications for M and D are provided under **DCM Timing Parameters** in Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics. By default, $M = 4$ and $D = 1$, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles, with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode. See Table 28 for more details.

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Table 28: **CLKDV Duty Cycle for Non-integer Divides**

CLKDV_DIVIDE	Duty Cycle
1.5	1/3
2.5	2/5
3.5	3/7
4.5	4/9
5.5	5/11
6.5	6/13
7.5	7/15

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 63 illustrates the effects of fine-phase shifting. For more information on DCM features, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 29 lists fine-phase shifting control pins, when used in variable mode.

Table 29: **Fine Phase Shifting Control Pins**

Control Pin	Direction	Function
PSINCDEC	In	Increment or decrement
PSEN	In	Enable ± phase shift
PSCLK	In	Clock for phase shift
PSDONE	Out	Active when completed

- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant. (See Global Clock Multiplexer Buffers, page 48.)
- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row. (See 3-State Buffers, page 43.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice. (See CLB/Slice Configurations, page 44.)
- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See Sum of Products, page 42.)
- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See Shift Registers, page 39.)

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II Pro device configuration using Boundary-Scan is compatible with with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 32: **Virtex-II Pro Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 33 lists the default total number of bits required to configure each device.

Table 33: **Virtex-II Pro Default Bitstream Lengths**

Device	Number of Configuration Bits
XC2VP2	1,305,376
XC2VP4	3,006,496
XC2VP7	4,485,408
XC2VP20	8,214,560
XC2VPX20	8,214,560
XC2VP30	11,589,920
XC2VP40	15,868,192
XC2VP50	19,021,344
XC2VP70	26,098,976
XC2VPX70	26,098,976
XC2VP100	34,292,768

Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 26: **RocketIO X Transmitter Switching Characteristics**(1)

Description	Symbol	Conditions	BREFCLK Frequency	Min	Typ	Max	Units
Serial data rate	F_{GTX}			2.488		6.25	Gb/s
Serial data output total jitter (p-p)(3)	T_{TJ}	2.488 Gb/s			0.15	0.20	UI(2)
		3.125 Gb/s			0.14	0.19	UI
		4.25 Gb/s			0.39	0.48	UI
		6.25 Gb/s			0.42	0.54	UI
Serial data output deterministic jitter (p-p)(3)	T_{DJ}	2.488 Gb/s	155.52 MHz		0.03	0.17	UI
		3.125 Gb/s	156.25 MHz		0.03	0.17	UI
		4.25 Gb/s	212.5 MHz		0.14	0.26	UI
		6.25 Gb/s	312.5 MHz		0.17	0.35	UI
Serial data output random jitter (p-p)(3,4)	T_{RJ}	2.488 Gb/s	155.52 MHz		0.12	0.18	UI
		3.125 Gb/s	156.25 MHz		0.12	0.20	UI
		4.25 Gb/s	212.5 MHz		0.25	0.39	UI
		6.25 Gb/s	312.5 MHz		0.25	0.39	UI
TX rise time	T_{RTX}	20% – 80% @ 2.500 Gb/s			60		ps
TX fall time	T_{FTX}				60		ps
Transmit latency(5)	T_{TXLAT}				14	19	TXUSRCLK cycles
TXUSRCLK duty cycle	T_{TXDC}			45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}			45	50	55	%

Notes:
1. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.
2. UI = Unit Interval
3. Total Jitter $T_{TJ} = T_{DJ} + T_{RJ}$
4. T_{RJ} specifications are *wideband* and include low-frequency jitter components (also referred to as *wander*).T_{RJ} specified is peak-to-peak, estimated at BER=10^{-12} using the Bathtub Method.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO X Transceiver User Guide*** for more information on calculating latency.

Table 38: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.62	0.71	0.78	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.20	0.23	0.25	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.00	0.00	0.00	ns
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.03	–0.03	–0.04	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.15	–0.15	–0.15	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	4.20	4.83	5.31	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	2.76	3.18	3.49	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	1.91	2.20	2.41	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	1.92	2.20	2.42	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	1.58	1.81	1.99	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	0.76	0.87	0.96	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	2.34	2.69	2.95	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	0.71	0.81	0.89	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.50	0.57	0.63	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.48	0.55	0.61	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.30	0.34	0.38	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.11	0.12	0.13	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	6.19	7.12	7.83	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	4.28	4.93	5.42	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	2.81	3.24	3.56	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	2.55	2.93	3.23	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	1.31	1.51	1.66	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	1.28	1.47	1.62	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	2.26	2.60	2.86	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	1.66	1.90	2.09	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	0.65	0.75	0.82	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.94	1.08	1.19	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.25	0.29	0.32	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.28	0.32	0.35	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	0.01	0.01	0.01	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	0.13	0.15	0.16	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	0.13	0.14	0.16	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	0.13	0.14	0.16	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{OLVPECL\_25}$	0.17	0.19	0.21	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	0.83	0.93	1.01	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	0.89	0.97	1.05	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	0.92	1.02	1.10	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	0.08	0.10	0.11	ns
GTL Plus	GTLP	T_{OGTLP}	0.04	0.05	0.06	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.56	0.64	0.70	ns

Date	Version	Revision
08/25/03	2.9	• Updated time and frequency parameters as per speedsfile **v1.81**. • Table 1: Footnote (2) rewritten to specify “one or more banks.” • Table 2: Added footnote referring to XAPP659 for 3.3V I/O operation. • Table 53 and Table 54: Revised test setup footnote to refer to Figure 6. Previously specified a capacitive load parameter. • Table 57: Due to a document compilation error in v2.8, some DCM parameters were erroneously omitted from the full data sheet file (all four modules concatenated), though not from the stand-alone Module 3 file. The omitted parameters have been restored. • Table 64 and Table 66: Corrected parameters to expression in picoseconds, as labeled. Previously expressed in nanoseconds, but labeled picoseconds. • Figure 6: Added note to figure regarding termination resistors. • Table 5: Added $I_{CCINTMIN}$ for XC2VP30 device.
09/10/03	2.10	• Figure 7: Changed representation of mode pins M0, M1, and M2 indicating that they must be held to a constant DC level during and after configuration. • Table 49: Added footnote indicating that mode pins M0, M1, and M2 must be held to a constant DC level during and after configuration.
10/14/03	2.11	• Table 1: Deleted Footnote (2), which had derated the absolute maximum T_J when one or more banks operated at 3.3V. Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. Added new Footnote (2) linking to website for package thermal data. • Table 4 and Table 5: Filled in power-on and quiescent current parameters for all devices through XC2VP70. Added Industrial Grade multiplier specification to Footnote (1) in both tables. • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 39 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 40, Output Delay Measurement Methodology. - Replaced Figure 6, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 58: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
11/10/03	2.12	• Table 1: Changed 3.3V absolute max V_{IN} and V_{TS} from 3.75V to 4.05V. Added footnote referring to **XAPP659**. • Table 4: Removed MIN column from table.
12/05/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, updated and released to **Production status** as per speedsfile **v1.83**. Featured changes: - Speedsfile parameter values for -7 speed grade added for devices XC2VP2-XC2VP70. - Table 13 and Table 14: Pin-to-pin and register-to_register performance parameter values added. - Table 64: New parameter T_{DCD_LOCAL} (and footnote) replaces T_{DCD_CLK0}. - All remaining source-synchronous parameter values added (Table 64 & following).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L03P_3	AC25			
3	IO_L02N_3	AC24			
3	IO_L02P_3	AD25			
3	IO_L01N_3/VRP_3	AD26			
3	IO_L01P_3/VRN_3	AE26			
4	IO_L01N_4/BUSY/DOUT(1)	AB22			
4	IO_L01P_4/INIT_B	AC22			
4	IO_L02N_4/D0/DIN(1)	AB21			
4	IO_L02P_4/D1	AC21			
4	IO_L03N_4/D2	Y20			
4	IO_L03P_4/D3	AA20			
4	IO_L05_4/No_Pair	AB20			
4	IO_L06N_4/VRP_4	AC20			
4	IO_L06P_4/VRN_4	AD20			
4	IO_L07N_4	W19			
4	IO_L07P_4/VREF_4	Y19			
4	IO_L09N_4	AA19			
4	IO_L09P_4/VREF_4	AB19			
4	IO_L37N_4	AE19			
4	IO_L37P_4	AF19			
4	IO_L39N_4	W18			
4	IO_L39P_4	Y18			
4	IO_L43N_4	AA18			
4	IO_L43P_4	AB18			
4	IO_L45N_4	AC18			
4	IO_L45P_4/VREF_4	AD18			
4	IO_L46N_4	W17			
4	IO_L46P_4	W16			
4	IO_L48N_4	AB17			
4	IO_L48P_4	AB16			
4	IO_L49N_4	AC17			
4	IO_L49P_4	AD17			
4	IO_L50_4/No_Pair	Y16			
4	IO_L53_4/No_Pair	AA16			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
1	IO_L06N_1	E9			
1	IO_L06P_1	E8			
1	IO_L05_1/No_Pair	F8			
1	IO_L03N_1/VREF_1	D7			
1	IO_L03P_1	E7			
1	IO_L02N_1	C6			
1	IO_L02P_1	D6			
1	IO_L01N_1/VRP_1	A3			
1	IO_L01P_1/VRN_1	B3			
2	IO_L01N_2/VRP_2	C4			
2	IO_L01P_2/VRN_2	D3			
2	IO_L02N_2	A2			
2	IO_L02P_2	B1			
2	IO_L03N_2	C2			
2	IO_L03P_2	C1			
2	IO_L04N_2/VREF_2	D2			
2	IO_L04P_2	D1			
2	IO_L05N_2	E4			
2	IO_L05P_2	E3			
2	IO_L06N_2	E2			
2	IO_L06P_2	E1			
2	IO_L40N_2/VREF_2	F5	NC	NC	NC
2	IO_L40P_2	F4	NC	NC	NC
2	IO_L42N_2	F3	NC	NC	NC
2	IO_L42P_2	F2	NC	NC	NC
2	IO_L43N_2	G6	NC		
2	IO_L43P_2	G5	NC		
2	IO_L44N_2	G4	NC		
2	IO_L44P_2	G3	NC		
2	IO_L45N_2	F1	NC		
2	IO_L45P_2	G1	NC		
2	IO_L46N_2/VREF_2	H6	NC		
2	IO_L46P_2	H5	NC		
2	IO_L47N_2	H4	NC		
2	IO_L47P_2	H3	NC		
2	IO_L48N_2	H2	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L87N_7	M25			
7	IO_L86P_7	M24			
7	IO_L86N_7	M23			
7	IO_L85P_7	M22			
7	IO_L85N_7	M21			
7	IO_L60P_7	N19	NC		
7	IO_L60N_7	M19	NC		
7	IO_L59P_7	L26	NC		
7	IO_L59N_7	L25	NC		
7	IO_L58P_7	L24	NC		
7	IO_L58N_7/VREF_7	L23	NC		
7	IO_L57P_7	L22	NC		
7	IO_L57N_7	L21	NC		
7	IO_L56P_7	M20	NC		
7	IO_L56N_7	L20	NC		
7	IO_L55P_7	L19	NC		
7	IO_L55N_7	K20	NC		
7	IO_L54P_7	K26	NC		
7	IO_L54N_7	J26	NC		
7	IO_L53P_7	K24	NC		
7	IO_L53N_7	K23	NC		
7	IO_L52P_7	K22	NC		
7	IO_L52N_7/VREF_7	K21	NC		
7	IO_L51P_7	J25	NC		
7	IO_L51N_7	J24	NC		
7	IO_L50P_7	J23	NC		
7	IO_L50N_7	J22	NC		
7	IO_L49P_7	J21	NC		
7	IO_L49N_7	J20	NC		
7	IO_L48P_7	H26	NC		
7	IO_L48N_7	H25	NC		
7	IO_L47P_7	H24	NC		
7	IO_L47N_7	H23	NC		
7	IO_L46P_7	H22	NC		
7	IO_L46N_7/VREF_7	H21	NC		
7	IO_L45P_7	G26	NC		
7	IO_L45N_7	F26	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		C14			
N/A	GND		C3			
N/A	GND		B29			
N/A	GND		B2			
N/A	GND		A22			
N/A	GND		A9			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L06N_6	AM34		
6	IO_L07P_6	AN30		
6	IO_L07N_6	AM30		
6	IO_L08P_6	AM26		
6	IO_L08N_6	AL26		
6	IO_L09P_6	AM28		
6	IO_L09N_6/VREF_6	AM29		
6	IO_L10P_6	AL33		
6	IO_L10N_6	AL34		
6	IO_L11P_6	AL27		
6	IO_L11N_6	AK27		
6	IO_L12P_6	AL29		
6	IO_L12N_6	AL30		
6	IO_L13P_6	AL32		
6	IO_L13N_6	AK32		
6	IO_L14P_6	AJ27		
6	IO_L14N_6	AJ28		
6	IO_L15P_6	AL31		
6	IO_L15N_6/VREF_6	AK31		
6	IO_L16P_6	AL28		
6	IO_L16N_6	AK28		
6	IO_L17P_6	AJ26		
6	IO_L17N_6	AH26		
6	IO_L18P_6	AJ33		
6	IO_L18N_6	AJ34		
6	IO_L19P_6	AJ31		
6	IO_L19N_6	AJ32		
6	IO_L20P_6	AG27		
6	IO_L20N_6	AG28		
6	IO_L21P_6	AK29		
6	IO_L21N_6/VREF_6	AJ29		
6	IO_L22P_6	AH33		
6	IO_L22N_6	AH34		
6	IO_L23P_6	AF27		
6	IO_L23N_6	AE27		
6	IO_L24P_6	AJ30		
6	IO_L24N_6	AH30		
6	IO_L25P_6	AH28		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L87P_4/VREF_4		AP15	NC	
4	IO_L37N_4		AV15		
4	IO_L37P_4		AU15		
4	IO_L38N_4		AY14		
4	IO_L38P_4		AY15		
4	IO_L39N_4		AM16		
4	IO_L39P_4		AL16		
4	IO_L43N_4		AP16		
4	IO_L43P_4		AN16		
4	IO_L44N_4		AR16		
4	IO_L44P_4		AT16		
4	IO_L45N_4		AV16		
4	IO_L45P_4/VREF_4		AU16		
4	IO_L46N_4		AL18		
4	IO_L46P_4		AL17		
4	IO_L47N_4		AM17		
4	IO_L47P_4		AN17		
4	IO_L48N_4		AR17		
4	IO_L48P_4		AP17		
4	IO_L49N_4		AU17		
4	IO_L49P_4		AT17		
4	IO_L50_4/No_Pair		AW16		
4	IO_L53_4/No_Pair		AW17		
4	IO_L54N_4		AN18		
4	IO_L54P_4		AM18		
4	IO_L55N_4		AT18		
4	IO_L55P_4		AR18		
4	IO_L56N_4		AV17		
4	IO_L56P_4		AV18		
4	IO_L57N_4		AY18		
4	IO_L57P_4/VREF_4		AY17		
4	IO_L58N_4		AM19		
4	IO_L58P_4		AL19		
4	IO_L59N_4		AP19		
4	IO_L59P_4		AN19		
4	IO_L60N_4		AT19		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD17		BB15		
N/A	GNDA17		AY16		
N/A	TXPPAD17		BB16		
N/A	TXNPAD17		BB17		
N/A	VTTXPAD17		BA17		
N/A	AVCCAUXTX17		BA16		
N/A	AVCCAUXRX18		BA18		
N/A	VTRXPAD18		BA19		
N/A	RXNPAD18		BB18		
N/A	RXPPAD18		BB19		
N/A	GNDA18		AY21		
N/A	TXPPAD18		BB20		
N/A	TXNPAD18		BB21		
N/A	VTTXPAD18		BA21		
N/A	AVCCAUXTX18		BA20		
N/A	AVCCAUXRX19		BA22		
N/A	VTRXPAD19		BA23		
N/A	RXNPAD19		BB22		
N/A	RXPPAD19		BB23		
N/A	GNDA19		AY22		
N/A	TXPPAD19		BB24		
N/A	TXNPAD19		BB25		
N/A	VTTXPAD19		BA25		
N/A	AVCCAUXTX19		BA24		
N/A	AVCCAUXRX20		BA26		
N/A	VTRXPAD20		BA27		
N/A	RXNPAD20		BB26		
N/A	RXPPAD20		BB27		
N/A	GNDA20		AY27		
N/A	TXPPAD20		BB28		
N/A	TXNPAD20		BB29		
N/A	VTTXPAD20		BA29		
N/A	AVCCAUXTX20		BA28		
N/A	AVCCAUXRX21		BA30		
N/A	VTRXPAD21		BA31		
N/A	RXNPAD21		BB30		

FF1696 Flip-Chip Fine-Pitch BGA Package

As shown in Table 14, XC2VP100 Virtex-II Pro devices are available in the FF1696 flip-chip fine-pitch BGA package. Following this table are the FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L01N_0/VRP_0	E33	
0	IO_L01P_0/VRN_0	F33	
0	IO_L02N_0	K32	
0	IO_L02P_0	L32	
0	IO_L03N_0	C32	
0	IO_L03P_0/VREF_0	C33	
0	IO_L05_0/No_Pair	G33	
0	IO_L06N_0	A33	
0	IO_L06P_0	B33	
0	IO_L07N_0	F32	
0	IO_L07P_0	G32	
0	IO_L08N_0	H32	
0	IO_L08P_0	J32	
0	IO_L09N_0	D32	
0	IO_L09P_0/VREF_0	E32	
0	IO_L19N_0	A32	
0	IO_L19P_0	B32	
0	IO_L20N_0	K31	
0	IO_L20P_0	L31	
0	IO_L21N_0	H30	
0	IO_L21P_0	G31	
0	IO_L25N_0	E31	
0	IO_L25P_0	F31	
0	IO_L26N_0	H31	
0	IO_L26P_0	J31	
0	IO_L27N_0	D30	
0	IO_L27P_0/VREF_0	D31	
0	IO_L28N_0	B31	
0	IO_L28P_0	C31	
0	IO_L29N_0	K30	
0	IO_L29P_0	L30	
0	IO_L30N_0	F30	
0	IO_L30P_0	G30	
0	IO_L34N_0	B30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L40P_2	R5	
2	IO_L41N_2	V6	
2	IO_L41P_2	V7	
2	IO_L42N_2	R3	
2	IO_L42P_2	P3	
2	IO_L43N_2	R1	
2	IO_L43P_2	R2	
2	IO_L44N_2	W10	
2	IO_L44P_2	W11	
2	IO_L45N_2	T7	
2	IO_L45P_2	R7	
2	IO_L46N_2/VREF_2	T4	
2	IO_L46P_2	T5	
2	IO_L47N_2	W9	
2	IO_L47P_2	Y10	
2	IO_L48N_2	T1	
2	IO_L48P_2	T2	
2	IO_L49N_2	U6	
2	IO_L49P_2	T6	
2	IO_L50N_2	W7	
2	IO_L50P_2	Y8	
2	IO_L51N_2	U4	
2	IO_L51P_2	T3	
2	IO_L52N_2/VREF_2	U2	
2	IO_L52P_2	U3	
2	IO_L53N_2	Y11	
2	IO_L53P_2	Y12	
2	IO_L54N_2	V4	
2	IO_L54P_2	V5	
2	IO_L55N_2	V1	
2	IO_L55P_2	V2	
2	IO_L56N_2	Y6	
2	IO_L56P_2	Y7	
2	IO_L57N_2	W5	
2	IO_L57P_2	W6	
2	IO_L58N_2/VREF_2	W3	
2	IO_L58P_2	V3	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L45N_7	T36	
7	IO_L44P_7	W32	
7	IO_L44N_7	W33	
7	IO_L43P_7	R41	
7	IO_L43N_7	R42	
7	IO_L42P_7	P40	
7	IO_L42N_7	R40	
7	IO_L41P_7	V36	
7	IO_L41N_7	V37	
7	IO_L40P_7	R38	
7	IO_L40N_7/VREF_7	R39	
7	IO_L39P_7	P38	
7	IO_L39N_7	R37	
7	IO_L38P_7	V34	
7	IO_L38N_7	V35	
7	IO_L37P_7	P41	
7	IO_L37N_7	P42	
7	IO_L36P_7	P36	
7	IO_L36N_7	P37	
7	IO_L35P_7	V32	
7	IO_L35N_7	V33	
7	IO_L34P_7	M41	
7	IO_L34N_7/VREF_7	N41	
7	IO_L33P_7	N39	
7	IO_L33N_7	N40	
7	IO_L32P_7	U35	
7	IO_L32N_7	U36	
7	IO_L31P_7	N36	
7	IO_L31N_7	N37	
7	IO_L30P_7	M39	
7	IO_L30N_7	M40	
7	IO_L29P_7	U32	
7	IO_L29N_7	U33	
7	IO_L28P_7	M37	
7	IO_L28N_7/VREF_7	M38	
7	IO_L27P_7	L37	
7	IO_L27N_7	M36	