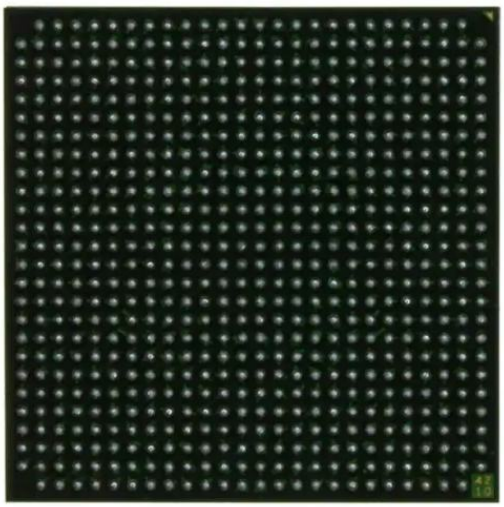

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5ff672c

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

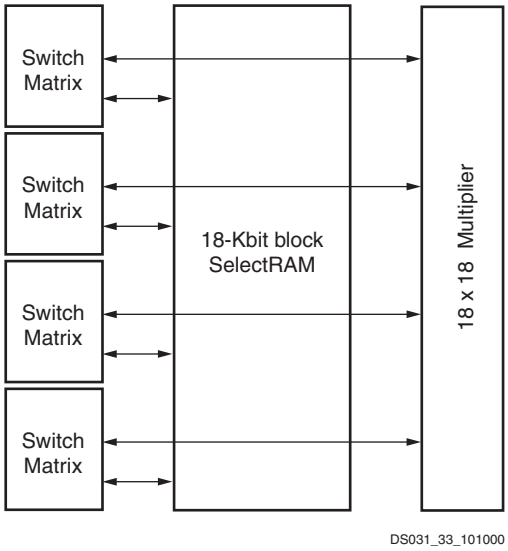

Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

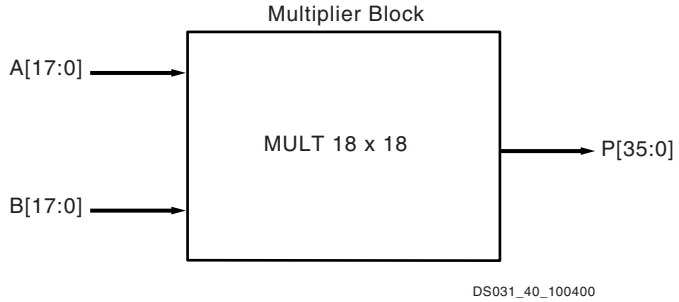

Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Figure 57 shows clock distribution in Virtex-II Pro devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). To reduce power consumption, any unused clock branches remain static.

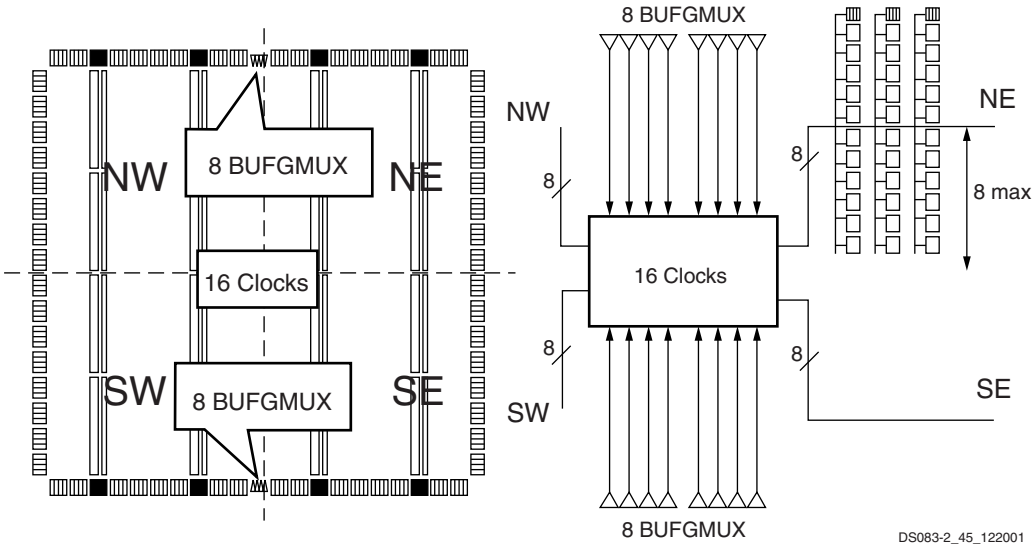

Figure 57: **Virtex-II Pro Clock Distribution**

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 58.

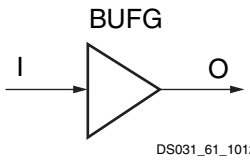

Figure 58: **Virtex-II Pro BUFG Function**

The Virtex-II Pro global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 59), as well as a two-input clock multiplexer (Figure 60). A functional description of these two options is provided below. Each of them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE and S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

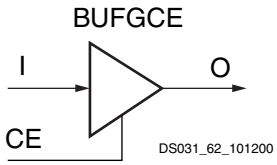

Figure 59: **Virtex-II Pro BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I_0 input, a High on S selects the I_1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect.

synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as DCI.

Readback

In this mode, configuration data from the Virtex-II Pro FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM+, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II Pro Platform FPGA User Guide.*

Bitstream Encryption

Virtex-II Pro devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II Pro devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the ***Virtex-II Pro Platform FPGA User Guide***. Your local FAE can also provide specific information on this feature.

Partial Reconfiguration

Partial reconfiguration of Virtex-II Pro devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

For more information on Partial Reconfiguration in Virtex-II Pro devices, please refer to Xilinx Application Note **XAPP290**, *Two Flows for Partial Reconfiguration*.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	• Revised Reset and Power sections. • Updated Table 8, which lists compatible input standards. [Table deleted in v2.6.] • Added Figure 28, Figure 29, and Figure 30, which provide examples illustrating the use of I/O standards.
09/27/02	2.2	• In section RocketIO Overview, corrected max number of MGTs from 16 to 24. • In section Input/Output Blocks (IOBs), added references to XAPP653 regarding implementation of 3.3V I/O standards.
11/20/02	2.3	• Table 8: Added rows for LVTTL, LVCMOS33, and PCI-X. • Table 8: Added LVTTL and LVCMOS33 to compatible 3.3V cells. [Table deleted in v2.6.] • Table 33: Correct bitstream lengths.
12/03/02	2.4	• Added mention of LVTTL and PCI with respect to SelectIO-Ultra configurations. See section Input/Output Individual Options and Figure 22.
01/20/03	2.5	• Added qualification to features vs. Virtex-II (open-drain output pin TDO does not have internal pull-up resistor) • Table 7: Added HSTL18 (I, II, III, & IV) and HSTL18_DCI (I,II, III & IV) to 1.8V VCCO row. [Table deleted in v2.6.] • Table 8: Numerous revisions. [Table deleted in v2.6.]

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: **Processor Clocks Absolute AC Characteristics**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	400(1)	0	350(1)	0	300	MHz
JTAGC405TCK frequency(2)	0	200	0	175	0	150	MHz
PLBCLK(3)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(3)	0	400	0	350	0	300	MHz
BRAMISOCMCLK(3)	0	400	0	350	0	300	MHz

Notes:

1. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1, Module 1 to identify dual-processor devices.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PowerPC 405 Processor Block Reference Guide*** and **XAPP640** for more information.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
1	IO_L02N_1	C13
1	IO_L02P_1	B14
1	IO_L01N_1/VRP_1	C14
1	IO_L01P_1/VRN_1	C15
2	IO_L01N_2/VRP_2	E14
2	IO_L01P_2/VRN_2	E15
2	IO_L02N_2	E13
2	IO_L02P_2	F12
2	IO_L03N_2	F13
2	IO_L03P_2	F14
2	IO_L04N_2/VREF_2	F15
2	IO_L04P_2	F16
2	IO_L06N_2	G13
2	IO_L06P_2	G14
2	IO_L85N_2	G15
2	IO_L85P_2	G16
2	IO_L86N_2	G12
2	IO_L86P_2	H13
2	IO_L88N_2/VREF_2	H14
2	IO_L88P_2	H15
2	IO_L90N_2	H16
2	IO_L90P_2	J16
3	IO_L90N_3	J15
3	IO_L90P_3	J14
3	IO_L89N_3	J13
3	IO_L89P_3	K12
3	IO_L87N_3/VREF_3	K16
3	IO_L87P_3	K15
3	IO_L85N_3	K14
3	IO_L85P_3	K13
3	IO_L06N_3	L16
3	IO_L06P_3	L15
3	IO_L05N_3	L14

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/BUSY/DOUT(1)	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0/DIN(1)	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	V19				
N/A	GND	V20				
N/A	GND	V21				
N/A	GND	W1				
N/A	GND	W14				
N/A	GND	W15				
N/A	GND	W16				
N/A	GND	W17				
N/A	GND	W18				
N/A	GND	W19				
N/A	GND	W20				
N/A	GND	W21				
N/A	GND	W34				
N/A	GND	Y8				
N/A	GND	Y14				
N/A	GND	Y15				
N/A	GND	Y16				
N/A	GND	Y17				
N/A	GND	Y18				
N/A	GND	Y19				
N/A	GND	Y20				
N/A	GND	Y21				
N/A	GND	Y27				
N/A	GND	AA14				
N/A	GND	AA15				
N/A	GND	AA16				
N/A	GND	AA17				
N/A	GND	AA18				
N/A	GND	AA19				
N/A	GND	AA20				
N/A	GND	AA21				
N/A	GND	AC5				
N/A	GND	AC8				
N/A	GND	AC27				
N/A	GND	AC30				
N/A	GND	AE3				
N/A	GND	AE32				
N/A	GND	H23				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L34P_0	E27	NC	
0	IO_L35N_0	L26	NC	
0	IO_L35P_0	L25	NC	
0	IO_L36N_0	G26	NC	
0	IO_L36P_0/VREF_0	H26	NC	
0	IO_L37N_0	E26		
0	IO_L37P_0	F26		
0	IO_L38N_0	K25		
0	IO_L38P_0	K24		
0	IO_L39N_0	C26		
0	IO_L39P_0	D26		
0	IO_L43N_0	H25		
0	IO_L43P_0	J25		
0	IO_L44N_0	M25		
0	IO_L44P_0	M24		
0	IO_L45N_0	F25		
0	IO_L45P_0/VREF_0	G25		
0	IO_L46N_0	C25		
0	IO_L46P_0	D25		
0	IO_L47N_0	L23		
0	IO_L47P_0	M22		
0	IO_L48N_0	H24		
0	IO_L48P_0	J24		
0	IO_L49N_0	E25		
0	IO_L49P_0	E24		
0	IO_L50_0/No_Pair	N23		
0	IO_L53_0/No_Pair	M23		
0	IO_L54N_0	H23		
0	IO_L54P_0	J23		
0	IO_L55N_0	F24		
0	IO_L55P_0	G23		
0	IO_L56N_0	K22		
0	IO_L56P_0	L22		
0	IO_L57N_0	C23		
0	IO_L57P_0/VREF_0	D23		
0	IO_L58N_0	H22		
0	IO_L58P_0	J22		
0	IO_L59N_0	N22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L04P_6	AR33		
6	IO_L04N_6	AP33		
6	IO_L05P_6	AM32		
6	IO_L05N_6	AL31		
6	IO_L06P_6	AT34		
6	IO_L06N_6	AR34		
6	IO_L73P_6	AU35	NC	
6	IO_L73N_6	AT35	NC	
6	IO_L75P_6	AT38	NC	
6	IO_L75N_6/VREF_6	AT39	NC	
6	IO_L76P_6	AR37	NC	
6	IO_L76N_6	AR38	NC	
6	IO_L78P_6	AP38	NC	
6	IO_L78N_6	AP39	NC	
6	IO_L79P_6	AP36	NC	
6	IO_L79N_6	AP37	NC	
6	IO_L81P_6	AP35	NC	
6	IO_L81N_6/VREF_6	AN35	NC	
6	IO_L82P_6	AN38	NC	
6	IO_L82N_6	AN39	NC	
6	IO_L84P_6	AN36	NC	
6	IO_L84N_6	AN37	NC	
6	IO_L07P_6	AN33		
6	IO_L07N_6	AN34		
6	IO_L08P_6	AK31		
6	IO_L08N_6	AK32		
6	IO_L09P_6	AM37		
6	IO_L09N_6/VREF_6	AM38		
6	IO_L10P_6	AM36		
6	IO_L10N_6	AL35		
6	IO_L11P_6	AJ31		
6	IO_L11N_6	AH30		
6	IO_L12P_6	AM33		
6	IO_L12N_6	AM34		
6	IO_L13P_6	AL38		
6	IO_L13N_6	AL39		
6	IO_L14P_6	AH29		
6	IO_L14N_6	AG29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	AU3		
N/A	GND	AT3		
N/A	GND	D3		
N/A	GND	C3		
N/A	GND	B3		
N/A	GND	AN12		
N/A	GND	G12		
N/A	GND	C12		
N/A	GND	Y10		
N/A	GND	AH9		
N/A	GND	AD9		
N/A	GND	T9		
N/A	GND	M9		
N/A	GND	AU8		
N/A	GND	AN8		
N/A	GND	G8		
N/A	GND	C8		
N/A	GND	Y6		
N/A	GND	AM5		
N/A	GND	AH5		
N/A	GND	T17		
N/A	GND	AT16		
N/A	GND	AN16		
N/A	GND	AJ16		
N/A	GND	AC16		
N/A	GND	AB16		
N/A	GND	AA16		
N/A	GND	Y16		
N/A	GND	W16		
N/A	GND	V16		
N/A	GND	U16		
N/A	GND	L16		
N/A	GND	G16		
N/A	GND	D16		
N/A	GND	AU12		
N/A	GND	AB18		
N/A	GND	AA18		
N/A	GND	Y18		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L26P_2		N12		
2	IO_L27N_2		P9		
2	IO_L27P_2		P10		
2	IO_L28N_2/VREF_2		P7		
2	IO_L28P_2		P8		
2	IO_L29N_2		P11		
2	IO_L29P_2		P12		
2	IO_L30N_2		P5		
2	IO_L30P_2		P6		
2	IO_L31N_2		P1		
2	IO_L31P_2		P2		
2	IO_L32N_2		R9		
2	IO_L32P_2		R10		
2	IO_L33N_2		R5		
2	IO_L33P_2		R6		
2	IO_L34N_2/VREF_2		P3		
2	IO_L34P_2		R3		
2	IO_L35N_2		R1		
2	IO_L35P_2		R2		
2	IO_L36N_2		R11		
2	IO_L36P_2		R12		
2	IO_L37N_2		T6		
2	IO_L37P_2		T7		
2	IO_L38N_2		T8		
2	IO_L38P_2		R8		
2	IO_L39N_2		T4		
2	IO_L39P_2		T5		
2	IO_L40N_2/VREF_2		T2		
2	IO_L40P_2		T3		
2	IO_L41N_2		T10		
2	IO_L41P_2		T11		
2	IO_L42N_2		U7		
2	IO_L42P_2		U8		
2	IO_L43N_2		U5		
2	IO_L43P_2		U6		
2	IO_L44N_2		U9		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AB18		
N/A	GND		AB17		
N/A	GND		AB11		
N/A	GND		AB8		
N/A	GND		AB5		
N/A	GND		AC41		
N/A	GND		AC26		
N/A	GND		AC25		
N/A	GND		AC24		
N/A	GND		AC23		
N/A	GND		AC22		
N/A	GND		AC21		
N/A	GND		AC20		
N/A	GND		AC19		
N/A	GND		AC18		
N/A	GND		AC17		
N/A	GND		AC2		
N/A	GND		AD26		
N/A	GND		AD25		
N/A	GND		AD24		
N/A	GND		AD23		
N/A	GND		AD22		
N/A	GND		AD21		
N/A	GND		AD20		
N/A	GND		AD19		
N/A	GND		AD18		
N/A	GND		AD17		
N/A	GND		AE37		
N/A	GND		AE34		
N/A	GND		AE26		
N/A	GND		AE25		
N/A	GND		AE24		
N/A	GND		AE23		
N/A	GND		AE22		
N/A	GND		AE21		
N/A	GND		AE20		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L56N_3	AC11	
3	IO_L56P_3	AC12	
3	IO_L55N_3	AD3	
3	IO_L55P_3	AE3	
3	IO_L54N_3	AE1	
3	IO_L54P_3	AE2	
3	IO_L53N_3	AC6	
3	IO_L53P_3	AC7	
3	IO_L52N_3	AF2	
3	IO_L52P_3	AF3	
3	IO_L51N_3/VREF_3	AF6	
3	IO_L51P_3	AG6	
3	IO_L50N_3	AD10	
3	IO_L50P_3	AD11	
3	IO_L49N_3	AG4	
3	IO_L49P_3	AG5	
3	IO_L48N_3	AF4	
3	IO_L48P_3	AG3	
3	IO_L47N_3	AC10	
3	IO_L47P_3	AD9	
3	IO_L46N_3	AG1	
3	IO_L46P_3	AG2	
3	IO_L45N_3/VREF_3	AG7	
3	IO_L45P_3	AH7	
3	IO_L44N_3	AC8	
3	IO_L44P_3	AD7	
3	IO_L43N_3	AH4	
3	IO_L43P_3	AH5	
3	IO_L42N_3	AH1	
3	IO_L42P_3	AH2	
3	IO_L41N_3	AE10	
3	IO_L41P_3	AE11	
3	IO_L40N_3	AJ6	
3	IO_L40P_3	AJ7	
3	IO_L39N_3/VREF_3	AH6	
3	IO_L39P_3	AJ5	
3	IO_L38N_3	AE8	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L58P_4	AW19	
4	IO_L59N_4	AP19	
4	IO_L59P_4	AN19	
4	IO_L60N_4	BB19	
4	IO_L60P_4	BA19	
4	IO_L64N_4	AU20	
4	IO_L64P_4	AT20	
4	IO_L65N_4	AL21	
4	IO_L65P_4	AL20	
4	IO_L66N_4	BA20	
4	IO_L66P_4/VREF_4	AY20	
4	IO_L67N_4	AR21	
4	IO_L67P_4	AP21	
4	IO_L68N_4	AN20	
4	IO_L68P_4	AM20	
4	IO_L69N_4	AU21	
4	IO_L69P_4/VREF_4	AT21	
4	IO_L73N_4	AW21	
4	IO_L73P_4	AV21	
4	IO_L74N_4/GCLK3S	AN21	
4	IO_L74P_4/GCLK2P	AM21	
4	IO_L75N_4/GCLK1S	BA21	
4	IO_L75P_4/GCLK0P	AY21	
5	IO_L75N_5/GCLK7S	AY22	
5	IO_L75P_5/GCLK6P	BA22	
5	IO_L74N_5/GCLK5S	AM22	
5	IO_L74P_5/GCLK4P	AN22	
5	IO_L73N_5	AV22	
5	IO_L73P_5	AW22	
5	IO_L69N_5/VREF_5	AT22	
5	IO_L69P_5	AU22	
5	IO_L68N_5	AM23	
5	IO_L68P_5	AN23	
5	IO_L67N_5	AP22	
5	IO_L67P_5	AR22	
5	IO_L66N_5/VREF_5	AY23	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L34P_5	AU30	
5	IO_L30N_5	AM30	
5	IO_L30P_5	AN30	
5	IO_L29N_5	AY31	
5	IO_L29P_5	BA31	
5	IO_L28N_5	AW31	
5	IO_L28P_5	AW30	
5	IO_L27N_5/VREF_5	AP31	
5	IO_L27P_5	AR31	
5	IO_L26N_5	AU31	
5	IO_L26P_5	AV31	
5	IO_L25N_5	AT31	
5	IO_L25P_5	AR30	
5	IO_L21N_5	AM31	
5	IO_L21P_5	AN31	
5	IO_L20N_5	BA32	
5	IO_L20P_5	BB32	
5	IO_L19N_5	AV32	
5	IO_L19P_5	AW32	
5	IO_L09N_5/VREF_5	AP32	
5	IO_L09P_5	AR32	
5	IO_L08N_5	AT32	
5	IO_L08P_5	AU32	
5	IO_L07N_5/VREF_5	BA33	
5	IO_L07P_5	BB33	
5	IO_L06N_5/VRP_5	AY33	
5	IO_L06P_5/VRN_5	AY32	
5	IO_L05_5/No_Pair	AT33	
5	IO_L03N_5/D4	AM32	
5	IO_L03P_5/D5	AN32	
5	IO_L02N_5/D6	AU33	
5	IO_L02P_5/D7	AV33	
5	IO_L01N_5/RDWR_B	AL31	
5	IO_L01P_5/CS_B	AL32	
6	IO_L01P_6/VRN_6	BB39	
6	IO_L01N_6/VRP_6	BA39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	E13	
N/A	GND	A13	
N/A	GND	AD12	
N/A	GND	W12	
N/A	GND	BB9	
N/A	GND	AV9	
N/A	GND	AP9	
N/A	GND	AK9	
N/A	GND	AF9	
N/A	GND	AC9	
N/A	GND	Y9	
N/A	GND	U9	
N/A	GND	N9	
N/A	GND	J9	
N/A	GND	E9	
N/A	GND	A9	
N/A	GND	BB5	
N/A	GND	AV5	
N/A	GND	AP5	
N/A	GND	AK5	
N/A	GND	AF5	
N/A	GND	AC5	
N/A	GND	Y5	
N/A	GND	U5	
N/A	GND	N5	
N/A	GND	J5	
N/A	GND	E5	
N/A	GND	A5	
N/A	GND	BA3	
N/A	GND	B3	
N/A	GND	BA2	
N/A	GND	AY2	
N/A	GND	C2	
N/A	GND	B2	
N/A	GND	AV1	
N/A	GND	AP1	
N/A	GND	AK1	