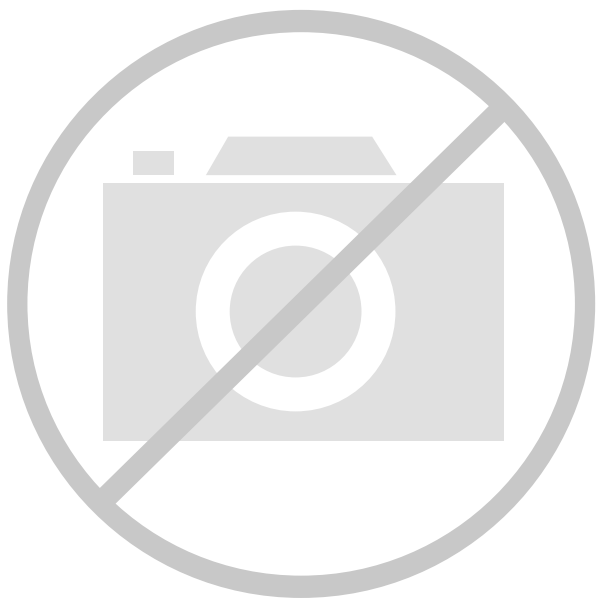




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5ff896c

Revision History

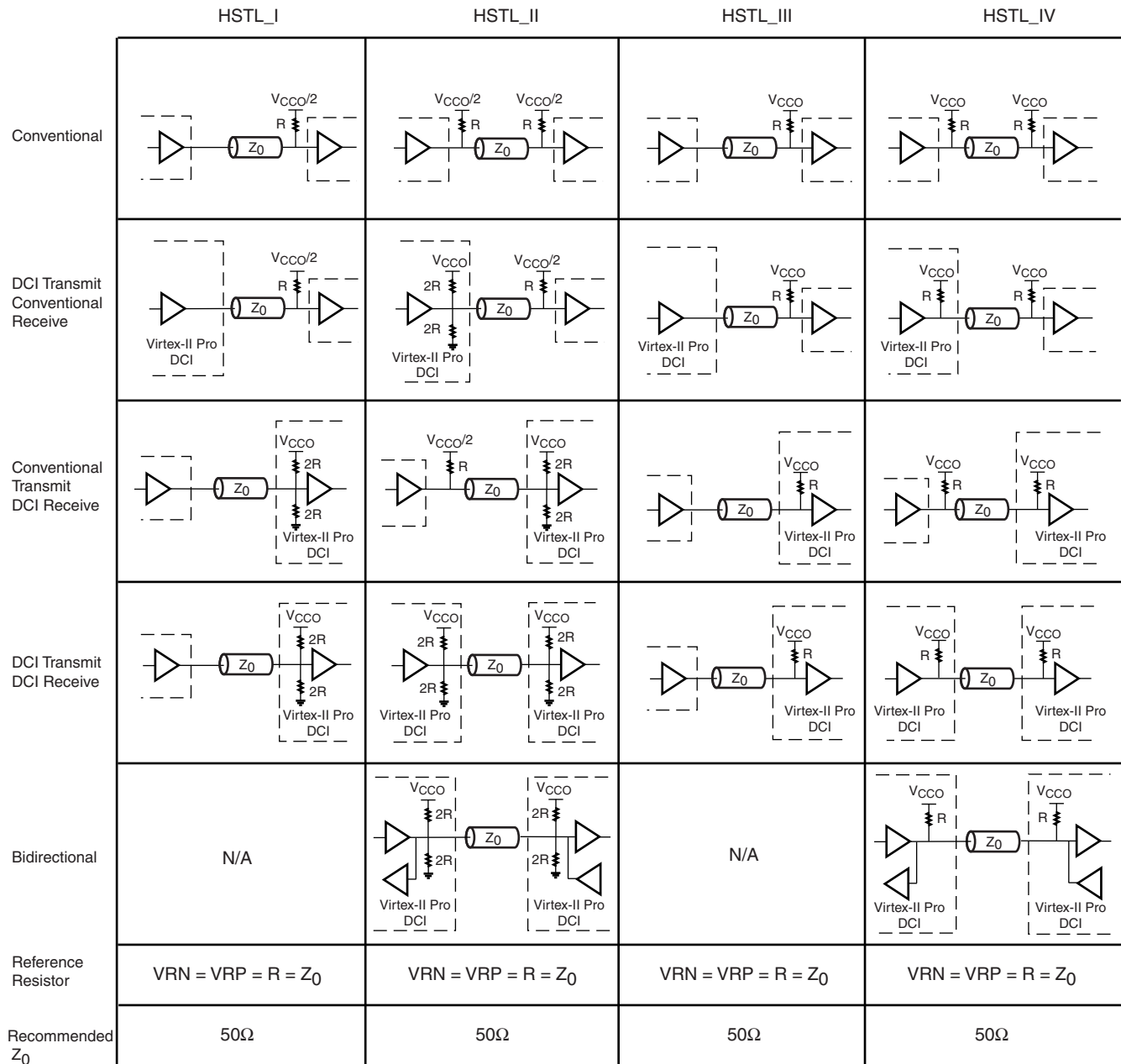
This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile v1.62 .
09/03/02	2.1	Updates to Table 1 and Table 3 . Processor Block information added to Table 4 .
09/27/02	2.2	In Table 1 , correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	- In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. - Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	- Correct number of single-ended I/O standards from 19 to 22. - Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to Production status.
02/19/04	3.1	Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. - Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. - Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	<i>No changes in Module 1 for this revision.</i>
03/01/05	4.2	Table 3 : Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	<i>No changes in Module 1 for this revision.</i>
09/15/05	4.4	- Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. - Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	- Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. - Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	<i>No changes in Module 1 for this revision.</i>
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added <i>Product Not Recommended for New Designs</i> banner.

Table 15: SelectIO-Ultra Differential Buffers With On-Chip Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).



DS083-2_65a_082102

Figure 28: HSTL DCI Usage Examples

Figure 30 provides examples illustrating the use of the LVDS_25_DCI and LVDSEXT_25_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).

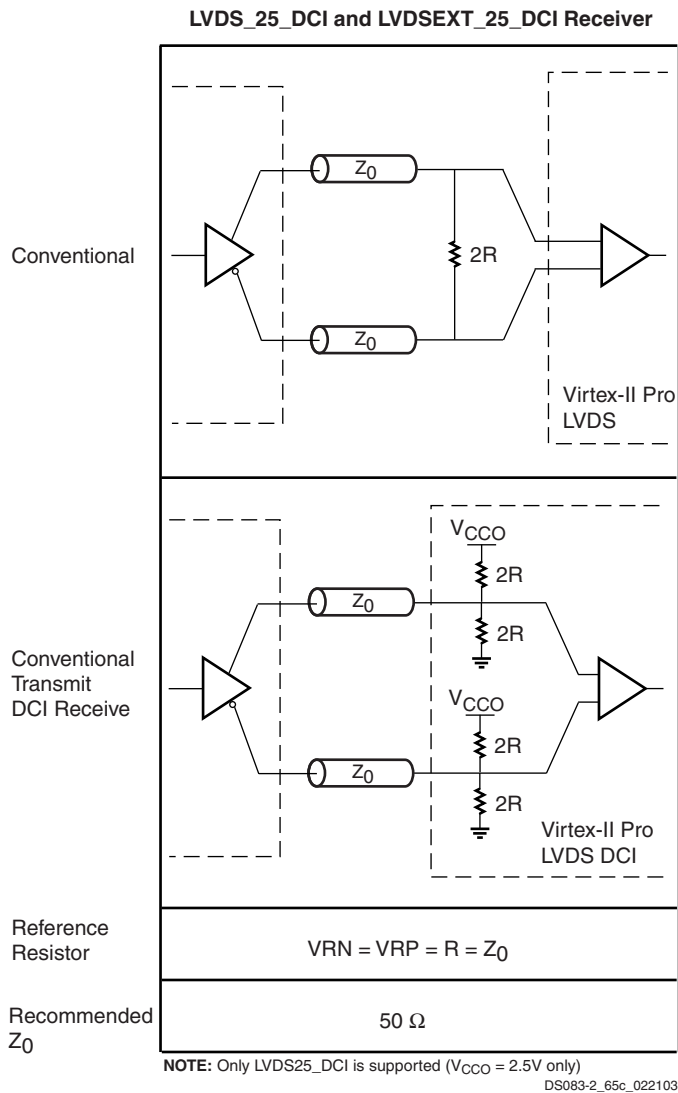


Figure 30: LVDS DCI Usage Examples

On-Chip Differential Termination

Virtex-II Pro provides a true $100\ \Omega$ differential termination (DT) across the input differential receiver terminals. The LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT I/O standards. For further details, refer to [Solution Record 17244](#). Also see the [Virtex-II Pro Platform FPGA User Guide](#) for more design information.

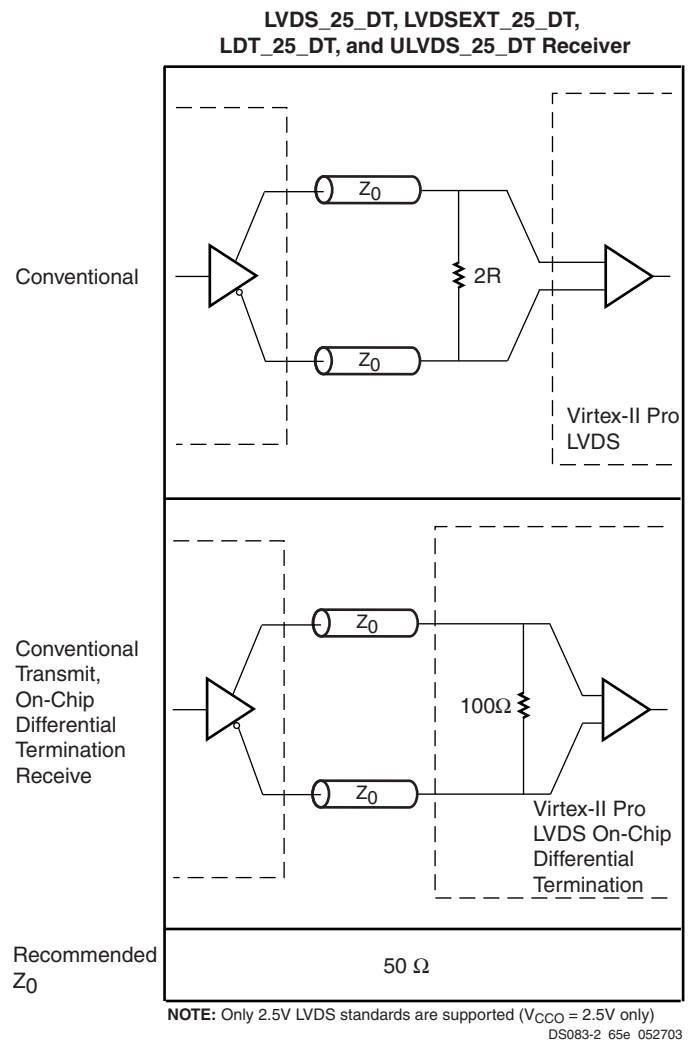


Figure 31: LVDS Differential Termination Usage Examples

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 39**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

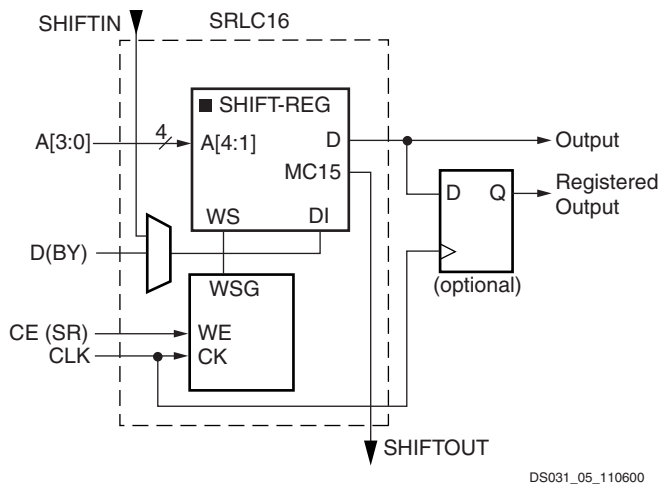


Figure 39: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 40**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

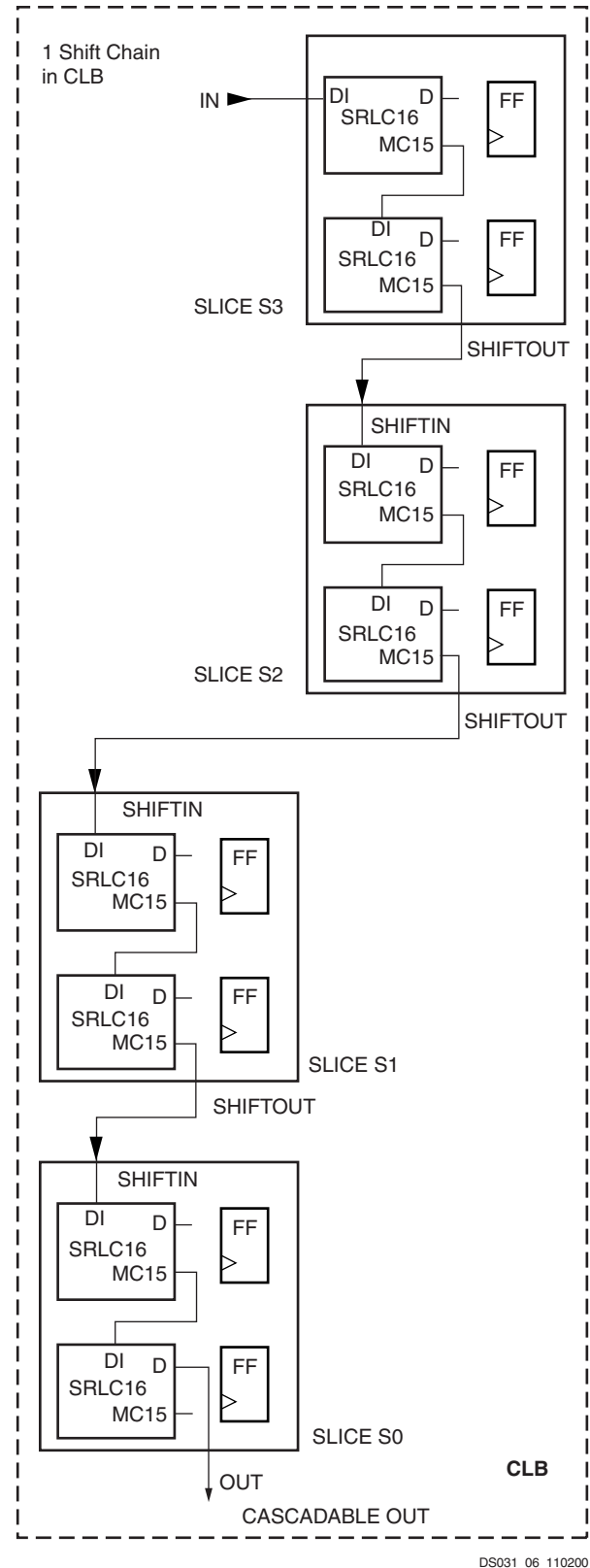


Figure 40: Cascadable Shift Register

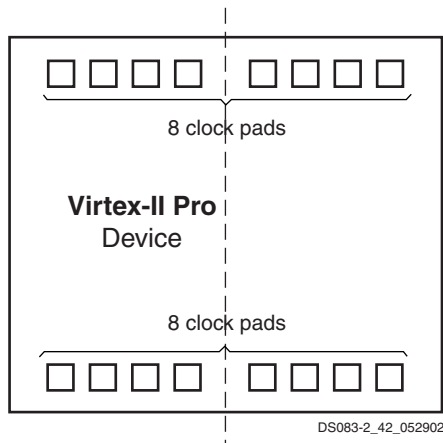


Figure 55: Virtex-II Pro Clock Pads

Each global clock multiplexer buffer can be driven either by the clock pad to distribute a clock directly to the device, or by the Digital Clock Manager (DCM), discussed in [Digital Clock Manager \(DCM\)](#), page 51. Each global clock multiplexer buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock multiplexer buffer inputs, as shown in [Figure 56](#).

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM+ blocks).

Eight global clocks can be used in each quadrant of the Virtex-II Pro device. Designers should consider the clock distribution detail of the device prior to pin-locking and floor-planning. (See the *Virtex-II Pro Platform FPGA User Guide*.)

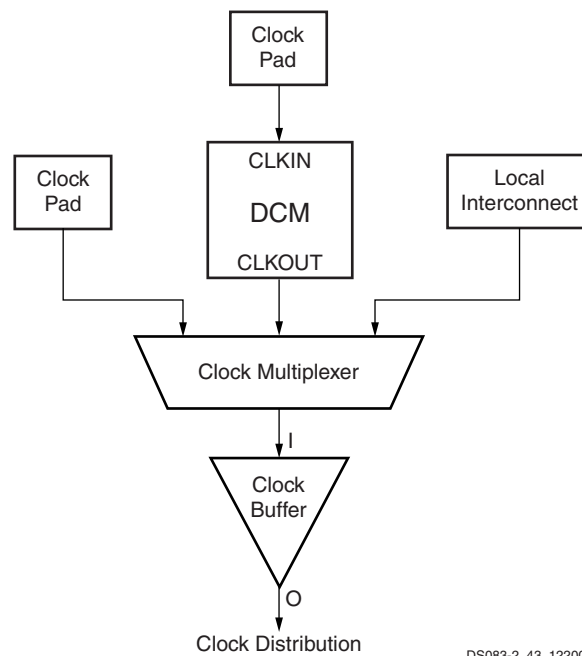


Figure 56: Virtex-II Pro Clock Multiplexer Buffer Configuration

Table 4: Quiescent Supply Current

Symbol	Description	Device	Typ ⁽¹⁾	Max	Units
I _{CCINTQ}	Quiescent V _{CCINT} supply current	XC2VP2	20	300	mA
		XC2VP4	30	400	mA
		XC2VP7	35	500	mA
		XC2VP20	40	600	mA
		XC2VPX20	40	600	mA
		XC2VP30	50	800	mA
		XC2VP40	60	1050	mA
		XC2VP50	70	1250	mA
		XC2VP70	85	1700	mA
		XC2VPX70	85	1700	mA
		XC2VP100	100	2200	mA
I _{CCOQ}	Quiescent V _{CCO} supply current	XC2VP2	1.0	8.0	mA
		XC2VP4	1.0	8.0	mA
		XC2VP7	1.0	8.0	mA
		XC2VP20	1.25	10	mA
		XC2VPX20	1.25	10	mA
		XC2VP30	1.25	10	mA
		XC2VP40	1.25	10	mA
		XC2VP50	1.5	12	mA
		XC2VP70	1.5	12	mA
		XC2VPX70	1.5	12	mA
		XC2VP100	1.75	15	mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC2VP2	5	50	mA
		XC2VP4	5	50	mA
		XC2VP7	5	50	mA
		XC2VP20	10	75	mA
		XC2VPX20	10	75	mA
		XC2VP30	10	75	mA
		XC2VP40	10	75	mA
		XC2VP50	20	100	mA
		XC2VP70	20	100	mA
		XC2VPX70	20	100	mA
		XC2VP100	20	125	mA

Notes:

1. Typical values are specified at nominal voltage, 25° C.
2. Quiescent current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
3. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
4. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™.

CLB Distributed RAM Switching Characteristics

Table 43: CLB Distributed RAM Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	T _{SHCKO16}	1.25	1.38	1.54	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	T _{SHCKO32}	1.57	1.75	1.95	ns, max
Clock CLK to F5 output	T _{SHCKOF5}	1.52	1.68	1.88	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T _{DS} /T _{DH}	0.38/−0.07	0.41/−0.07	0.46/−0.08	ns, min
F/G address inputs	T _{AS} /T _{AH}	0.42/ 0.00	0.47/ 0.00	0.52/ 0.00	ns, min
SR input	T _{WES} /T _{WEH}	0.22/ 0.04	0.24/ 0.05	0.26/ 0.05	ns, min
Clock CLK					
Minimum Pulse Width, High	T _{WPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T _{WPL}	0.63	0.72	0.79	ns, min
Minimum clock period to meet address write cycle time	T _{WC}	1.25	1.44	1.58	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 44: CLB Shift Register Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Sequential Delays					
Clock CLK to X/Y outputs	T _{REG}	2.78	3.12	3.49	ns, max
Clock CLK to X/Y outputs	T _{REG32}	3.10	3.49	3.90	ns, max
Clock CLK to XB output via MC15 LUT output	T _{REGXB}	2.84	3.18	3.55	ns, max
Clock CLK to YB output via MC15 LUT output	T _{REGYB}	2.55	2.88	3.21	ns, max
Clock CLK to Shiftout	T _{CKSH}	2.50	2.83	3.15	ns, max
Clock CLK to F5 output	T _{REGF5}	3.05	3.42	3.83	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T _{SRLDS} /T _{SRLDH}	0.70/−0.16	0.77/−0.18	0.98/−0.21	ns, min
SR input	T _{WSS} /T _{WSH}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T _{SRPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T _{SRPL}	0.63	0.72	0.79	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in [Figure 7](#); corresponding timing characteristics are listed in [Table 49](#).

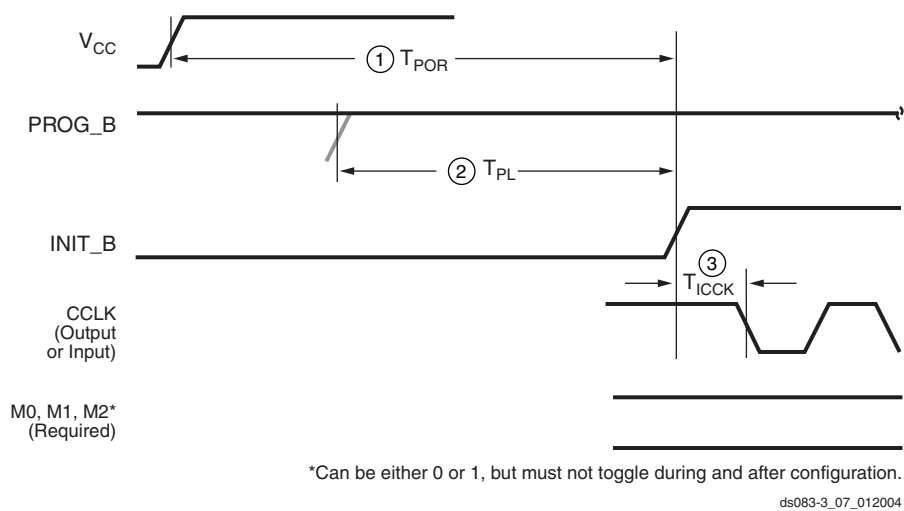


Figure 7: Configuration Power-Up Timing

Table 49: Power-Up Timing Characteristics

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	$T_{PL} + 2$	ms, max
Program latency	2	T_{PL}	4	μ s per frame, max
CCLK (output) delay	3	T_{ICCK}	0.25	μ s, min
			4.00	μ s, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:

- The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX} . The mode pins should not be toggled during and after configuration.

Miscellaneous Timing Parameters

Table 61: Miscellaneous Timing Parameters

			Speed Grade			
Description	Symbol	Constraints F _{CLKIN}	-7	-6	-5	Units
Time Required to Achieve LOCK						
Using DLL outputs ⁽¹⁾	LOCK_DLL:					
	LOCK_DLL_60	> 60MHz	20.00	20.00	20.00	us
	LOCK_DLL_50_60	50 - 60 MHz	25.00	25.00	25.00	us
	LOCK_DLL_40_50	40 - 50 MHz	50.00	50.00	50.00	us
	LOCK_DLL_30_40	30 - 40 MHz	90.00	90.00	90.00	us
	LOCK_DLL_24_30	24 - 30 MHz	120.00	120.00	120.00	us
Using CLKFX outputs	LOCK_FX_MIN		10.00	10.00	10.00	ms
	LOCK_FX_MAX		10.00	10.00	10.00	ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT		50.00	50.00	50.00	us
Fine Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.00	10.00	10.00	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.00	30.00	30.00	ps
	DCM_TAP_MAX		50.00	50.00	50.00	ps

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Frequency Synthesis

Table 62: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross-Reference

Table 63: Parameter Cross-Reference

Libraries Guide	Data Sheet
DLL_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_{1X 2X DV}_LF
DFS_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_{1X DV}_HF
DFS_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_FX_HF

Date	Version	Revision
08/25/03	2.9	- Updated time and frequency parameters as per speedsfile v1.81. Table 1: Footnote (2) rewritten to specify “one or more banks.” Table 2: Added footnote referring to XAPP659 for 3.3V I/O operation. Table 53 and Table 54: Revised test setup footnote to refer to Figure 6. Previously specified a capacitive load parameter. Table 57: Due to a document compilation error in v2.8, some DCM parameters were erroneously omitted from the full data sheet file (all four modules concatenated), though not from the stand-alone Module 3 file. The omitted parameters have been restored. Table 64 and Table 66: Corrected parameters to expression in picoseconds, as labeled. Previously expressed in nanoseconds, but labeled picoseconds. Figure 6: Added note to figure regarding termination resistors. Table 5: Added $I_{CCINTMIN}$ for XC2VP30 device.
09/10/03	2.10	Figure 7: Changed representation of mode pins M0, M1, and M2 indicating that they must be held to a constant DC level during and after configuration. Table 49: Added footnote indicating that mode pins M0, M1, and M2 must be held to a constant DC level during and after configuration.
10/14/03	2.11	Table 1: Deleted Footnote (2), which had derated the absolute maximum T_J when one or more banks operated at 3.3V. Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. Added new Footnote (2) linking to website for package thermal data. Table 4 and Table 5: Filled in power-on and quiescent current parameters for all devices through XC2VP70. Added Industrial Grade multiplier specification to Footnote (1) in both tables. - In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to XAPP689 regarding handling of simultaneously switching outputs (SSO). - In section I/O Standard Adjustment Measurement Methodology: Table 39 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 40, Output Delay Measurement Methodology. - Replaced Figure 6, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. Table 58: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
11/10/03	2.12	Table 1: Changed 3.3V absolute max V_{IN} and V_{TS} from 3.75V to 4.05V. Added footnote referring to XAPP659. Table 4: Removed MIN column from table.
12/05/03	3.0	- XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, updated and released to Production status as per speedsfile v1.83. Featured changes: - Speedsfile parameter values for -7 speed grade added for devices XC2VP2-XC2VP70. Table 13 and Table 14: Pin-to-pin and register-to_register performance parameter values added. Table 64: New parameter T_{DCD_LOCAL} (and footnote) replaces T_{DCD_CLK0}. - All remaining source-synchronous parameter values added (Table 64 & following).

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)

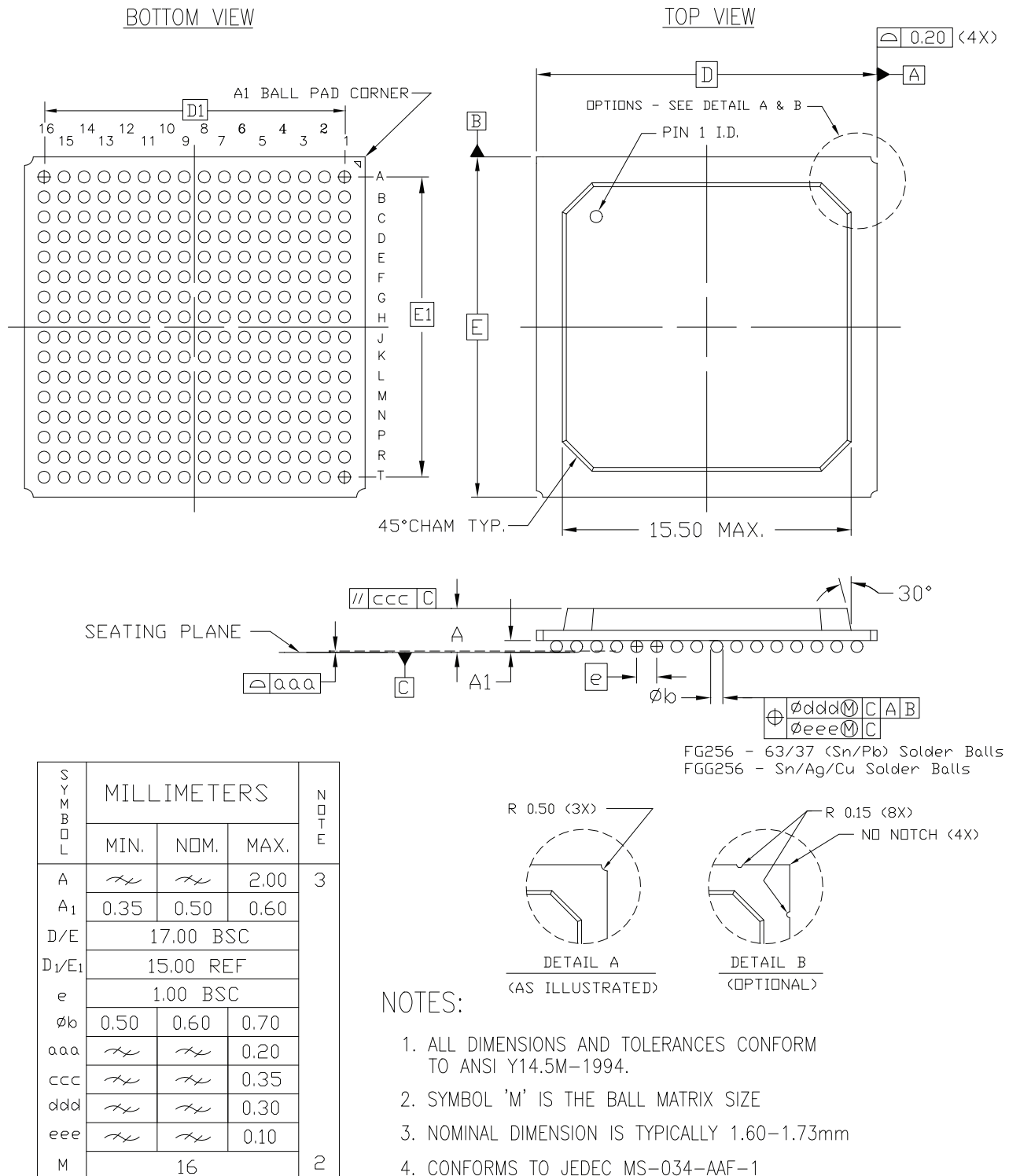


Figure 1: FG256/FGG256 Fine-Pitch BGA Package Specifications

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L52P_7	M7			
7	IO_L52N_7/VREF_7	L7			
7	IO_L50P_7	K1			
7	IO_L50N_7	K2			
7	IO_L49P_7	L3			
7	IO_L49N_7	K3			
7	IO_L48P_7	K4			
7	IO_L48N_7	K5			
7	IO_L46P_7	L8			
7	IO_L46N_7/VREF_7	K8			
7	IO_L44P_7	J1			
7	IO_L44N_7	J2			
7	IO_L43P_7	J3			
7	IO_L43N_7	J4			
7	IO_L42P_7	J5			
7	IO_L42N_7	J6			
7	IO_L40P_7	J7			
7	IO_L40N_7/VREF_7	J8			
7	IO_L38P_7	H1			
7	IO_L38N_7	H2			
7	IO_L37P_7	H6			
7	IO_L37N_7	H7			
7	IO_L36P_7	G1			
7	IO_L36N_7	G2			
7	IO_L34P_7	G3			
7	IO_L34N_7/VREF_7	G4			
7	IO_L32P_7	H5			
7	IO_L32N_7	G5			
7	IO_L31P_7	F1			
7	IO_L31N_7	F2			
7	IO_L24P_7	F3	NC		
7	IO_L24N_7	F4	NC		
7	IO_L06P_7	G6			
7	IO_L06N_7	F6			
7	IO_L04P_7	E1			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	RSVD	C23			
N/A	VBATT	A24			
N/A	TMS	B24			
N/A	TCK	B26			
N/A	TDO	D24			
N/A	CCLK	AE24			
N/A	PWRDWN_B	AF24			
N/A	DONE	AD23			
N/A	AVCCAUXRX16	AE23			
N/A	VTRXPAD16	AE22			
N/A	RXNPAD16	AF23			
N/A	RXPPAD16	AF22			
N/A	GNDA16	AD21			
N/A	TXPPAD16	AF21			
N/A	TXNPAD16	AF20			
N/A	VTTXPAD16	AE20			
N/A	AVCCAUTX16	AE21			
N/A	AVCCAUXRX18	AE18			
N/A	VTRXPAD18	AE17			
N/A	RXNPAD18	AF18			
N/A	RXPPAD18	AF17			
N/A	GNDA18	AD16			
N/A	TXPPAD18	AF16			
N/A	TXNPAD18	AF15			
N/A	VTTXPAD18	AE15			
N/A	AVCCAUTX18	AE16			
N/A	AVCCAUXRX19	AE12			
N/A	VTRXPAD19	AE11			
N/A	RXNPAD19	AF12			
N/A	RXPPAD19	AF11			
N/A	GNDA19	AD11			
N/A	TXPPAD19	AF10			
N/A	TXNPAD19	AF9			
N/A	VTTXPAD19	AE9			
N/A	AVCCAUTX19	AE10			

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	RXPPAD7		A12			
N/A	RXNPAD7		A11			
N/A	VTRXPAD7		B12			
N/A	AVCCAUXRX7		B11			
N/A	AVCCAUXTX9		B6			
N/A	VTTXPAD9		B7			
N/A	TXNPAD9		A7			
N/A	TXPPAD9		A6			
N/A	GND A9		C6			
N/A	RXPPAD9		A5			
N/A	RXNPAD9		A4			
N/A	VTRXPAD9		B5			
N/A	AVCCAUXRX9		B4			
N/A	AVCCAUXRX16		AJ4			
N/A	VTRXPAD16		AJ5			
N/A	RXNPAD16		AK4			
N/A	RXPPAD16		AK5			
N/A	GND A16		AH6			
N/A	TXPPAD16		AK6			
N/A	TXNPAD16		AK7			
N/A	VTTXPAD16		AJ7			
N/A	AVCCAUXTX16		AJ6			
N/A	AVCCAUXRX18		AJ11			
N/A	VTRXPAD18		AJ12			
N/A	RXNPAD18		AK11			
N/A	RXPPAD18		AK12			
N/A	GND A18		AH12			
N/A	TXPPAD18		AK13			
N/A	TXNPAD18		AK14			
N/A	VTTXPAD18		AJ14			
N/A	AVCCAUXTX18		AJ13			
N/A	AVCCAUXRX19		AJ17			
N/A	VTRXPAD19		AJ18			
N/A	RXNPAD19		AK17			
N/A	RXPPAD19		AK18			
N/A	GND A19		AH19			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L01P_6/VRN_6	AJ30				
6	IO_L01N_6/VRP_6	AJ31				
6	IO_L02P_6	AJ27				
6	IO_L02N_6	AJ28				
6	IO_L03P_6	AK31				
6	IO_L03N_6/VREF_6	AK32				
6	IO_L04P_6	AH29				
6	IO_L04N_6	AH30				
6	IO_L05P_6	AH27				
6	IO_L05N_6	AG28				
6	IO_L06P_6	AL33				
6	IO_L06N_6	AL34				
6	IO_L15P_6	AG29	NC			
6	IO_L15N_6/VREF_6	AG30	NC			
6	IO_L16P_6	AK33	NC			
6	IO_L16N_6	AK34	NC			
6	IO_L17P_6	AF27	NC			
6	IO_L17N_6	AF28	NC			
6	IO_L18P_6	AJ33	NC			
6	IO_L18N_6	AJ34	NC			
6	IO_L19P_6	AH31	NC			
6	IO_L19N_6	AH32	NC			
6	IO_L20P_6	AD25	NC			
6	IO_L20N_6	AD26	NC			
6	IO_L21P_6	AG31	NC			
6	IO_L21N_6/VREF_6	AG32	NC			
6	IO_L22P_6	AF29	NC			
6	IO_L22N_6	AF30	NC			
6	IO_L23P_6	AE27	NC			
6	IO_L23N_6	AE28	NC			
6	IO_L24P_6	AH33	NC			
6	IO_L24N_6	AH34	NC			
6	IO_L31P_6	AF31				
6	IO_L31N_6	AF32				
6	IO_L32P_6	AC25				
6	IO_L32N_6	AC26				
6	IO_L33P_6	AG33				
6	IO_L33N_6/VREF_6	AG34				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L27P_5	AL23		
5	IO_L26N_5	AD22		
5	IO_L26P_5	AE22		
5	IO_L25N_5	AJ23		
5	IO_L25P_5	AK23		
5	IO_L21N_5	AN24		
5	IO_L21P_5	AP24		
5	IO_L20N_5	AE23		
5	IO_L20P_5	AF23		
5	IO_L19N_5	AM23		
5	IO_L19P_5	AM24		
5	IO_L09N_5/VREF_5	AJ24		
5	IO_L09P_5	AK24		
5	IO_L08N_5	AG22		
5	IO_L08P_5	AG23		
5	IO_L07N_5/VREF_5	AH23		
5	IO_L07P_5	AH24		
5	IO_L06N_5/VRP_5	AN25		
5	IO_L06P_5/VRN_5	AP25		
5	IO_L05_5/No_Pair	AH25		
5	IO_L03N_5/D4	AL25		
5	IO_L03P_5/D5	AM25		
5	IO_L02N_5/D6	AE24		
5	IO_L02P_5/D7	AF24		
5	IO_L01N_5/RDWR_B	AJ25		
5	IO_L01P_5/CS_B	AK25		
6	IO_L01P_6/VRN_6	AP32		
6	IO_L01N_6/VRP_6	AN32		
6	IO_L02P_6	AP28		
6	IO_L02N_6	AN28		
6	IO_L03P_6	AP31		
6	IO_L03N_6/VREF_6	AN31		
6	IO_L04P_6	AP29		
6	IO_L04N_6	AN29		
6	IO_L05P_6	AN26		
6	IO_L05N_6	AN27		
6	IO_L06P_6	AM33		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L57N_5/VREF_5	AT23		
5	IO_L57P_5	AU23		
5	IO_L56N_5	AJ22		
5	IO_L56P_5	AK22		
5	IO_L55N_5	AN23		
5	IO_L55P_5	AP24		
5	IO_L54N_5	AL23		
5	IO_L54P_5	AM23		
5	IO_L53_5/No_Pair	AH23		
5	IO_L50_5/No_Pair	AG23		
5	IO_L49N_5	AR24		
5	IO_L49P_5	AR25		
5	IO_L48N_5	AL24		
5	IO_L48P_5	AM24		
5	IO_L47N_5	AH22		
5	IO_L47P_5	AJ23		
5	IO_L46N_5	AT25		
5	IO_L46P_5	AU25		
5	IO_L45N_5/VREF_5	AN25		
5	IO_L45P_5	AP25		
5	IO_L44N_5	AH24		
5	IO_L44P_5	AH25		
5	IO_L43N_5	AL25		
5	IO_L43P_5	AM25		
5	IO_L39N_5	AT26		
5	IO_L39P_5	AU26		
5	IO_L38N_5	AK24		
5	IO_L38P_5	AK25		
5	IO_L37N_5	AP26		
5	IO_L37P_5	AR26		
5	IO_L36N_5/VREF_5	AM26	NC	
5	IO_L36P_5	AN26	NC	
5	IO_L35N_5	AJ25	NC	
5	IO_L35P_5	AJ26	NC	
5	IO_L34N_5	AR27	NC	
5	IO_L34P_5	AT27	NC	
5	IO_L30N_5	AN27	NC	
5	IO_L30P_5	AP28	NC	

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	VCCINT	R17		
N/A	VCCINT	AE16		
N/A	VCCINT	AD16		
N/A	VCCINT	T16		
N/A	VCCINT	R16		
N/A	VCCINT	AE15		
N/A	VCCINT	AD15		
N/A	VCCINT	AC15		
N/A	VCCINT	AB15		
N/A	VCCINT	AA15		
N/A	VCCINT	Y15		
N/A	VCCINT	W15		
N/A	VCCINT	V15		
N/A	VCCINT	U15		
N/A	VCCINT	T15		
N/A	VCCINT	R15		
N/A	VCCINT	AF14		
N/A	VCCINT	P14		
N/A	VCCINT	AG13		
N/A	VCCINT	N13		
N/A	VCCINT	AH12		
N/A	VCCINT	M12		
N/A	VCCAUX	AV39		
N/A	VCCAUX	AA39		
N/A	VCCAUX	Y39		
N/A	VCCAUX	W39		
N/A	VCCAUX	B39		
N/A	VCCAUX	AW38		
N/A	VCCAUX	Y38		
N/A	VCCAUX	A38		
N/A	VCCAUX	AR35		
N/A	VCCAUX	E35		
N/A	VCCAUX	AP34		
N/A	VCCAUX	F34		
N/A	VCCAUX	AW20		
N/A	VCCAUX	AV20		
N/A	VCCAUX	B20		
N/A	VCCAUX	A20		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L02P_6	BA34	
6	IO_L02N_6	AY34	
6	IO_L03P_6	BB37	
6	IO_L03N_6/VREF_6	BA37	
6	IO_L04P_6	BB36	
6	IO_L04N_6	BA36	
6	IO_L05P_6	AW34	
6	IO_L05N_6	AW35	
6	IO_L06P_6	BB35	
6	IO_L06N_6	BA35	
6	IO_L73P_6	BA38	
6	IO_L73N_6	AY38	
6	IO_L74P_6	AU34	
6	IO_L74N_6	AT34	
6	IO_L75P_6	AY39	
6	IO_L75N_6/VREF_6	AY40	
6	IO_L76P_6	AY37	
6	IO_L76N_6	AW36	
6	IO_L77P_6	AR34	
6	IO_L77N_6	AR35	
6	IO_L78P_6	AY35	
6	IO_L78N_6	AY36	
6	IO_L79P_6	AW41	
6	IO_L79N_6	AW42	
6	IO_L80P_6	AP35	
6	IO_L80N_6	AN34	
6	IO_L81P_6	AW40	
6	IO_L81N_6/VREF_6	AV40	
6	IO_L82P_6	AW39	
6	IO_L82N_6	AV39	
6	IO_L83P_6	AM34	
6	IO_L83N_6	AM35	
6	IO_L84P_6	AW38	
6	IO_L84N_6	AV37	
6	IO_L61P_6	AV41	
6	IO_L61N_6	AU40	
6	IO_L62P_6	AL34	