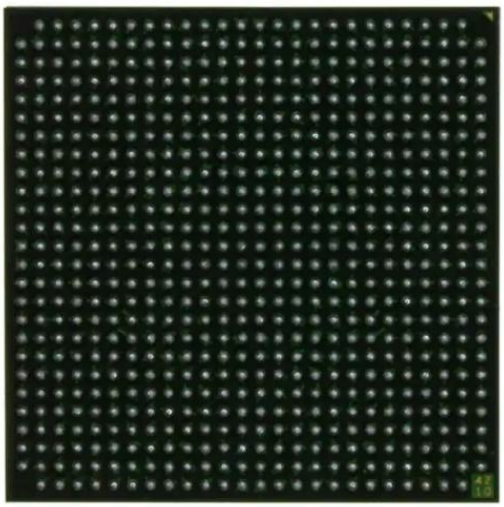

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5ffg672i

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

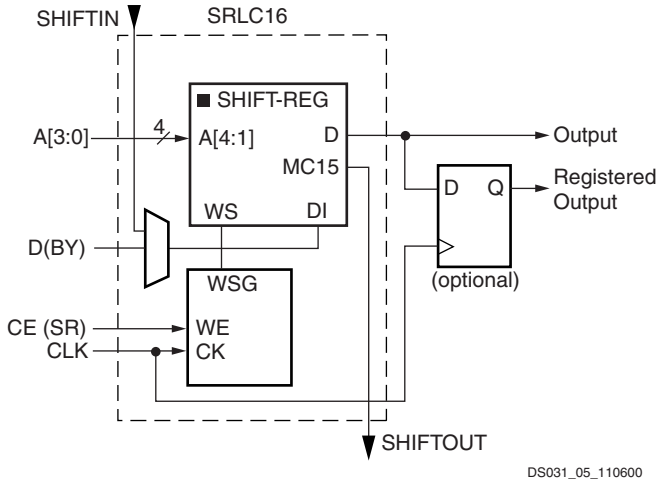


Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

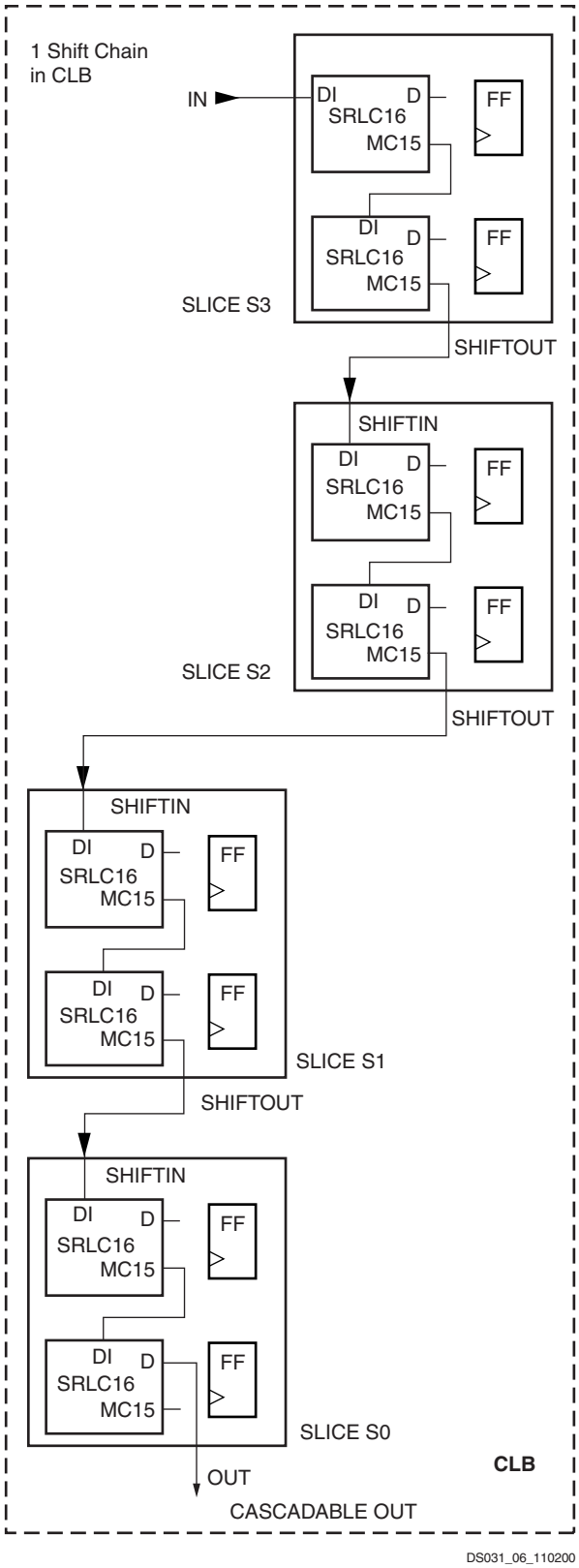


Figure 40: **Cascadable Shift Register**

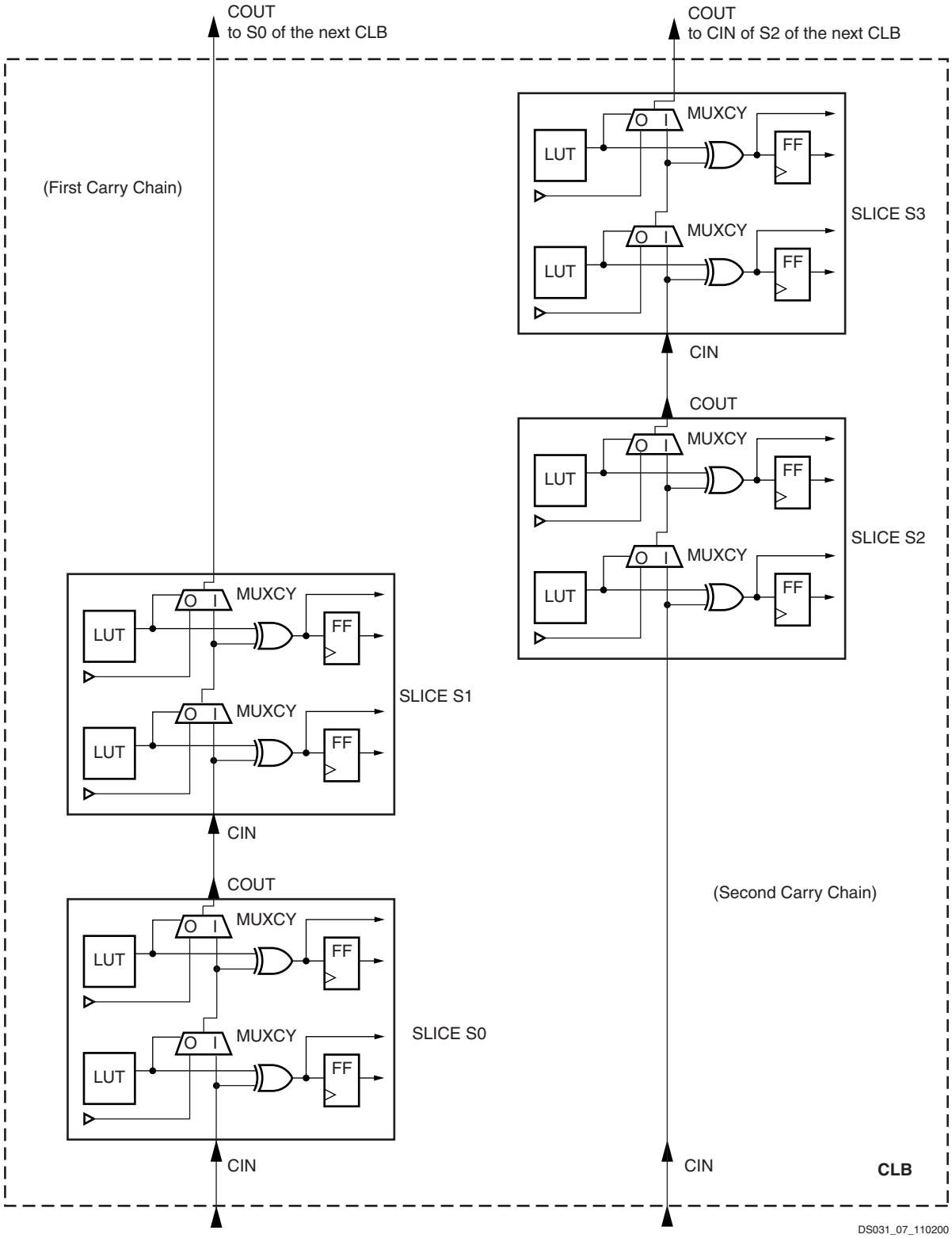


Figure 42: **Fast Carry Logic Path**

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

Table 37: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.58	1.68	1.85	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.65	1.82	1.99	ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}	1.23	1.35	1.51	ns, max
T input to valid data on Pad	T_{IOTP}	1.51	1.63	1.78	ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$	1.08	1.22	1.36	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.56	1.69	1.85	ns, max
GTS to Pad high-impedance(2)	T_{GTS}	4.11	4.73	5.20	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.59	1.76	1.93	ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}	1.39	1.55	1.73	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.67	1.82	2.00	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
Set/Reset Delays					
Minimum Pulse Width, SR inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
SR input to Pad (asynchronous)	T_{IOSRP}	2.33	2.56	2.83	ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}	1.97	2.16	2.41	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.24	2.44	2.69	ns, max
GSR to Pad	T_{IOGSRQ}	5.87	6.75	7.43	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

Multiplier Switching Characteristics

Table 45: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T_{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T_{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T_{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T_{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T_{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T_{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T_{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T_{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T_{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T_{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T_{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T_{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T_{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T_{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T_{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T_{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T_{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T_{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T_{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T_{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T_{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T_{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T_{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T_{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T_{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T_{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T_{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T_{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T_{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T_{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T_{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T_{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T_{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T_{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T_{MULT_P0}	1.13	1.27	1.43	ns, max

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 8, with Master Serial clock timing shown in Figure 9. Programming parameters for both Slave and Master modes are given in Table 50.

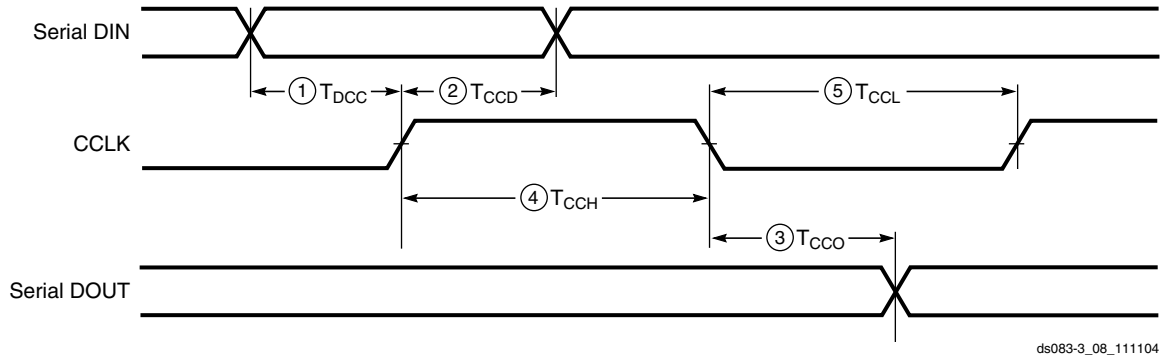


Figure 8: **Slave Serial Mode Timing Sequence**

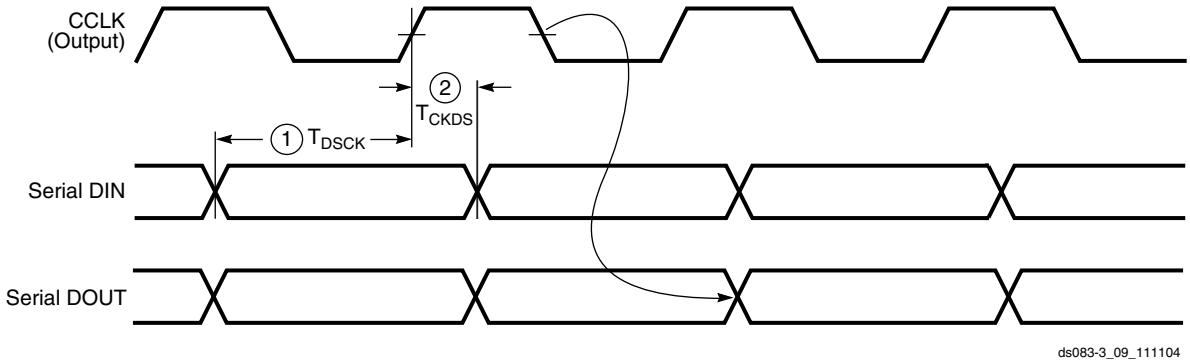


Figure 9: **Master Serial Mode Timing Sequence**

Table 50: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 8)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 9)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

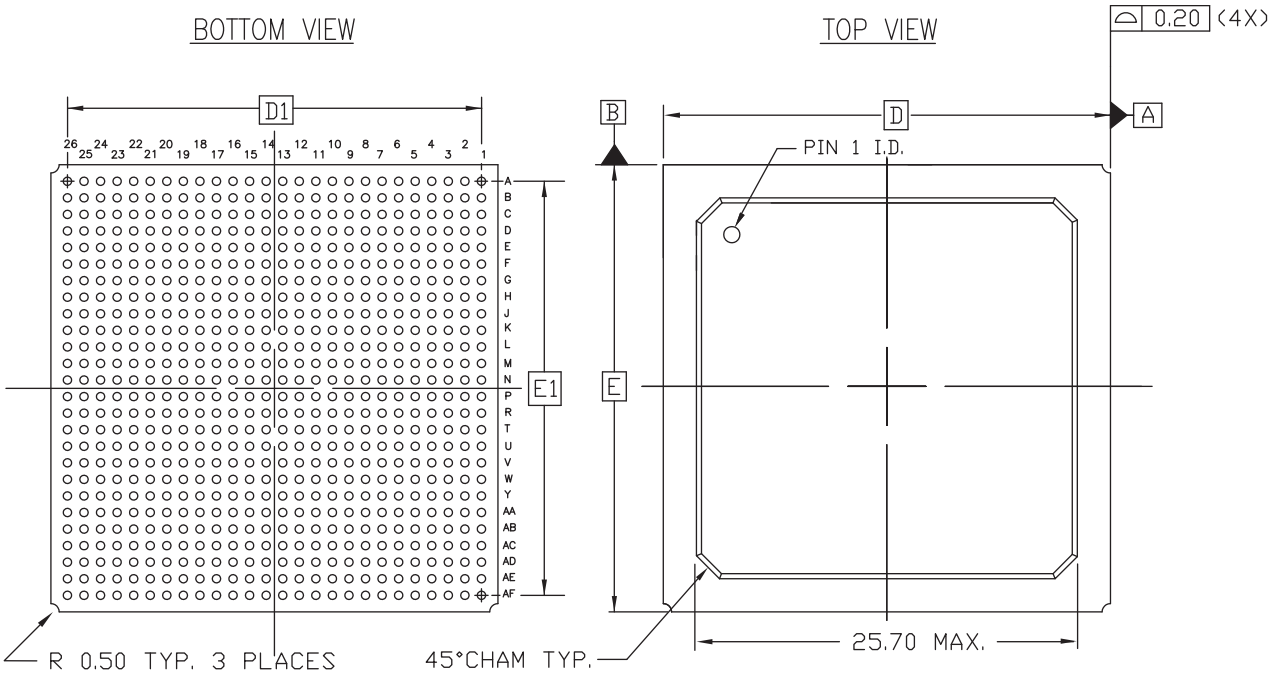
			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

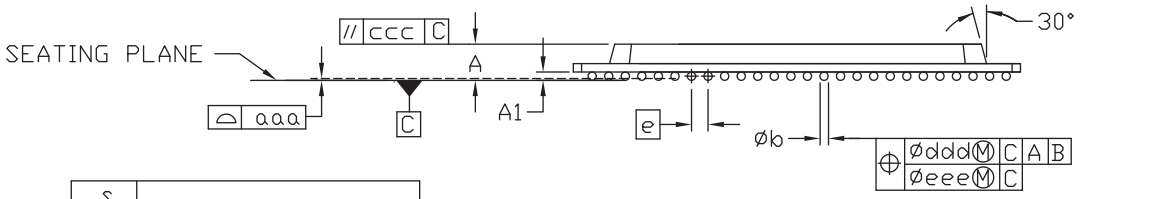
Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)





FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L41N_2		L8	NC		
2	IO_L41P_2		L7	NC		
2	IO_L42N_2		H4	NC		
2	IO_L42P_2		H3	NC		
2	IO_L43N_2		H2			
2	IO_L43P_2		J2			
2	IO_L44N_2		M8			
2	IO_L44P_2		M7			
2	IO_L45N_2		K6			
2	IO_L45P_2		K5			
2	IO_L46N_2/VREF_2		J1			
2	IO_L46P_2		K1			
2	IO_L47N_2		M6			
2	IO_L47P_2		M5			
2	IO_L48N_2		J4			
2	IO_L48P_2		J3			
2	IO_L49N_2		K2			
2	IO_L49P_2		L2			
2	IO_L50N_2		N8			
2	IO_L50P_2		N7			
2	IO_L51N_2		K4			
2	IO_L51P_2		K3			
2	IO_L52N_2/VREF_2		L1			
2	IO_L52P_2		M1			
2	IO_L53N_2		N6			
2	IO_L53P_2		N5			
2	IO_L54N_2		L5			
2	IO_L54P_2		L4			
2	IO_L55N_2		M2			
2	IO_L55P_2		N2			
2	IO_L56N_2		P9			
2	IO_L56P_2		R9			
2	IO_L57N_2		M4			
2	IO_L57P_2		M3			
2	IO_L58N_2/VREF_2		N1			
2	IO_L58P_2		P1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L54N_7		L26			
7	IO_L53P_7		N26			
7	IO_L53N_7		N25			
7	IO_L52P_7		M30			
7	IO_L52N_7/VREF_7		L30			
7	IO_L51P_7		K28			
7	IO_L51N_7		K27			
7	IO_L50P_7		N24			
7	IO_L50N_7		N23			
7	IO_L49P_7		L29			
7	IO_L49N_7		K29			
7	IO_L48P_7		J28			
7	IO_L48N_7		J27			
7	IO_L47P_7		M26			
7	IO_L47N_7		M25			
7	IO_L46P_7		K30			
7	IO_L46N_7/VREF_7		J30			
7	IO_L45P_7		K26			
7	IO_L45N_7		K25			
7	IO_L44P_7		M24			
7	IO_L44N_7		M23			
7	IO_L43P_7		J29			
7	IO_L43N_7		H29			
7	IO_L42P_7		H28	NC		
7	IO_L42N_7		H27	NC		
7	IO_L41P_7		L24	NC		
7	IO_L41N_7		L23	NC		
7	IO_L40P_7		G30	NC		
7	IO_L40N_7/VREF_7		G29	NC		
7	IO_L39P_7		G28	NC		
7	IO_L39N_7		G27	NC		
7	IO_L38P_7		J26	NC		
7	IO_L38N_7		J25	NC		
7	IO_L37P_7		F30	NC		
7	IO_L37N_7		F29	NC		
7	IO_L36P_7		F28	NC		

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E29				
0	IO_L01P_0/VRN_0	E28				
0	IO_L02N_0	H26				
0	IO_L02P_0	G26				
0	IO_L03N_0	H25				
0	IO_L03P_0/VREF_0	G25				
0	IO_L05_0/No_Pair	J25				
0	IO_L06N_0	K24				
0	IO_L06P_0	J24				
0	IO_L07N_0	F26				
0	IO_L07P_0	E26				
0	IO_L08N_0	D30				
0	IO_L08P_0	D29				
0	IO_L09N_0	K23				
0	IO_L09P_0/VREF_0	J23				
0	IO_L19N_0	F24	NC	NC		
0	IO_L19P_0	E24	NC	NC		
0	IO_L20N_0	D28	NC	NC		
0	IO_L20P_0	C28	NC	NC		
0	IO_L21N_0	H24	NC	NC		
0	IO_L21P_0	G24	NC	NC		
0	IO_L25N_0	G23	NC	NC		
0	IO_L25P_0	F23	NC	NC		
0	IO_L26N_0	E27	NC	NC		
0	IO_L26P_0	D27	NC	NC		
0	IO_L27N_0	K22	NC	NC		
0	IO_L27P_0/VREF_0	J22	NC	NC		
0	IO_L37N_0	H22				
0	IO_L37P_0	G22				
0	IO_L38N_0	D26				
0	IO_L38P_0	C26				
0	IO_L39N_0	K21				
0	IO_L39P_0	J21				
0	IO_L43N_0	F22				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AF34				
N/A	GND	B34				
N/A	GND	C1				
N/A	GND	C2				
N/A	GND	C10				
N/A	GND	C16				
N/A	GND	C19				
N/A	GND	C25				
N/A	GND	C33				
N/A	GND	C34				
N/A	GND	D4				
N/A	GND	D31				
N/A	GND	E5				
N/A	GND	E12				
N/A	GND	E23				
N/A	GND	E30				
N/A	GND	F6				
N/A	GND	F29				
N/A	GND	G7				
N/A	GND	G28				
N/A	GND	B1				
N/A	GND	H8				
N/A	GND	H12				
N/A	GND	H15				
N/A	GND	H20				
N/A	GND	J1				
N/A	GND	H27				
N/A	GND	AF1				
N/A	GND	K3				
N/A	GND	K32				
N/A	GND	M5				
N/A	GND	M8				
N/A	GND	M27				
N/A	GND	M30				
N/A	GND	P14				
N/A	GND	P15				
N/A	GND	P16				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L21P_2	E6		
2	IO_L22N_2/VREF_2	F7		
2	IO_L22P_2	F8		
2	IO_L23N_2	M10		
2	IO_L23P_2	L10		
2	IO_L24N_2	G5		
2	IO_L24P_2	F5		
2	IO_L25N_2	F3		
2	IO_L25P_2	F4		
2	IO_L26N_2	M8		
2	IO_L26P_2	M9		
2	IO_L27N_2	F1		
2	IO_L27P_2	F2		
2	IO_L28N_2/VREF_2	G6		
2	IO_L28P_2	G7		
2	IO_L29N_2	M7		
2	IO_L29P_2	N8		
2	IO_L30N_2	G3		
2	IO_L30P_2	H4		
2	IO_L31N_2	G1		
2	IO_L31P_2	G2		
2	IO_L32N_2	N10		
2	IO_L32P_2	N11		
2	IO_L33N_2	H5		
2	IO_L33P_2	H6		
2	IO_L34N_2/VREF_2	H2		
2	IO_L34P_2	H3		
2	IO_L35N_2	N6		
2	IO_L35P_2	N7		
2	IO_L36N_2	K4		
2	IO_L36P_2	J4		
2	IO_L37N_2	J2		
2	IO_L37P_2	J3		
2	IO_L38N_2	P10		
2	IO_L38P_2	P11		
2	IO_L39N_2	K5		
2	IO_L39P_2	K6		
2	IO_L40N_2/VREF_2	L3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L48N_1		J17		
1	IO_L48P_1		H17		
1	IO_L47N_1		K17		
1	IO_L47P_1		L17		
1	IO_L46N_1		M17		
1	IO_L46P_1		M18		
1	IO_L45N_1/VREF_1		F16		
1	IO_L45P_1		E16		
1	IO_L44N_1		G16		
1	IO_L44P_1		H16		
1	IO_L43N_1		K16		
1	IO_L43P_1		J16		
1	IO_L39N_1		M16		
1	IO_L39P_1		L16		
1	IO_L38N_1		C15		
1	IO_L38P_1		C14		
1	IO_L37N_1		F15		
1	IO_L37P_1		E15		
1	IO_L87N_1/VREF_1		J15	NC	
1	IO_L87P_1		H15	NC	
1	IO_L86N_1		K15	NC	
1	IO_L86P_1		L15	NC	
1	IO_L85N_1		E14	NC	
1	IO_L85P_1		D14	NC	
1	IO_L84N_1		G14	NC	
1	IO_L84P_1		F14	NC	
1	IO_L83_1/No_Pair		H14	NC	
1	IO_L78N_1		L14	NC	
1	IO_L78P_1		K14	NC	
1	IO_L36N_1/VREF_1		M14		
1	IO_L36P_1		M15		
1	IO_L35N_1		C13		
1	IO_L35P_1		D13		
1	IO_L34N_1		F13		
1	IO_L34P_1		E13		
1	IO_L30N_1		H13		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L77N_3		AT3		
3	IO_L77P_3		AT4		
3	IO_L76N_3		AU1		
3	IO_L76P_3		AU2		
3	IO_L75N_3/VREF_3		AU3		
3	IO_L75P_3		AU4		
3	IO_L74N_3		AV3		
3	IO_L74P_3		AW3		
3	IO_L73N_3		AV1		
3	IO_L73P_3		AV2		
3	IO_L06N_3		AW1		
3	IO_L06P_3		AW2		
3	IO_L05N_3		AT8		
3	IO_L05P_3		AU8		
3	IO_L04N_3		AT6		
3	IO_L04P_3		AU7		
3	IO_L03N_3/VREF_3		AY5		
3	IO_L03P_3		AY6		
3	IO_L02N_3		AV7		
3	IO_L02P_3		AW7		
3	IO_L01N_3/VRP_3		AV6		
3	IO_L01P_3/VRN_3		AW6		
4	IO_L01N_4/BUSY/DOUT(1)		AT9		
4	IO_L01P_4/INIT_B		AR9		
4	IO_L02N_4/D0/DIN(1)		AU9		
4	IO_L02P_4/D1		AV9		
4	IO_L03N_4/D2		AY9		
4	IO_L03P_4/D3		AW9		
4	IO_L05_4/No_Pair		AN11		
4	IO_L06N_4/VRP_4		AR10		
4	IO_L06P_4/VRN_4		AP10		
4	IO_L07N_4		AU10		
4	IO_L07P_4/VREF_4		AT10		
4	IO_L08N_4		AV10		
4	IO_L08P_4		AW10		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L60P_4		AR19		
4	IO_L64N_4		AV19		
4	IO_L64P_4		AU19		
4	IO_L65N_4		AW19		
4	IO_L65P_4		AY19		
4	IO_L66N_4		AL21		
4	IO_L66P_4/VREF_4		AL20		
4	IO_L67N_4		AN20		
4	IO_L67P_4		AM20		
4	IO_L68N_4		AP20		
4	IO_L68P_4		AR20		
4	IO_L69N_4		AV20		
4	IO_L69P_4/VREF_4		AU20		
4	IO_L73N_4		AY20		
4	IO_L73P_4		AW20		
4	IO_L74N_4/GCLK3S		AN21		
4	IO_L74P_4/GCLK2P		AP21		
4	IO_L75N_4/GCLK1S		AU21		
4	IO_L75P_4/GCLK0P		AT21		
5	IO_L75N_5/GCLK7S	BREFCLKN	AT22		
5	IO_L75P_5/GCLK6P	BREFCLKP	AU22		
5	IO_L74N_5/GCLK5S		AP22		
5	IO_L74P_5/GCLK4P		AN22		
5	IO_L73N_5		AW23		
5	IO_L73P_5		AY23		
5	IO_L69N_5/VREF_5		AU23		
5	IO_L69P_5		AV23		
5	IO_L68N_5		AR23		
5	IO_L68P_5		AP23		
5	IO_L67N_5		AM23		
5	IO_L67P_5		AN23		
5	IO_L66N_5/VREF_5		AL23		
5	IO_L66P_5		AL22		
5	IO_L65N_5		AY24		
5	IO_L65P_5		AW24		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L34P_0	C30	
0	IO_L35N_0	L29	
0	IO_L35P_0	M29	
0	IO_L36N_0	H28	
0	IO_L36P_0/VREF_0	G29	
0	IO_L76N_0	E29	
0	IO_L76P_0	F29	
0	IO_L77N_0	J29	
0	IO_L77P_0	K29	
0	IO_L78N_0	D28	
0	IO_L78P_0	C29	
0	IO_L79N_0	A29	
0	IO_L79P_0	B29	
0	IO_L80_0/No_Pair	L28	
0	IO_L83_0/No_Pair	M28	
0	IO_L84N_0	G27	
0	IO_L84P_0	G28	
0	IO_L85N_0	E28	
0	IO_L85P_0	F28	
0	IO_L86N_0	J28	
0	IO_L86P_0	K28	
0	IO_L87N_0	C27	
0	IO_L87P_0/VREF_0	C28	
0	IO_L37N_0	A28	
0	IO_L37P_0	B28	
0	IO_L38N_0	L27	
0	IO_L38P_0	M27	
0	IO_L39N_0	H26	
0	IO_L39P_0	H27	
0	IO_L43N_0	E27	
0	IO_L43P_0	F27	
0	IO_L44N_0	J27	
0	IO_L44P_0	K27	
0	IO_L45N_0	D26	
0	IO_L45P_0/VREF_0	D27	
0	IO_L10N_0	A27	NC
0	IO_L10P_0	B27	NC

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	VCCO_7	AA29	
7	VCCO_7	Y29	
7	VCCO_7	W29	
7	VCCO_7	V29	
7	VCCO_7	U29	
7	VCCO_7	T29	
7	VCCO_7	R29	
7	VCCO_7	AA28	
7	VCCO_7	Y28	
7	VCCO_7	W28	
7	VCCO_7	V28	
7	VCCO_7	U28	
7	VCCO_7	T28	
6	VCCO_6	AU39	
6	VCCO_6	AN39	
6	VCCO_6	AJ39	
6	VCCO_6	AD39	
6	VCCO_6	AW37	
6	VCCO_6	AN35	
6	VCCO_6	AJ35	
6	VCCO_6	AD35	
6	VCCO_6	AR33	
6	VCCO_6	AL33	
6	VCCO_6	AH29	
6	VCCO_6	AG29	
6	VCCO_6	AF29	
6	VCCO_6	AE29	
6	VCCO_6	AD29	
6	VCCO_6	AC29	
6	VCCO_6	AB29	
6	VCCO_6	AG28	
6	VCCO_6	AF28	
6	VCCO_6	AE28	
6	VCCO_6	AD28	
6	VCCO_6	AC28	
6	VCCO_6	AB28	
5	VCCO_5	AW33	