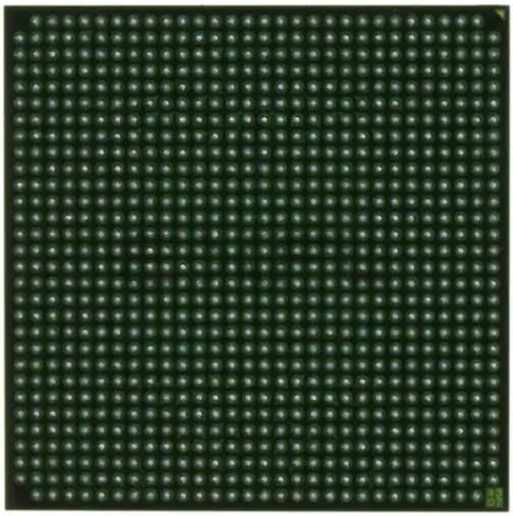

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5ffg896c

  - HyperTransport (LDT) I/O with current driver buffers
  - Built-in DDR input and output registers
- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13 µm Nine-Layer Copper Process with 90 nm High-Speed Transistors
- 1.5V (V_{CCINT}) core power supply, dedicated 2.5V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
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General Description

The Virtex-II Pro and Virtex-II Pro X families contain platform FPGAs for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU blocks in Virtex-II Pro Series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13 µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gate arrays.

Architecture

Array Overview

Virtex-II Pro and Virtex-II Pro X devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high-density and high-performance system designs. Virtex-II Pro devices implement the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel (RocketIO) or 6.25 Gb/s (RocketIO X).
- Embedded IBM PowerPC 405 RISC processor blocks provide performance up to 400 MHz.
- SelectIO-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM+ memory modules provide large 18 Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and supports high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Features

This section briefly describes Virtex-II Pro / Virtex-II Pro X features. For more details, refer to Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description.

RocketIO / RocketIO X MGT Cores

The RocketIO and RocketIO X Multi-Gigabit Transceivers are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 100 Gb/s (RocketIO) or 170 Gb/s (RocketIO X) of full-duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s (RocketIO) or 6.25 Gb/s (RocketIO X).

Functional Description: FPGA

Input/Output Blocks (IOBs)

Virtex-II Pro I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 18.

IOB blocks are designed for high-performance I/O, supporting 22 single-ended standards, as well as differential signaling with LVDS, LDT, bus LVDS, and LVPECL.

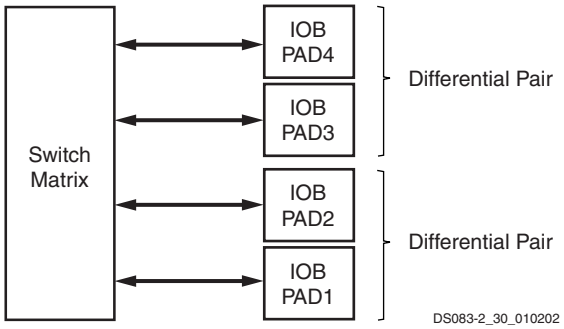

Figure 18: **Virtex-II Pro Input/Output Tile**

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II Pro IOB blocks feature SelectIO-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 8 and Table 9). An auxiliary supply voltage (V_{CCAUX} = 2.5V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. The IOBs are not compatible or compliant with 5V I/O standards (not 5V-tolerant).

Table 10 lists supported I/O standards with Digitally Controlled Impedance. See Digitally Controlled Impedance (DCI), page 31.

Table 8: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL(1)	3.3	3.3	N/R	N/R
LVCMOS33(1)	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	Note (2)	Note (2)	N/R	N/R
PCI66_3	Note (2)	Note (2)	N/R	N/R
PCIX	Note (2)	Note (2)	N/R	N/R
GTL	Note (3)	Note (3)	0.8	1.2
GTLP	Note (3)	Note (3)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL18_I (4)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9

Notes:
1. Refer to **XAPP659** for more details on interfacing to these 3.3V standards.
2. For PCI and PCI-X standards, refer to **XAPP653**.
3. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. *Example:* If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
4. SSTL18_I is not a JEDEC-supported standard.
5. N/R = no requirement.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments.

Table 35: **IOB Input Switching Characteristics**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.84	0.87	0.91	ns, max
Pad to I output, with delay	T_{IOPID}	XC2VP2	1.84	1.94	2.06	ns, max
		XC2VP4	1.84	1.94	2.06	ns, max
		XC2VP7	1.84	1.94	2.06	ns, max
		XC2VP20	2.14	2.23	2.37	ns, max
		XC2VPX20	2.14	2.23	2.37	ns, max
		XC2VP30	2.14	2.26	2.46	ns, max
		XC2VP40	2.54	2.67	2.81	ns, max
		XC2VP50	2.54	2.68	2.87	ns, max
		XC2VP70	2.54	2.72	2.91	ns, max
		XC2VPX70	2.54	2.72	2.91	ns, max
		XC2VP100	N/A	4.71	4.80	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.86	0.89	0.93	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2VP2	2.30	2.62	2.97	ns, max
		XC2VP4	2.57	2.89	3.23	ns, max
		XC2VP7	2.50	2.84	3.17	ns, max
		XC2VP20	2.65	3.04	3.42	ns, max
		XC2VPX20	2.65	3.04	3.42	ns, max
		XC2VP30	2.69	3.12	3.51	ns, max
		XC2VP40	3.30	3.63	4.03	ns, max
		XC2VP50	3.86	4.10	4.45	ns, max
		XC2VP70	4.00	4.25	4.57	ns, max
		XC2VPX70	4.00	4.25	4.57	ns, max
		XC2VP100	N/A	6.50	7.06	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.60	0.60	0.67	ns, max

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 55: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}.
3. IFF = Input Flip-Flop or Latch

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. These pins can be used to clock the RocketIO transceiver. See the **RocketIO Transceiver User Guide** for design guidelines and BREFCLK-specific pins, by device.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins:(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection. Pin is biased by V_{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used. The mode pins are not to be toggled (changed) while in operation during and after configuration.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock. This pin is 3.3V compatible.
TDI	Input	Boundary Scan Data Input. This pin is 3.3V compatible.
TDO	Output (open-drain)	Boundary Scan Data Output. Pin is open-drain and can be pulled up to 3.3V. It is recommended that the external pull-up be greater than 200Ω. There is no internal pull-up.
TMS	Input	Boundary Scan Mode Select. This pin is 3.3V compatible.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins:		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Connect to V_{CCAUX} or GND if battery not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the RocketIO MGT (2.5V).
AVCCAUXTX#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (2.5V).
BREFCLKN, BREFCLKP(2)	Input	Differential clock input that clocks the RocketIO X MGTs populating the same side of the chip (top or bottom). Can also drive DCMs for RocketIO X MGT use.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	GND	R15
N/A	GND	L6
N/A	GND	L11
N/A	GND	K9
N/A	GND	K8
N/A	GND	K7
N/A	GND	K10
N/A	GND	J9
N/A	GND	J8
N/A	GND	J7
N/A	GND	J10
N/A	GND	H9
N/A	GND	H8
N/A	GND	H7
N/A	GND	H10
N/A	GND	G9
N/A	GND	G8
N/A	GND	G7
N/A	GND	G10
N/A	GND	F6
N/A	GND	F11
N/A	GND	B2
N/A	GND	B15
N/A	GND	A16
N/A	GND	A1

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 6, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FG456/FGG456 fine-pitch BGA package. The pins in these devices are same, except for the differences shown in the "No Connects" column. Following this table are the FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	D5			
0	IO_L01P_0/VRN_0	D6			
0	IO_L02N_0	E6			
0	IO_L02P_0	E7			
0	IO_L03N_0	D7			
0	IO_L03P_0/VREF_0	C7			
0	IO_L05_0/No_Pair	E8			
0	IO_L06N_0	D8			
0	IO_L06P_0	C8			
0	IO_L07N_0	F9			
0	IO_L07P_0	E9			
0	IO_L09N_0	D9			
0	IO_L09P_0/VREF_0	D10			
0	IO_L67N_0	F10			
0	IO_L67P_0	E10			
0	IO_L69N_0	C10			
0	IO_L69P_0/VREF_0	B11			
0	IO_L74N_0/GCLK7P	F11			
0	IO_L74P_0/GCLK6S	E11			
0	IO_L75N_0/GCLK5P	D11			
0	IO_L75P_0/GCLK4S	C11			
1	IO_L75N_1/GCLK3P	C12			
1	IO_L75P_1/GCLK2S	D12			
1	IO_L74N_1/GCLK1P	E12			
1	IO_L74P_1/GCLK0S	F12			
1	IO_L69N_1/VREF_1	B12			
1	IO_L69P_1	C13			
1	IO_L67N_1	E13			
1	IO_L67P_1	F13			
1	IO_L09N_1/VREF_1	D13			
1	IO_L09P_1	D14			
1	IO_L07N_1	E14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	VCCO_2	K2			
2	VCCO_2	K8			
2	VCCO_2	L9			
2	VCCO_2	M9			
2	VCCO_2	N9			
3	VCCO_3	P9			
3	VCCO_3	R9			
3	VCCO_3	T9			
3	VCCO_3	U2			
3	VCCO_3	U8			
3	VCCO_3	V8			
3	VCCO_3	Y2			
4	VCCO_4	W9			
4	VCCO_4	AD7			
4	VCCO_4	V11			
4	VCCO_4	V12			
4	VCCO_4	V13			
4	VCCO_4	W10			
4	VCCO_4	AD10			
5	VCCO_5	V14			
5	VCCO_5	V15			
5	VCCO_5	V16			
5	VCCO_5	W17			
5	VCCO_5	W18			
5	VCCO_5	AD17			
5	VCCO_5	AD20			
6	VCCO_6	P18			
6	VCCO_6	R18			
6	VCCO_6	T18			
6	VCCO_6	U19			
6	VCCO_6	U25			
6	VCCO_6	V19			
6	VCCO_6	Y25			
7	VCCO_7	G25			
7	VCCO_7	J19			
7	VCCO_7	K19			
7	VCCO_7	K25			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L01N_0/VRP_0		E25			
0	IO_L01P_0/VRN_0		E24			
0	IO_L02N_0		F24			
0	IO_L02P_0		F23			
0	IO_L03N_0		E23			
0	IO_L03P_0/VREF_0		E22			
0	IO_L05_0/No_Pair		G23			
0	IO_L06N_0		H22			
0	IO_L06P_0		G22			
0	IO_L07N_0		F22			
0	IO_L07P_0		F21			
0	IO_L08N_0		D24			
0	IO_L08P_0		C24			
0	IO_L09N_0		H21			
0	IO_L09P_0/VREF_0		G21			
0	IO_L37N_0		E21			
0	IO_L37P_0		D21			
0	IO_L38N_0		D23			
0	IO_L38P_0		C23			
0	IO_L39N_0		H20			
0	IO_L39P_0		G20			
0	IO_L43N_0		E20			
0	IO_L43P_0		D20			
0	IO_L44N_0		B23			
0	IO_L44P_0		A23			
0	IO_L45N_0		H19			
0	IO_L45P_0/VREF_0		G19			
0	IO_L46N_0		E19	NC		
0	IO_L46P_0		E18	NC		
0	IO_L47N_0		C22	NC		
0	IO_L47P_0		B22	NC		
0	IO_L48N_0		F20	NC		
0	IO_L48P_0		F19	NC		
0	IO_L49N_0		G17	NC		
0	IO_L49P_0		F17	NC		
0	IO_L50_0/No_Pair		B21	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L02P_6		AH26			
6	IO_L02N_6		AG26			
6	IO_L03P_6		AH29			
6	IO_L03N_6/VREF_6		AH30			
6	IO_L04P_6		AH27			
6	IO_L04N_6		AG28			
6	IO_L05P_6		AD25			
6	IO_L05N_6		AD26			
6	IO_L06P_6		AG29			
6	IO_L06N_6		AG30			
6	IO_L31P_6		AF25	NC		
6	IO_L31N_6		AE26	NC		
6	IO_L32P_6		AB23	NC		
6	IO_L32N_6		AB24	NC		
6	IO_L33P_6		AE27	NC		
6	IO_L33N_6/VREF_6		AE28	NC		
6	IO_L34P_6		AF27	NC		
6	IO_L34N_6		AF28	NC		
6	IO_L35P_6		AC25	NC		
6	IO_L35N_6		AC26	NC		
6	IO_L36P_6		AF29	NC		
6	IO_L36N_6		AF30	NC		
6	IO_L37P_6		AD27	NC		
6	IO_L37N_6		AD28	NC		
6	IO_L38P_6		AA23	NC		
6	IO_L38N_6		AA24	NC		
6	IO_L39P_6		AE29	NC		
6	IO_L39N_6/VREF_6		AE30	NC		
6	IO_L40P_6		AB25	NC		
6	IO_L40N_6		AB26	NC		
6	IO_L41P_6		Y23	NC		
6	IO_L41N_6		Y24	NC		
6	IO_L42P_6		AD29	NC		
6	IO_L42N_6		AD30	NC		
6	IO_L43P_6		AC27			
6	IO_L43N_6		AC28			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L74N_1/GCLK1P	D17				
1	IO_L74P_1/GCLK0S	E17				
1	IO_L73N_1	F17				
1	IO_L73P_1	G17				
1	IO_L69N_1/VREF_1	K17				
1	IO_L69P_1	L17				
1	IO_L68N_1	D16				
1	IO_L68P_1	E16				
1	IO_L67N_1	F16				
1	IO_L67P_1	G16				
1	IO_L57N_1/VREF_1	H16				
1	IO_L57P_1	J16				
1	IO_L56N_1	D15				
1	IO_L56P_1	D14				
1	IO_L55N_1	F15				
1	IO_L55P_1	G15				
1	IO_L54N_1	K16				
1	IO_L54P_1	L16				
1	IO_L53_1/No_Pair	C13				
1	IO_L50_1/No_Pair	C14				
1	IO_L49N_1	E14				
1	IO_L49P_1	F14				
1	IO_L48N_1	J15				
1	IO_L48P_1	K15				
1	IO_L47N_1	C11				
1	IO_L47P_1	D11				
1	IO_L46N_1	D12				
1	IO_L46P_1	D13				
1	IO_L45N_1/VREF_1	G14				
1	IO_L45P_1	H14				
1	IO_L44N_1	D10				
1	IO_L44P_1	E10				
1	IO_L43N_1	E13				
1	IO_L43P_1	F13				
1	IO_L39N_1	J14				
1	IO_L39P_1	K14				
1	IO_L38N_1	C9				
1	IO_L38P_1	D9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L43N_7	M31				
7	IO_L42P_7	L32				
7	IO_L42N_7	L31				
7	IO_L41P_7	N28				
7	IO_L41N_7	N27				
7	IO_L40P_7	M33				
7	IO_L40N_7/VREF_7	L33				
7	IO_L39P_7	M29				
7	IO_L39N_7	M28				
7	IO_L38P_7	N26				
7	IO_L38N_7	N25				
7	IO_L37P_7	L34				
7	IO_L37N_7	K34				
7	IO_L36P_7	L30				
7	IO_L36N_7	L29				
7	IO_L35P_7	L28				
7	IO_L35N_7	L27				
7	IO_L34P_7	K33				
7	IO_L34N_7/VREF_7	J33				
7	IO_L33P_7	K31				
7	IO_L33N_7	K30				
7	IO_L32P_7	M26				
7	IO_L32N_7	M25				
7	IO_L31P_7	H34				
7	IO_L31N_7	H33				
7	IO_L24P_7	H32	NC			
7	IO_L24N_7	H31	NC			
7	IO_L23P_7	K28	NC			
7	IO_L23N_7	K27	NC			
7	IO_L22P_7	J32	NC			
7	IO_L22N_7/VREF_7	J31	NC			
7	IO_L21P_7	J30	NC			
7	IO_L21N_7	J29	NC			
7	IO_L20P_7	G34	NC			
7	IO_L20N_7	G33	NC			
7	IO_L19P_7	H30	NC			
7	IO_L19N_7	H29	NC			
7	IO_L18P_7	L26	NC			

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L44N_6	AA28		
6	IO_L45P_6	AC31		
6	IO_L45N_6/VREF_6	AC32		
6	IO_L46P_6	AC29		
6	IO_L46N_6	AC30		
6	IO_L47P_6	AA24		
6	IO_L47N_6	AA25		
6	IO_L48P_6	AB32		
6	IO_L48N_6	AB33		
6	IO_L49P_6	AB28		
6	IO_L49N_6	AB29		
6	IO_L50P_6	AA26		
6	IO_L50N_6	Y26		
6	IO_L51P_6	AA33		
6	IO_L51N_6/VREF_6	AA34		
6	IO_L52P_6	AB31		
6	IO_L52N_6	AA31		
6	IO_L53P_6	Y24		
6	IO_L53N_6	Y25		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AA30		
6	IO_L55P_6	Y33		
6	IO_L55N_6	Y34		
6	IO_L56P_6	Y28		
6	IO_L56N_6	W27		
6	IO_L57P_6	AA32		
6	IO_L57N_6/VREF_6	Y32		
6	IO_L58P_6	Y29		
6	IO_L58N_6	Y30		
6	IO_L59P_6	W24		
6	IO_L59N_6	W25		
6	IO_L60P_6	W31		
6	IO_L60N_6	W32		
6	IO_L85P_6	W28		
6	IO_L85N_6	W29		
6	IO_L86P_6	V26		
6	IO_L86N_6	V27		
6	IO_L87P_6	W33		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L49N_2	U5		
2	IO_L49P_2	U6		
2	IO_L50N_2	U13		
2	IO_L50P_2	V13		
2	IO_L51N_2	U4		
2	IO_L51P_2	T4		
2	IO_L52N_2/VREF_2	U1		
2	IO_L52P_2	U2		
2	IO_L53N_2	V9		
2	IO_L53P_2	V10		
2	IO_L54N_2	V7		
2	IO_L54P_2	V8		
2	IO_L55N_2	V5		
2	IO_L55P_2	V6		
2	IO_L56N_2	V11		
2	IO_L56P_2	V12		
2	IO_L57N_2	V3		
2	IO_L57P_2	V4		
2	IO_L58N_2/VREF_2	V1		
2	IO_L58P_2	V2		
2	IO_L59N_2	W10		
2	IO_L59P_2	W11		
2	IO_L60N_2	W7		
2	IO_L60P_2	W8		
2	IO_L85N_2	W5		
2	IO_L85P_2	W6		
2	IO_L86N_2	W12		
2	IO_L86P_2	W13		
2	IO_L87N_2	W3		
2	IO_L87P_2	W4		
2	IO_L88N_2/VREF_2	Y7		
2	IO_L88P_2	Y8		
2	IO_L89N_2	W9		
2	IO_L89P_2	Y9		
2	IO_L90N_2	Y3		
2	IO_L90P_2	Y4		
3	IO_L90N_3	AA7		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L53P_6	AB30		
6	IO_L53N_6	AB31		
6	IO_L54P_6	AC38		
6	IO_L54N_6	AC39		
6	IO_L55P_6	AC34		
6	IO_L55N_6	AC35		
6	IO_L56P_6	AA28		
6	IO_L56N_6	AA29		
6	IO_L57P_6	AB38		
6	IO_L57N_6/VREF_6	AB39		
6	IO_L58P_6	AB36		
6	IO_L58N_6	AB37		
6	IO_L59P_6	AA30		
6	IO_L59N_6	AA31		
6	IO_L60P_6	AB34		
6	IO_L60N_6	AB35		
6	IO_L85P_6	AB32		
6	IO_L85N_6	AB33		
6	IO_L86P_6	AA27		
6	IO_L86N_6	Y27		
6	IO_L87P_6	AA36		
6	IO_L87N_6/VREF_6	AA37		
6	IO_L88P_6	AA34		
6	IO_L88N_6	AA35		
6	IO_L89P_6	Y28		
6	IO_L89N_6	Y29		
6	IO_L90P_6	AA32		
6	IO_L90N_6	AA33		
7	IO_L90P_7	Y36		
7	IO_L90N_7	Y37		
7	IO_L89P_7	Y31		
7	IO_L89N_7	W31		
7	IO_L88P_7	Y32		
7	IO_L88N_7/VREF_7	Y33		
7	IO_L87P_7	W36		
7	IO_L87N_7	W37		
7	IO_L86P_7	W27		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	AU3		
N/A	GND	AT3		
N/A	GND	D3		
N/A	GND	C3		
N/A	GND	B3		
N/A	GND	AN12		
N/A	GND	G12		
N/A	GND	C12		
N/A	GND	Y10		
N/A	GND	AH9		
N/A	GND	AD9		
N/A	GND	T9		
N/A	GND	M9		
N/A	GND	AU8		
N/A	GND	AN8		
N/A	GND	G8		
N/A	GND	C8		
N/A	GND	Y6		
N/A	GND	AM5		
N/A	GND	AH5		
N/A	GND	T17		
N/A	GND	AT16		
N/A	GND	AN16		
N/A	GND	AJ16		
N/A	GND	AC16		
N/A	GND	AB16		
N/A	GND	AA16		
N/A	GND	Y16		
N/A	GND	W16		
N/A	GND	V16		
N/A	GND	U16		
N/A	GND	L16		
N/A	GND	G16		
N/A	GND	D16		
N/A	GND	AU12		
N/A	GND	AB18		
N/A	GND	AA18		
N/A	GND	Y18		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	