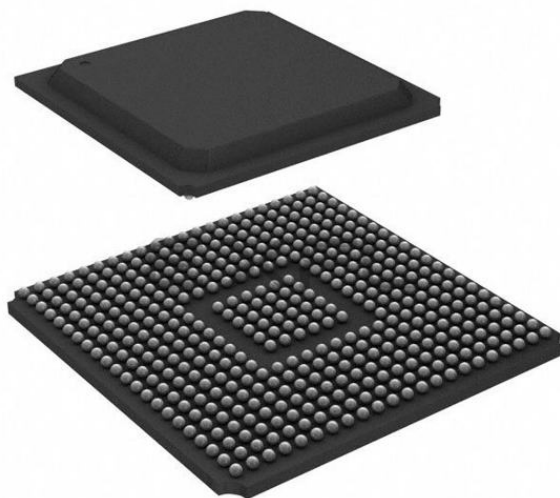




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5fg456c



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011

Product Specification

Virtex-II Pro⁽¹⁾ Array Functional Description

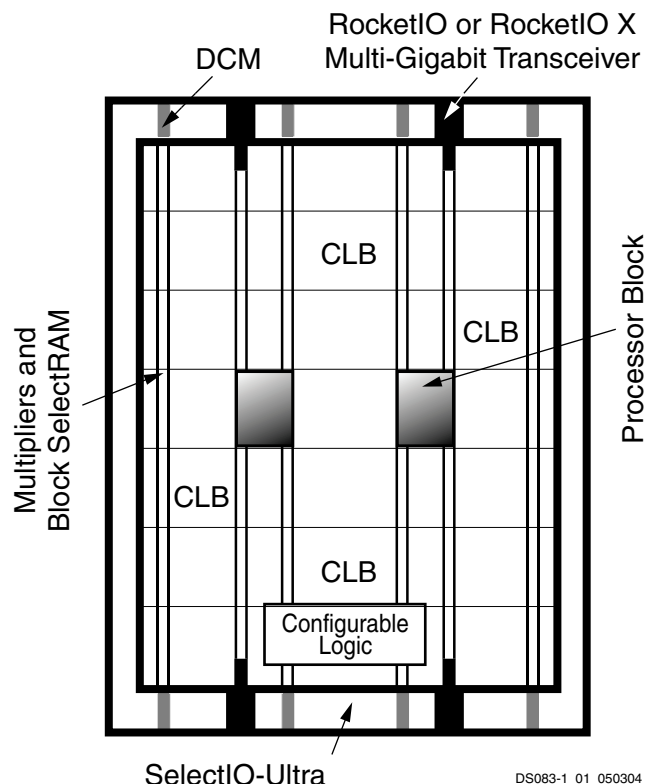


Figure 1: Virtex-II Pro Generic Architecture Overview

This module describes the following Virtex™-II Pro functional components, as shown in **Figure 1**:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in **Module 3** of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see [PowerPC Processor Reference Guide](#) and [PowerPC 405 Processor Block Reference Guide](#).
- For detailed RocketIO transceiver digital/analog design considerations, see [RocketIO Transceiver User Guide](#).
- For detailed RocketIO X transceiver digital/analog design considerations, see [RocketIO X Transceiver User Guide](#).
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see [Virtex-II Pro Platform FPGA User Guide](#).

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

- [Functional Description: RocketIO X Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: RocketIO Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: Processor Block](#)
- [Functional Description: Embedded PowerPC 405 Core](#)
- [Functional Description: FPGA](#)
- [Revision History](#)

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX} , the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 μ m has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Date	Version	Revision
03/24/03	2.5.1	Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	- Removed Compatible Output Standards and Compatible Input Standards tables. - Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. - Corrected sentence in section Input/Output Individual Options, page 27, to read "The optional weak-keeper circuit is connected to each <i>user I/O pad</i>." - Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	- Added four Differential Termination I/O standards to Table 9 and Table 12. - Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	- Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. - Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to Production status.
02/19/04	3.1	Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	Figure 11, page 12: Corrected figure by removing coupling capacitors from input. - Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	- Reassigned heading hierarchies for better agreement with content. Table 7: Corrected VCCAUTX and VCCAUXRX to AVCCAUTX and AVCCAUXRX respectively. Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	<i>No changes in Module 2 for this revision.</i>
09/15/05	4.4	Table 1: Deleted SONET OC-192 protocol. Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. - Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Table 17: Processor Block Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	T _{PCCK_DCR} /T _{PCKC_DCR}	0.38/–0.18	0.44/–0.20	0.48/–0.23	ns, min
Device Control Register Bus data inputs	T _{PDCK_DCR} /T _{PCKD_DCR}	0.65/–0.01	0.75/–0.01	0.82/–0.02	ns, min
Clock and Power Management control inputs	T _{PCCK_CPM} /T _{PCKC_CPM}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	T _{PCCK_RST} /T _{PCKC_RST}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	T _{PCCK_DBG} /T _{PCKC_DBG}	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	T _{PCCK_TRC} /T _{PCKC_TRC}	1.37/–0.41	1.57/–0.48	1.73/–0.52	ns, min
External Interrupt Controller control inputs	T _{PCCK_EIC} /T _{PCKC_EIC}	0.57/–0.22	0.66/–0.25	0.72/–0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	T _{PCKCO_DCR}	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	T _{PCKAO_DCR}	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	T _{PCKDO_DCR}	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	T _{PCKCO_CPM}	1.26	1.45	1.59	ns, max
Reset control outputs	T _{PCKCO_RST}	1.32	1.51	1.66	ns, max
Debug control outputs	T _{PCKCO_DBG}	1.94	2.22	2.44	ns, max
Trace control outputs	T _{PCKCO_TRC}	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T _{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T _{CPWL}	1.25	1.42	1.66	ns, min

Table 18: Processor Block PLB Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	T _{PCKC} _PLB/T _{PCKC} _PLB	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	T _{PCKD} _PLB/T _{PCKD} _PLB	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	T _{PCKCO} _PLB	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	T _{PCKAO} _PLB	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	T _{PCKDO} _PLB	1.44	1.65	1.81	ns, max

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in [IOB Input Switching Characteristics Standard Adjustments](#).

Table 35: IOB Input Switching Characteristics

			Speed Grade			
Description	Symbol	Device	-7	-6	-5	Units
Propagation Delays						
Pad to I output, no delay	T _{IOPI}	All	0.84	0.87	0.91	ns, max
Pad to I output, with delay	T _{IOPID}	XC2VP2	1.84	1.94	2.06	ns, max
		XC2VP4	1.84	1.94	2.06	ns, max
		XC2VP7	1.84	1.94	2.06	ns, max
		XC2VP20	2.14	2.23	2.37	ns, max
		XC2VPX20	2.14	2.23	2.37	ns, max
		XC2VP30	2.14	2.26	2.46	ns, max
		XC2VP40	2.54	2.67	2.81	ns, max
		XC2VP50	2.54	2.68	2.87	ns, max
		XC2VP70	2.54	2.72	2.91	ns, max
		XC2VPX70	2.54	2.72	2.91	ns, max
		XC2VP100	N/A	4.71	4.80	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T _{IOPLI}	All	0.86	0.89	0.93	ns, max
Pad to output IQ via transparent latch, with delay	T _{IOPLID}	XC2VP2	2.30	2.62	2.97	ns, max
		XC2VP4	2.57	2.89	3.23	ns, max
		XC2VP7	2.50	2.84	3.17	ns, max
		XC2VP20	2.65	3.04	3.42	ns, max
		XC2VPX20	2.65	3.04	3.42	ns, max
		XC2VP30	2.69	3.12	3.51	ns, max
		XC2VP40	3.30	3.63	4.03	ns, max
		XC2VP50	3.86	4.10	4.45	ns, max
		XC2VP70	4.00	4.25	4.57	ns, max
		XC2VPX70	4.00	4.25	4.57	ns, max
		XC2VP100	N/A	6.50	7.06	ns, max
Clock CLK to output IQ	T _{IOCKIQ}	All	0.60	0.60	0.67	ns, max

IOB Output Switching Characteristics Standard Adjustments

Table 38 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF} . Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 38: IOB Output Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	$T_{OLVTTTL_S2}$	5.42	6.24	6.86	ns
LVTTL, Slow, 4 mA	LVTTL_S4	$T_{OLVTTTL_S4}$	3.09	3.55	3.91	ns
LVTTL, Slow, 6 mA	LVTTL_S6	$T_{OLVTTTL_S6}$	2.26	2.60	2.86	ns
LVTTL, Slow, 8 mA	LVTTL_S8	$T_{OLVTTTL_S8}$	1.47	1.69	1.86	ns
LVTTL, Slow, 12 mA	LVTTL_S12	$T_{OLVTTTL_S12}$	1.02	1.18	1.29	ns
LVTTL, Slow, 16 mA	LVTTL_S16	$T_{OLVTTTL_S16}$	0.46	0.53	0.58	ns
LVTTL, Slow, 24 mA	LVTTL_S24	$T_{OLVTTTL_S24}$	0.37	0.42	0.47	ns
LVTTL, Fast, 2 mA	LVTTL_F2	$T_{OLVTTTL_F2}$	4.42	5.09	5.59	ns
LVTTL, Fast, 4 mA	LVTTL_F4	$T_{OLVTTTL_F4}$	1.95	2.24	2.46	ns
LVTTL, Fast, 6 mA	LVTTL_F6	$T_{OLVTTTL_F6}$	1.10	1.26	1.39	ns
LVTTL, Fast, 8 mA	LVTTL_F8	$T_{OLVTTTL_F8}$	0.40	0.46	0.51	ns
LVTTL, Fast, 12 mA	LVTTL_F12	$T_{OLVTTTL_F12}$	0.24	0.27	0.30	ns
LVTTL, Fast, 16 mA	LVTTL_F16	$T_{OLVTTTL_F16}$	0.05	0.06	0.07	ns
LVTTL, Fast, 24 mA	LVTTL_F24	$T_{OLVTTTL_F24}$	-0.01	-0.01	-0.01	ns
LVC MOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVC MOS33_S2	$T_{OLVCMOS33_S2}$	5.42	6.23	6.86	ns
LVC MOS, 3.3V, Slow, 4 mA	LVC MOS33_S4	$T_{OLVCMOS33_S4}$	3.14	3.61	3.97	ns
LVC MOS, 3.3V, Slow, 6 mA	LVC MOS33_S6	$T_{OLVCMOS33_S6}$	2.26	2.60	2.86	ns
LVC MOS, 3.3V, Slow, 8 mA	LVC MOS33_S8	$T_{OLVCMOS33_S8}$	1.47	1.69	1.86	ns
LVC MOS, 3.3V, Slow, 12 mA	LVC MOS33_S12	$T_{OLVCMOS33_S12}$	1.03	1.18	1.30	ns
LVC MOS, 3.3V, Slow, 16 mA	LVC MOS33_S16	$T_{OLVCMOS33_S16}$	0.45	0.52	0.57	ns
LVC MOS, 3.3V, Slow, 24 mA	LVC MOS33_S24	$T_{OLVCMOS33_S24}$	0.39	0.44	0.49	ns
LVC MOS, 3.3V, Fast, 2 mA	LVC MOS33_F2	$T_{OLVCMOS33_F2}$	4.46	5.13	5.64	ns
LVC MOS, 3.3V, Fast, 4 mA	LVC MOS33_F4	$T_{OLVCMOS33_F4}$	1.96	2.25	2.48	ns
LVC MOS, 3.3V, Fast, 6 mA	LVC MOS33_F6	$T_{OLVCMOS33_F6}$	1.11	1.28	1.40	ns
LVC MOS, 3.3V, Fast, 8 mA	LVC MOS33_F8	$T_{OLVCMOS33_F8}$	0.41	0.47	0.52	ns
LVC MOS, 3.3V, Fast, 12 mA	LVC MOS33_F12	$T_{OLVCMOS33_F12}$	0.23	0.26	0.28	ns
LVC MOS, 3.3V, Fast, 16 mA	LVC MOS33_F16	$T_{OLVCMOS33_F16}$	0.02	0.02	0.03	ns
LVC MOS, 3.3V, Fast, 24 mA	LVC MOS33_F24	$T_{OLVCMOS33_F24}$	-0.07	-0.08	-0.09	ns
LVC MOS, 2.5V, Slow, 2 mA	LVC MOS25_S2	$T_{OLVCMOS25_S2}$	4.12	4.74	5.21	ns
LVC MOS, 2.5V, Slow, 4 mA	LVC MOS25_S4	$T_{OLVCMOS25_S4}$	2.43	2.80	3.07	ns
LVC MOS, 2.5V, Slow, 6 mA	LVC MOS25_S6	$T_{OLVCMOS25_S6}$	1.76	2.02	2.22	ns
LVC MOS, 2.5V, Slow, 8 mA	LVC MOS25_S8	$T_{OLVCMOS25_S8}$	1.04	1.19	1.31	ns
LVC MOS, 2.5V, Slow, 12 mA	LVC MOS25_S12	$T_{OLVCMOS25_S12}$	0.76	0.87	0.96	ns
LVC MOS, 2.5V, Slow, 16 mA	LVC MOS25_S16	$T_{OLVCMOS25_S16}$	0.41	0.47	0.52	ns
LVC MOS, 2.5V, Slow, 24 mA	LVC MOS25_S24	$T_{OLVCMOS25_S24}$	0.23	0.26	0.28	ns
LVC MOS, 2.5V, Fast, 2 mA	LVC MOS25_F2	$T_{OLVCMOS25_F2}$	3.29	3.78	4.16	ns
LVC MOS, 2.5V, Fast, 4 mA	LVC MOS25_F4	$T_{OLVCMOS25_F4}$	1.31	1.50	1.65	ns

Master/Slave SelectMAP Parameters

Figure 10 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the [Virtex-II Pro Platform FPGA User Guide](#).

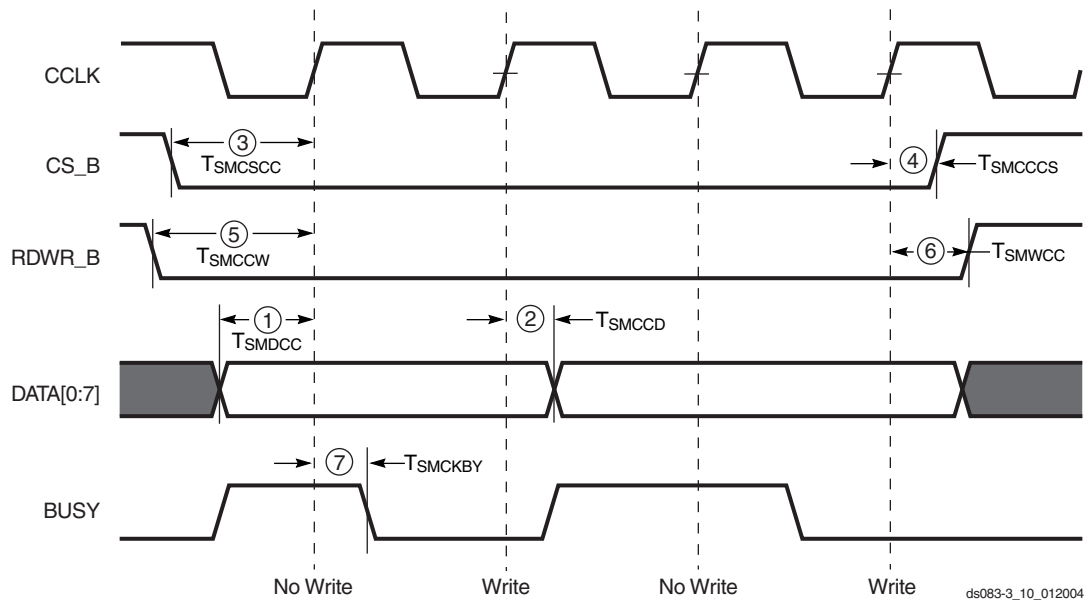


Figure 10: SelectMAP Mode Data Loading Sequence (Generic)

Table 51: SelectMAP Mode Write Timing Characteristics

	Description	Device	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	XC2VP2	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
		XC2VP4			5.0/0.0	ns, min
		XC2VP7			5.0/0.0	ns, min
		XC2VP20			5.0/0.0	ns, min
		XC2VPX20			5.0/0.0	ns, min
		XC2VP30			5.0/0.0	ns, min
		XC2VP40			5.0/0.0	ns, min
		XC2VP50			5.0/0.0	ns, min
		XC2VP70			6.0/0.0	ns, min
		XC2VPX70			6.0/0.0	ns, min
		XC2VP100			7.5/0.0	ns, min
	CS_B setup/hold		3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold		5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay		7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency			$F_{CC_STARTUP}$	50	MHz, max
	Maximum frequency			$F_{CC_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake			F_{CCNH}	50	MHz, max

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
3	IO_L05P_3	L13
3	IO_L03N_3/VREF_3	L12
3	IO_L03P_3	M13
3	IO_L02N_3	M16
3	IO_L02P_3	N16
3	IO_L01N_3/VRP_3	M15
3	IO_L01P_3/VRN_3	M14
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	P15
4	IO_L01P_4/INIT_B	P14
4	IO_L02N_4/D0/DIN ⁽¹⁾	R14
4	IO_L02P_4/D1	P13
4	IO_L03N_4/D2	T15
4	IO_L03P_4/D3	T14
4	IO_L06N_4/VRP_4	N12
4	IO_L06P_4/VRN_4	P12
4	IO_L07P_4/VREF_4	N11
4	IO_L09N_4	M11
4	IO_L09P_4/VREF_4	M10
4	IO_L69N_4	N10
4	IO_L69P_4/VREF_4	P10
4	IO_L74N_4/GCLK3S	N9
4	IO_L74P_4/GCLK2P	P9
4	IO_L75N_4/GCLK1S	R9
4	IO_L75P_4/GCLK0P	T9
5	IO_L75N_5/GCLK7S	T8
5	IO_L75P_5/GCLK6P	R8
5	IO_L74N_5/GCLK5S	P8
5	IO_L74P_5/GCLK4P	N8
5	IO_L69N_5/VREF_5	P7
5	IO_L69P_5	N7
5	IO_L09N_5/VREF_5	M7
5	IO_L09P_5	M6
5	IO_L07N_5/VREF_5	N6

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
7	IO_L85N_7	G2
7	IO_L06P_7	G3
7	IO_L06N_7	G4
7	IO_L04P_7	F1
7	IO_L04N_7/VREF_7	F2
7	IO_L03P_7	F3
7	IO_L03N_7	F4
7	IO_L02P_7	F5
7	IO_L02N_7	E4
7	IO_L01P_7/VRN_7	E2
7	IO_L01N_7/VRP_7	E3
0	VCCO_0	F8
0	VCCO_0	F7
0	VCCO_0	E8
1	VCCO_1	F9
1	VCCO_1	F10
1	VCCO_1	E9
2	VCCO_2	H12
2	VCCO_2	H11
2	VCCO_2	G11
3	VCCO_3	K11
3	VCCO_3	J12
3	VCCO_3	J11
4	VCCO_4	M9
4	VCCO_4	L9
4	VCCO_4	L10
5	VCCO_5	M8
5	VCCO_5	L8
5	VCCO_5	L7
6	VCCO_6	K6
6	VCCO_6	J6
6	VCCO_6	J5
7	VCCO_7	H6
7	VCCO_7	H5

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXTX18	AA14			
N/A	AVCCAUXRX19	AA10			
N/A	VTRXPAD19	AA9			
N/A	RXNPAD19	AB10			
N/A	RXPPAD19	AB9			
N/A	GNDA19	Y9			
N/A	TXPPAD19	AB8			
N/A	TXNPAD19	AB7			
N/A	VTTXPAD19	AA7			
N/A	AVCCAUXTX19	AA8			
N/A	AVCCAUXRX21	AA6	NC	NC	
N/A	VTRXPAD21	AA5	NC	NC	
N/A	RXNPAD21	AB6	NC	NC	
N/A	RXPPAD21	AB5	NC	NC	
N/A	GNDA21	Y6	NC	NC	
N/A	TXPPAD21	AB4	NC	NC	
N/A	TXNPAD21	AB3	NC	NC	
N/A	VTTXPAD21	AA3	NC	NC	
N/A	AVCCAUXTX21	AA4	NC	NC	
N/A	VCCINT	U6			
N/A	VCCINT	U17			
N/A	VCCINT	T8			
N/A	VCCINT	T7			
N/A	VCCINT	T16			
N/A	VCCINT	T15			
N/A	VCCINT	R7			
N/A	VCCINT	R16			
N/A	VCCINT	H7			
N/A	VCCINT	H16			
N/A	VCCINT	G8			
N/A	VCCINT	G7			
N/A	VCCINT	G16			
N/A	VCCINT	G15			
N/A	VCCINT	F6			
N/A	VCCINT	F17			
N/A	VCCAUX	M22			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
4	IO_L54N_4	V15			
4	IO_L54P_4	W15			
4	IO_L55N_4	Y15			
4	IO_L55P_4	AA15			
4	IO_L57N_4	AB15			
4	IO_L57P_4/VREF_4	AA14			
4	IO_L67N_4	AC15			
4	IO_L67P_4	AD15			
4	IO_L69N_4	V14			
4	IO_L69P_4/VREF_4	W14			
4	IO_L74N_4/GCLK3S	AB14			
4	IO_L74P_4/GCLK2P	AC14			
4	IO_L75N_4/GCLK1S	AD14			
4	IO_L75P_4/GCLK0P	AE14			
5	IO_L75N_5/GCLK7S	AE13			
5	IO_L75P_5/GCLK6P	AD13			
5	IO_L74N_5/GCLK5S	AC13			
5	IO_L74P_5/GCLK4P	AB13			
5	IO_L69N_5/VREF_5	W13			
5	IO_L69P_5	V13			
5	IO_L67N_5	AD12			
5	IO_L67P_5	AC12			
5	IO_L57N_5/VREF_5	AA13			
5	IO_L57P_5	AB12			
5	IO_L55N_5	AA12			
5	IO_L55P_5	Y12			
5	IO_L54N_5	W12			
5	IO_L54P_5	V12			
5	IO_L53_5/No_Pair	AA11			
5	IO_L50_5/No_Pair	Y11			
5	IO_L49N_5	AD10			
5	IO_L49P_5	AC10			
5	IO_L48N_5	AB11			
5	IO_L48P_5	AB10			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L43P_0	E22				
0	IO_L44N_0	E25				
0	IO_L44P_0	D25				
0	IO_L45N_0	H21				
0	IO_L45P_0/VREF_0	G21				
0	IO_L46N_0	D22				
0	IO_L46P_0	D23				
0	IO_L47N_0	D24				
0	IO_L47P_0	C24				
0	IO_L48N_0	K20				
0	IO_L48P_0	J20				
0	IO_L49N_0	F21				
0	IO_L49P_0	E21				
0	IO_L50_0/No_Pair	C21				
0	IO_L53_0/No_Pair	C22				
0	IO_L54N_0	L19				
0	IO_L54P_0	K19				
0	IO_L55N_0	G20				
0	IO_L55P_0	F20				
0	IO_L56N_0	D21				
0	IO_L56P_0	D20				
0	IO_L57N_0	J19				
0	IO_L57P_0/VREF_0	H19				
0	IO_L67N_0	G19				
0	IO_L67P_0	F19				
0	IO_L68N_0	E19				
0	IO_L68P_0	D19				
0	IO_L69N_0	L18				
0	IO_L69P_0/VREF_0	K18				
0	IO_L73N_0	G18				
0	IO_L73P_0	F18				
0	IO_L74N_0/GCLK7P	E18				
0	IO_L74P_0/GCLK6S	D18				
0	IO_L75N_0/GCLK5P	J18				
0	IO_L75P_0/GCLK4S	H18				
1	IO_L75N_1/GCLK3P	H17				
1	IO_L75P_1/GCLK2S	J17				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AG8				
N/A	GND	AG12				
N/A	GND	AG15				
N/A	GND	AG20				
N/A	GND	AG23				
N/A	GND	AG27				
N/A	GND	J34				
N/A	GND	AH7				
N/A	GND	AH28				
N/A	GND	AJ6				
N/A	GND	AJ29				
N/A	GND	AK5				
N/A	GND	AK12				
N/A	GND	AK23				
N/A	GND	AK30				
N/A	GND	AL4				
N/A	GND	AL31				
N/A	GND	AM1				
N/A	GND	AM2				
N/A	GND	AM10				
N/A	GND	AM16				
N/A	GND	AM19				
N/A	GND	AM25				
N/A	GND	AM33				
N/A	GND	AM34				
N/A	GND	AN1				
N/A	GND	AN34				

Notes:

1. See [Table 4](#) for an explanation of the signals available on this pin.

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L75N_1/GCLK3P		G21		
1	IO_L75P_1/GCLK2S		F21		
1	IO_L74N_1/GCLK1P		J21		
1	IO_L74P_1/GCLK0S		K21		
1	IO_L73N_1		D20		
1	IO_L73P_1		C20		
1	IO_L69N_1/VREF_1		F20		
1	IO_L69P_1		E20		
1	IO_L68N_1		H20		
1	IO_L68P_1		J20		
1	IO_L67N_1		L20		
1	IO_L67P_1		K20		
1	IO_L66N_1/VREF_1		M20		
1	IO_L66P_1		M21		
1	IO_L65N_1		C19		
1	IO_L65P_1		D19		
1	IO_L64N_1		F19		
1	IO_L64P_1		E19		
1	IO_L60N_1		H19		
1	IO_L60P_1		G19		
1	IO_L59N_1		K19		
1	IO_L59P_1		J19		
1	IO_L58N_1		M19		
1	IO_L58P_1		L19		
1	IO_L57N_1/VREF_1		C17		
1	IO_L57P_1		C18		
1	IO_L56N_1		E18		
1	IO_L56P_1		E17		
1	IO_L55N_1		H18		
1	IO_L55P_1		G18		
1	IO_L54N_1		L18		
1	IO_L54P_1		K18		
1	IO_L53_1/No_Pair		D17		
1	IO_L50_1/No_Pair		D16		
1	IO_L49N_1		G17		
1	IO_L49P_1		F17		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AA5		
N/A	GND		Y41		
N/A	GND		Y26		
N/A	GND		Y25		
N/A	GND		Y24		
N/A	GND		Y23		
N/A	GND		Y22		
N/A	GND		Y21		
N/A	GND		Y20		
N/A	GND		Y19		
N/A	GND		Y18		
N/A	GND		Y17		
N/A	GND		Y2		
N/A	GND		W26		
N/A	GND		W25		
N/A	GND		W24		
N/A	GND		W23		
N/A	GND		W22		
N/A	GND		W21		
N/A	GND		W20		
N/A	GND		W19		
N/A	GND		W18		
N/A	GND		W17		
N/A	GND		V37		
N/A	GND		V34		
N/A	GND		V26		
N/A	GND		V25		
N/A	GND		V24		
N/A	GND		V23		
N/A	GND		V22		
N/A	GND		V21		
N/A	GND		V20		
N/A	GND		V19		
N/A	GND		V18		
N/A	GND		V17		
N/A	GND		V9		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	VCCO_2	F4	
1	VCCO_1	R21	
1	VCCO_1	P21	
1	VCCO_1	R20	
1	VCCO_1	P20	
1	VCCO_1	R19	
1	VCCO_1	P19	
1	VCCO_1	R18	
1	VCCO_1	P18	
1	VCCO_1	H18	
1	VCCO_1	D18	
1	VCCO_1	P17	
1	VCCO_1	H14	
1	VCCO_1	D14	
1	VCCO_1	M13	
1	VCCO_1	D10	
0	VCCO_0	D33	
0	VCCO_0	M30	
0	VCCO_0	H29	
0	VCCO_0	D29	
0	VCCO_0	P26	
0	VCCO_0	R25	
0	VCCO_0	P25	
0	VCCO_0	H25	
0	VCCO_0	D25	
0	VCCO_0	R24	
0	VCCO_0	P24	
0	VCCO_0	R23	
0	VCCO_0	P23	
0	VCCO_0	R22	
0	VCCO_0	P22	
N/A	CCLK	AM10	
N/A	PROG_B	J33	
N/A	DONE	AN10	
N/A	M0	AP33	
N/A	M1	AN33	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	W16	
N/A	VCCINT	V16	
N/A	VCCINT	U16	
N/A	VCCINT	T16	
N/A	VCCINT	R16	
N/A	VCCINT	P16	
N/A	VCCINT	AJ15	
N/A	VCCINT	AH15	
N/A	VCCINT	R15	
N/A	VCCINT	P15	
N/A	VCCINT	AJ14	
N/A	VCCINT	P14	
N/A	VCCINT	AK13	
N/A	VCCINT	N13	
N/A	VCCAUX	BA42	
N/A	VCCAUX	AY42	
N/A	VCCAUX	AL42	
N/A	VCCAUX	AB42	
N/A	VCCAUX	AA42	
N/A	VCCAUX	M42	
N/A	VCCAUX	C42	
N/A	VCCAUX	B42	
N/A	VCCAUX	BB41	
N/A	VCCAUX	A41	
N/A	VCCAUX	BB40	
N/A	VCCAUX	A40	
N/A	VCCAUX	BB31	
N/A	VCCAUX	A31	
N/A	VCCAUX	BB22	
N/A	VCCAUX	A22	
N/A	VCCAUX	BB21	
N/A	VCCAUX	A21	
N/A	VCCAUX	BB12	
N/A	VCCAUX	A12	
N/A	VCCAUX	BB3	
N/A	VCCAUX	A3	
N/A	VCCAUX	BB2	