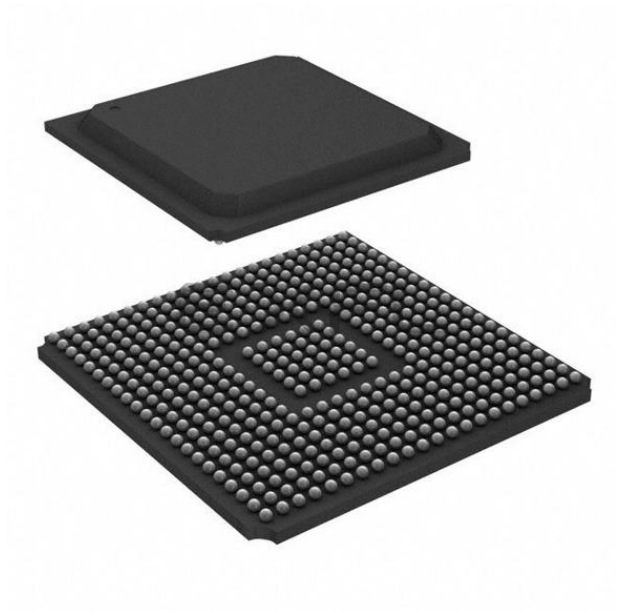
AMD Xilinx - XC2VP7-5FG456I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5fg456i

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

RXP and RXN as shown in Figure 5. This supports multiple termination styles, including high-side, low-side, and differential (floating or active). This configuration supports receiver termination compatible to Virtex-II Pro devices, using a CML (high-side) termination to an active supply of 1.8V – 2.5V. For DC coupling of two Virtex-II Pro X devices, a 1.5V CML termination for VTRX is recommended.

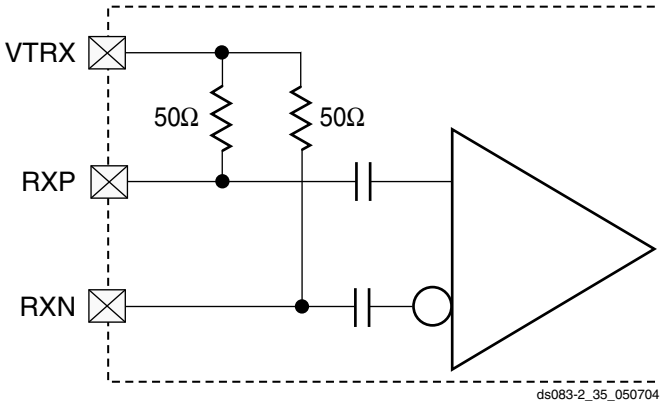


Figure 5: **RocketIO X Receive Termination**

PCS

Fabric Data Interface

Internally, the PCS operates in either 2-byte mode (16/20 bits) or 4-byte mode (32/40 bits). When in 2-byte mode, the FPGA fabric interface can either be 1, 2, or 4 bytes wide. When in 4-byte mode, the FPGA fabric interface can either be 4 or 8 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 2 summarizes the USRCLK2-to-USRCLK ratios for the different possible combinations of data widths.

Table 2: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2	
	2-Byte Internal Data Width	4-Byte Internal Data Width
1 byte	1:2 (1)	N/A
2 byte	1:1	N/A
4 byte	2:1 (1)	1:1
8 byte	N/A	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

As a general guide, use 2-byte internal data width mode when the serial speed is below 5 Gb/s, and 4-byte internal data width mode when the serial speed is greater than 5 Gb/s. In 2-byte mode, the PCS processes 4-byte data every other byte.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

64B/66B Encoder/Decoder

The RocketIO X PCS features a 64B/66B encoder/decoder, scrambler/descrambler, and gearbox functions that can be bypassed as needed. The encoder is compliant with IEEE 802.3ae specifications.

Scrambler/Gearbox

The bypassable scrambler operates on the read side of the transmit FIFO. The scrambler uses the following generator polynomial to scramble 64B/66B payload data:

$$G(x) = 1 + x^{39} + x^{58}$$

The scrambler works in conjunction with the gearbox, which frames 64B/66B data for the PMA. The gearbox should always be enabled when using the 64B/66B protocal.

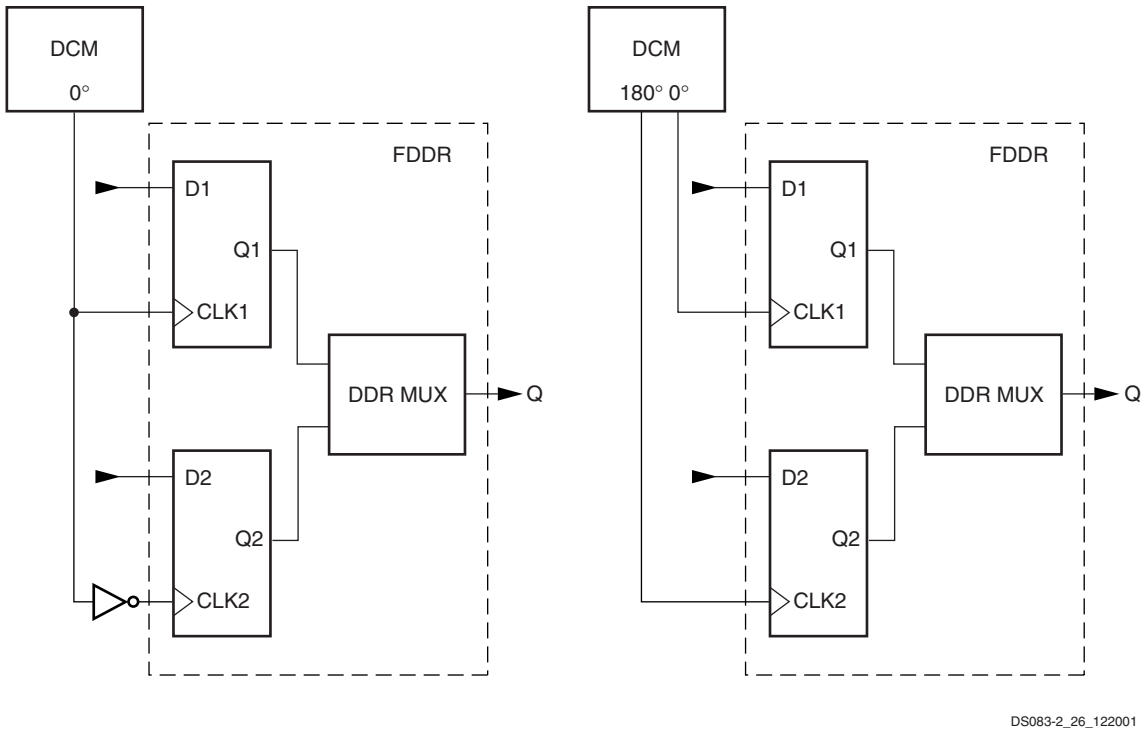


Figure 20: **Double Data Rate Registers**

This DDR mechanism can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II Pro devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals). Two neighboring IOBs have a shared routing resource connecting the ICLK and OTCLK pins on pairs of IOBs. If two adjacent IOBs using DDR registers do not share the same clock signals on their clock pins (ICLK1, ICLK2, OTCLK1, and OTCLK2), one of the clock signals will be unroutable.

The IOB pairing is identical to the LVDS IOB pairs. Hence, the package pin-out table can also be used for pin assignment to avoid conflict.

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic 1. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch, independent of all other registers or latches, can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Refer to Figure 21.

Figure 57 shows clock distribution in Virtex-II Pro devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). To reduce power consumption, any unused clock branches remain static.

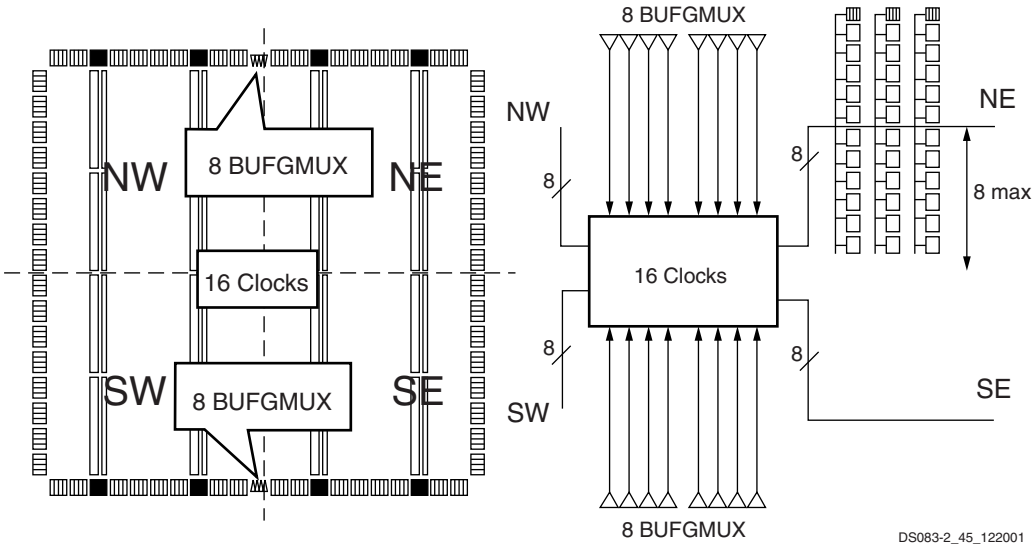


Figure 57: **Virtex-II Pro Clock Distribution**

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 58.

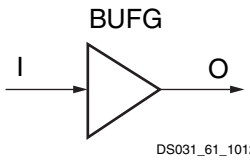


Figure 58: **Virtex-II Pro BUFG Function**

The Virtex-II Pro global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 59), as well as a two-input clock multiplexer (Figure 60). A functional description of these two options is provided below. Each of them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE and S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

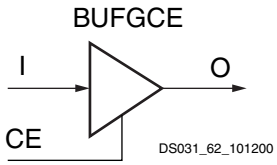


Figure 59: **Virtex-II Pro BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I_0 input, a High on S selects the I_1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II Pro device configuration using Boundary-Scan is compatible with with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 32: **Virtex-II Pro Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 33 lists the default total number of bits required to configure each device.

Table 33: **Virtex-II Pro Default Bitstream Lengths**

Device	Number of Configuration Bits
XC2VP2	1,305,376
XC2VP4	3,006,496
XC2VP7	4,485,408
XC2VP20	8,214,560
XC2VPX20	8,214,560
XC2VP30	11,589,920
XC2VP40	15,868,192
XC2VP50	19,021,344
XC2VP70	26,098,976
XC2VPX70	26,098,976
XC2VP100	34,292,768

Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2).

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on V_{CCAUX}, V_{CCO}, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device											Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VPX20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VPX70	XC2VP100	
$I_{CCINTMIN}$	500	500	500	600	600	800	1050	1250	1700	1700	2200	mA
$I_{CCAUXMIN}$	250	250	250	250	250	250	250	250	250	250	250	mA
I_{CCOMIN}	100	100	100	100	100	100	100	100	100	100	100	mA

Notes:
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Pro Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 38) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

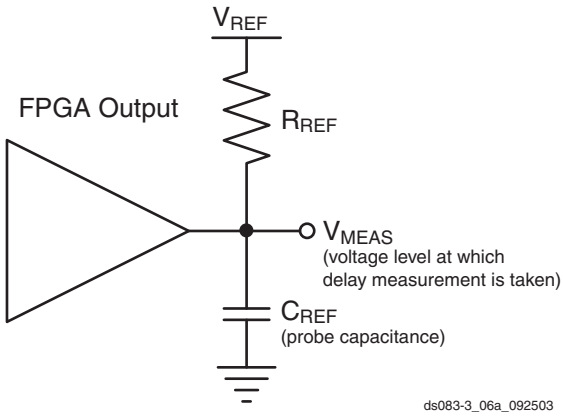


Figure 6: **Generalized Test Setup**

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.65	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	0
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Virtex-II Pro Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [TSAMP^{(1)} + TCKSKEW^{(2)} + TPKGSKEW^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/17/02	2.0	• Added new Virtex-II Pro family members. • Added timing parameters from speedsfile **v1.62**. • Added Table 46, Pipelined Multiplier Switching Characteristics. • Added 3.3V-vs-2.5V table entries for some parameters.
09/03/02	2.1	• Added Source-Synchronous Switching Characteristics section. • Added absolute max ratings for 3.3V-vs-2.5V parameters in Table 1. • Added recommended operating conditions for V_{IN} and RocketIO footnote to Table 2. • Updated SSTL2 values in Table 6. Added SSTL18 values: Table 6, Table 39, Table 32. [Table 32 removed in v2.8.] • Added Table 10, which contains LVPECL DC specifications.
09/27/02	2.2	Added section General Power Supply Requirements.
11/20/02	2.3	Updated parametric information in: • Table 1: Increase Absolute Max Rating for V_{CCO}, V_{REF}, V_{IN}, and V_{TS} from 3.6V to 3.75V. Delete cautionary footnotes related to voltage overshoot/undershoot. • Table 2: Delete V_{CCO} specifications for 2.5V and below operation. Delete footnote referencing special information for 3.3V operation. Add footnote for PCI/PCI-X. • Table 3: Add I_{BATT}. Delete I_L specifications for 2.5V and below operation. • Table 4: Add Typical Quiescent Supply Currents for XC2VP4 and XC2VP7 only • Table 6: Correct I_{OL} and I_{OH} for SSTL2 I. Add rows for LVTTL, LVCMOS33, and PCI-X. Correct max V_{IH} from V_{CCO} to 3.6V. • Table 7: Correct Min/Max V_{OD}, V_{OCM}, and V_{ICM} • Table 10: Reformat LVPECL DC Specifications to match Virtex-II data sheet format • Table 12: Correct parameter name from Differential Output Voltage to Single-Ended Output Voltage Swing. • Table 16: Add CPMC405CLOCK max frequencies • Table 27: Add footnote regarding serial data rate limitation in -5 part. • Table 39: Add rows for LVTTL, LVCMOS33, and PCI-X. • Table 32: Add LVTTL, LVCMOS33, and PCI-X. Correct all capacitive load values (except PCI/PCI-X) to 0 pF. [Table 32 removed in v2.8.] • Table 51: Correct CCLK max frequencies
11/25/02	2.4	Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.3V to –0.5V for 3.3V.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	VCCO_3	AB24			
4	VCCO_4	U14			
4	VCCO_4	U15			
4	VCCO_4	V16			
4	VCCO_4	V17			
4	VCCO_4	AC16			
4	VCCO_4	AD19			
4	VCCO_4	AD22			
5	VCCO_5	U12			
5	VCCO_5	U13			
5	VCCO_5	V10			
5	VCCO_5	V11			
5	VCCO_5	AC11			
5	VCCO_5	AD5			
5	VCCO_5	AD8			
6	VCCO_6	P10			
6	VCCO_6	R10			
6	VCCO_6	T4			
6	VCCO_6	T9			
6	VCCO_6	U9			
6	VCCO_6	W3			
6	VCCO_6	AB3			
7	VCCO_7	E3			
7	VCCO_7	H3			
7	VCCO_7	K9			
7	VCCO_7	L4			
7	VCCO_7	L9			
7	VCCO_7	M10			
7	VCCO_7	N10			
N/A	PROG_B	B1			
N/A	HSWAP_EN	B3			
N/A	DXP	A3			
N/A	DXN	C4			
N/A	AVCCAUXTX4	B5			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L44P_7	G24	NC		
7	IO_L44N_7	G23	NC		
7	IO_L43P_7	G22	NC		
7	IO_L43N_7	G21	NC		
7	IO_L42P_7	F25	NC	NC	NC
7	IO_L42N_7	F24	NC	NC	NC
7	IO_L40P_7	F23	NC	NC	NC
7	IO_L40N_7/VREF_7	F22	NC	NC	NC
7	IO_L06P_7	E26			
7	IO_L06N_7	E25			
7	IO_L05P_7	E24			
7	IO_L05N_7	E23			
7	IO_L04P_7	D26			
7	IO_L04N_7/VREF_7	D25			
7	IO_L03P_7	C26			
7	IO_L03N_7	C25			
7	IO_L02P_7	B26			
7	IO_L02N_7	A25			
7	IO_L01P_7/VRN_7	D24			
7	IO_L01N_7/VRP_7	C23			
0	VCCO_0	C17			
0	VCCO_0	C20			
0	VCCO_0	H17			
0	VCCO_0	H18			
0	VCCO_0	J14			
0	VCCO_0	J15			
0	VCCO_0	J16			
1	VCCO_1	C7			
1	VCCO_1	H9			
1	VCCO_1	C10			
1	VCCO_1	H10			
1	VCCO_1	J11			
1	VCCO_1	J12			
1	VCCO_1	J13			
2	VCCO_2	G2			
2	VCCO_2	J8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L86P_6		T23			
6	IO_L86N_6		T24			
6	IO_L87P_6		U28			
6	IO_L87N_6/VREF_6		U29			
6	IO_L88P_6		T27			
6	IO_L88N_6		T28			
6	IO_L89P_6		T25			
6	IO_L89N_6		T26			
6	IO_L90P_6		V30			
6	IO_L90N_6		U30			
7	IO_L90P_7		R28			
7	IO_L90N_7		R27			
7	IO_L89P_7		R26			
7	IO_L89N_7		R25			
7	IO_L88P_7		T29			
7	IO_L88N_7/VREF_7		R29			
7	IO_L87P_7		P27			
7	IO_L87N_7		P26			
7	IO_L86P_7		R24			
7	IO_L86N_7		R23			
7	IO_L85P_7		P29			
7	IO_L85N_7		P28			
7	IO_L60P_7		N28			
7	IO_L60N_7		N27			
7	IO_L59P_7		P24			
7	IO_L59N_7		P23			
7	IO_L58P_7		P30			
7	IO_L58N_7/VREF_7		N30			
7	IO_L57P_7		M28			
7	IO_L57N_7		M27			
7	IO_L56P_7		R22			
7	IO_L56N_7		P22			
7	IO_L55P_7		N29			
7	IO_L55N_7		M29			
7	IO_L54P_7		L27			

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L47P_3	AC10		
3	IO_L46N_3	AE7		
3	IO_L46P_3	AE8		
3	IO_L45N_3/VREF_3	AE5		
3	IO_L45P_3	AE6		
3	IO_L44N_3	AB13		
3	IO_L44P_3	AC13		
3	IO_L43N_3	AE3		
3	IO_L43P_3	AE4		
3	IO_L42N_3	AE1		
3	IO_L42P_3	AE2		
3	IO_L41N_3	AD10		
3	IO_L41P_3	AD11		
3	IO_L40N_3	AF6		
3	IO_L40P_3	AF7		
3	IO_L39N_3/VREF_3	AF4		
3	IO_L39P_3	AF5		
3	IO_L38N_3	AC12		
3	IO_L38P_3	AD12		
3	IO_L37N_3	AF1		
3	IO_L37P_3	AF2		
3	IO_L36N_3	AG6		
3	IO_L36P_3	AG7		
3	IO_L35N_3	AE9		
3	IO_L35P_3	AE10		
3	IO_L34N_3	AF3		
3	IO_L34P_3	AG3		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AE11		
3	IO_L32P_3	AE12		
3	IO_L31N_3	AH6		
3	IO_L31P_3	AH7		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AH4		
3	IO_L29N_3	AD13		
3	IO_L29P_3	AE13		
3	IO_L28N_3	AH2		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L09P_7		K36		
7	IO_L09N_7		K35		
7	IO_L08P_7		K38		
7	IO_L08N_7		K37		
7	IO_L07P_7		L33		
7	IO_L07N_7		K34		
7	IO_L84P_7		J41		
7	IO_L84N_7		J42		
7	IO_L83P_7		J39		
7	IO_L83N_7		J38		
7	IO_L82P_7		J36		
7	IO_L82N_7/VREF_7		J37		
7	IO_L81P_7		J35		
7	IO_L81N_7		H36		
7	IO_L80P_7		H41		
7	IO_L80N_7		H40		
7	IO_L79P_7		H38		
7	IO_L79N_7		H39		
7	IO_L78P_7		H37		
7	IO_L78N_7		G38		
7	IO_L77P_7		G42		
7	IO_L77N_7		G41		
7	IO_L76P_7		G39		
7	IO_L76N_7/VREF_7		G40		
7	IO_L75P_7		F41		
7	IO_L75N_7		F42		
7	IO_L74P_7		F40		
7	IO_L74N_7		F39		
7	IO_L73P_7		E41		
7	IO_L73N_7		E42		
7	IO_L06P_7		D41		
7	IO_L06N_7		D42		
7	IO_L05P_7		E40		
7	IO_L05N_7		D40		
7	IO_L04P_7		F36		
7	IO_L04N_7/VREF_7		G37		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	