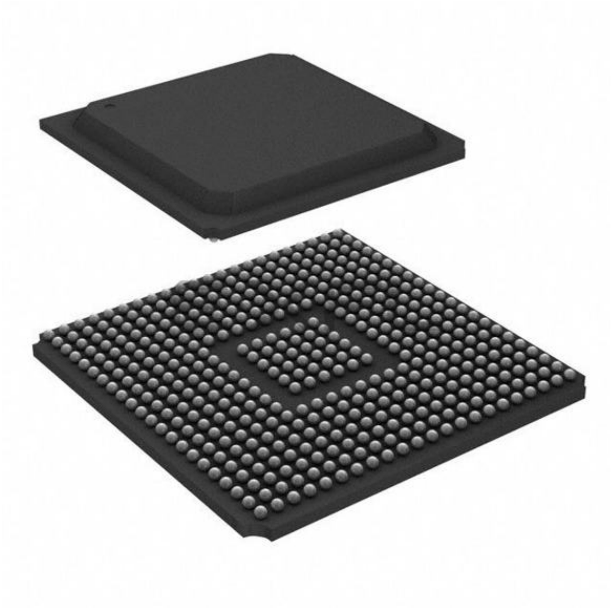


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-5fgg456i

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

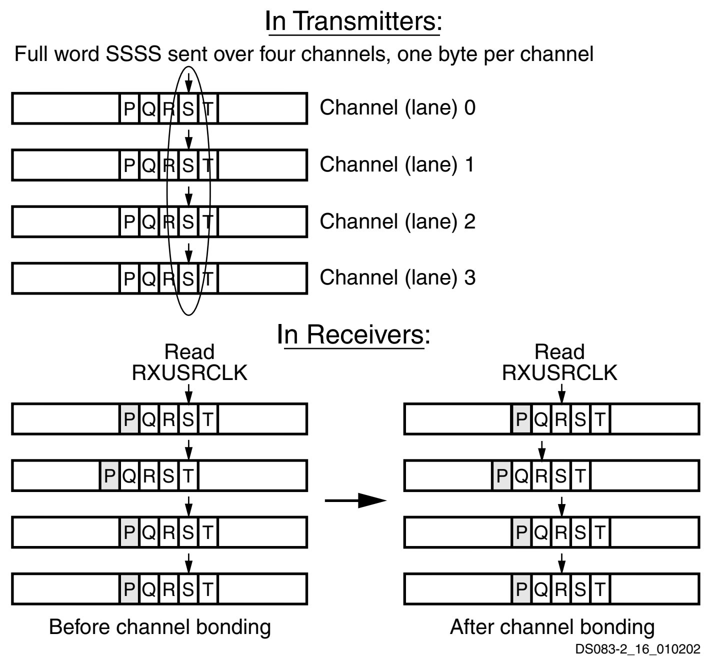


Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe PowerPC Processor Reference Guide and the PowerPC 405 Processor Block Reference Guide available on the Xilinx website at http://www.xilinx.com.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

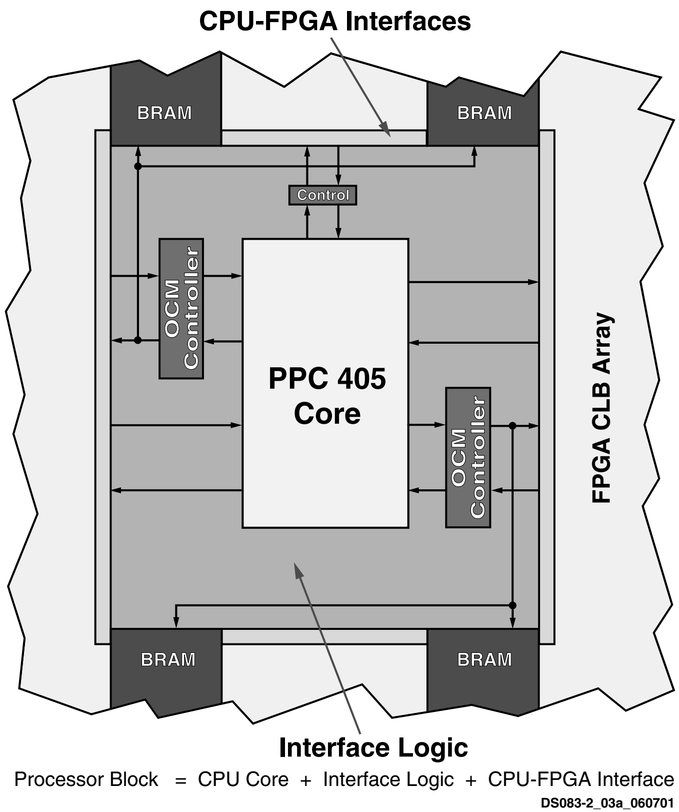


Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 μm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

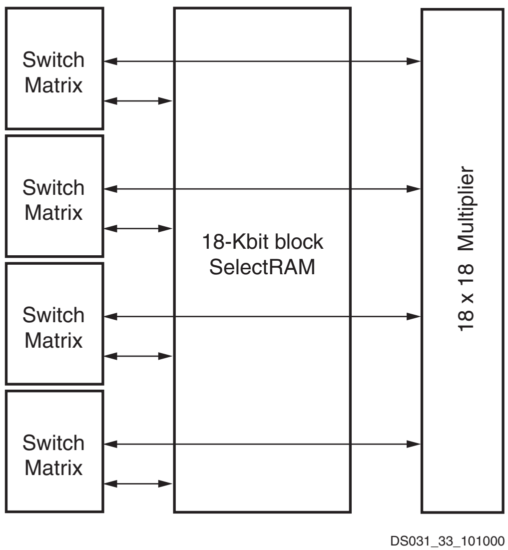


Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

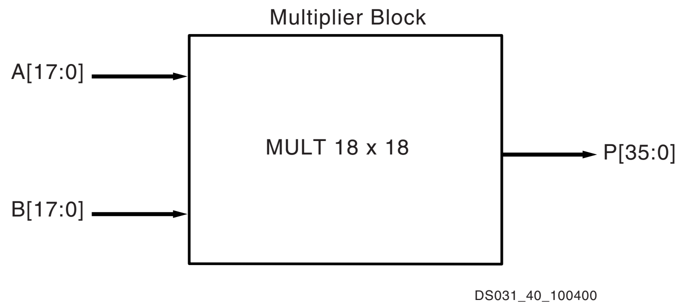


Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: **Processor Clocks Absolute AC Characteristics**

	Speed Grade						
	-7		-6		-5		
Description	Min	Max	Min	Max	Min	Max	Units
CPMC405CLOCK frequency	0	400(1)	0	350(1)	0	300	MHz
JTAGC405TCK frequency(2)	0	200	0	175	0	150	MHz
PLBCLK(3)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(3)	0	400	0	350	0	300	MHz
BRAMISOCMCLK(3)	0	400	0	350	0	300	MHz

Notes:

1. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in XAPP755, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1, Module 1 to identify dual-processor devices.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PowerPC 405 Processor Block Reference Guide*** and XAPP640 for more information.

Table 24: **RocketIO X Receiver Switching Characteristics**[1]

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance using default equalization and PRBS-15 pattern	T_{JTOL}	2.488 Gb/s		0.80	0.65	UI[2]
		3.125 Gb/s		0.80	0.65	UI
		4.25 Gb/s		0.80	0.65	UI
		6.25 Gb/s		0.80	0.65	UI
Receive random jitter tolerance	T_{RJTOL}	2.488 Gb/s		0.30		UI
		3.125 Gb/s		0.30		UI
		4.25 Gb/s		0.30		UI
		6.25 Gb/s		0.30		UI
Receive sinusoidal jitter tolerance measured at 70 MHz	T_{SJTOL}	2.488 Gb/s		0.30	0.15	UI
		3.125 Gb/s		0.30	0.15	UI
		4.25 Gb/s		0.30	0.15	UI
		6.25 Gb/s		0.30	0.15	UI
Receive deterministic jitter tolerance	T_{DJTOL}	2.488 Gb/s		0.55	0.45	UI
		3.125 Gb/s		0.55	0.45	UI
		4.25 Gb/s		0.55	0.45	UI
		6.25 Gb/s		0.50	0.45	UI
Receive latency[3]	T_{RXLAT}			25	34[4]	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%
Differential receive input sensitivity	V_{EYE}			120	250	mV

Notes:
1. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.
2. UI = Unit Interval
3. Receive latency delay RXP/RXN to RXDATA. Refer to ***RocketIO X Transceiver User Guide*** for more information on calculating latency.
4. This maximum may occur when certain conditions are present and clock correction and channel bonding are enabled. If these functions are both disabled, the maximum will be near the typical values.

Block SelectRAM+ Switching Characteristics

Table 47: **Block SelectRAM+ Switching Characteristics**

Description	Symbol	Speed Grade -7	Speed Grade -6	Speed Grade -5	Units
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	1.41	1.50	1.68	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.27/ 0.22	0.31/ 0.25	0.35/ 0.28	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.20/ 0.22	0.23/ 0.25	0.26/ 0.28	ns, min
EN input	T_{BECK}/T_{BCKE}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.33/ 0.00	0.35/ 0.00	0.39/ 0.00	ns, min
Clock CLK					
CLKA to CLKB setup time for different ports	T_{BCCS}	1.0	1.0	1.0	ns, min
Minimum Pulse Width, High	T_{BPWH}	1.17	1.30	1.50	ns, min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.30	1.50	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 48: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade -7	Speed Grade -6	Speed Grade -5	Units
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.88	1.01	1.12	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.48	0.55	0.61	ns, max
TRI input to valid data on OUT output	T_{ON}	0.48	0.55	0.61	ns, max

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade –7 Min	–7 Max	–6 Min	–6 Max	–5 Min	–5 Max	Units
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L23N_6	Y6	NC		
6	IO_L24P_6	AA4	NC		
6	IO_L24N_6	AA3	NC		
6	IO_L31P_6	AA2			
6	IO_L31N_6	AA1			
6	IO_L33P_6	Y5			
6	IO_L33N_6/VREF_6	W5			
6	IO_L35P_6	Y4			
6	IO_L35N_6	Y3			
6	IO_L36P_6	Y2			
6	IO_L36N_6	Y1			
6	IO_L37P_6	W7			
6	IO_L37N_6	W6			
6	IO_L39P_6	W2			
6	IO_L39N_6/VREF_6	W1			
6	IO_L41P_6	V8			
6	IO_L41N_6	V7			
6	IO_L42P_6	V6			
6	IO_L42N_6	V5			
6	IO_L43P_6	V4			
6	IO_L43N_6	V3			
6	IO_L45P_6	V2			
6	IO_L45N_6/VREF_6	V1			
6	IO_L47P_6	U8			
6	IO_L47N_6	T8			
6	IO_L48P_6	U5			
6	IO_L48N_6	U4			
6	IO_L49P_6	U3			
6	IO_L49N_6	T3			
6	IO_L51P_6	U2			
6	IO_L51N_6/VREF_6	U1			
6	IO_L53P_6	T7			
6	IO_L53N_6	R7			
6	IO_L54P_6	T6			
6	IO_L54N_6	T5			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L48P_2	H1	NC		
2	IO_L49N_2	J7	NC		
2	IO_L49P_2	J6	NC		
2	IO_L50N_2	J5	NC		
2	IO_L50P_2	J4	NC		
2	IO_L51N_2	J3	NC		
2	IO_L51P_2	J2	NC		
2	IO_L52N_2/VREF_2	K6	NC		
2	IO_L52P_2	K5	NC		
2	IO_L53N_2	K4	NC		
2	IO_L53P_2	K3	NC		
2	IO_L54N_2	J1	NC		
2	IO_L54P_2	K1	NC		
2	IO_L55N_2	K7	NC		
2	IO_L55P_2	L8	NC		
2	IO_L56N_2	L7	NC		
2	IO_L56P_2	M7	NC		
2	IO_L57N_2	L6	NC		
2	IO_L57P_2	L5	NC		
2	IO_L58N_2/VREF_2	L4	NC		
2	IO_L58P_2	L3	NC		
2	IO_L59N_2	L2	NC		
2	IO_L59P_2	L1	NC		
2	IO_L60N_2	M8	NC		
2	IO_L60P_2	N8	NC		
2	IO_L85N_2	M6			
2	IO_L85P_2	M5			
2	IO_L86N_2	M4			
2	IO_L86P_2	M3			
2	IO_L87N_2	M2			
2	IO_L87P_2	M1			
2	IO_L88N_2/VREF_2	N7			
2	IO_L88P_2	N6			
2	IO_L89N_2	N5			
2	IO_L89P_2	N4			
2	IO_L90N_2	N3			
2	IO_L90P_2	N2			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L05_4/No_Pair	Y8			
4	IO_L06N_4/VRP_4	AB8			
4	IO_L06P_4/VRN_4	AB9			
4	IO_L07N_4	AC8			
4	IO_L07P_4/VREF_4	AD8			
4	IO_L08N_4	AE8			
4	IO_L08P_4	AF8			
4	IO_L09N_4	Y9			
4	IO_L09P_4/VREF_4	AA9			
4	IO_L37N_4	AC9	NC	NC	
4	IO_L37P_4	AD9	NC	NC	
4	IO_L38N_4	Y10	NC	NC	
4	IO_L38P_4	W11	NC	NC	
4	IO_L39N_4	AA10	NC	NC	
4	IO_L39P_4	AA11	NC	NC	
4	IO_L43N_4	AB10	NC	NC	
4	IO_L43P_4	AC10	NC	NC	
4	IO_L44N_4	Y11	NC	NC	
4	IO_L44P_4	Y12	NC	NC	
4	IO_L45N_4	AB11	NC	NC	
4	IO_L45P_4/VREF_4	AC11	NC	NC	
4	IO_L67N_4	AA12			
4	IO_L67P_4	AB12			
4	IO_L68N_4	AC12			
4	IO_L68P_4	AD12			
4	IO_L69N_4	W12			
4	IO_L69P_4/VREF_4	W13			
4	IO_L73N_4	Y13			
4	IO_L73P_4	AA13			
4	IO_L74N_4/GCLK3S	AB13			
4	IO_L74P_4/GCLK2P	AC13			
4	IO_L75N_4/GCLK1S	AD13			
4	IO_L75P_4/GCLK0P	AE13			
5	IO_L75N_5/GCLK7S	AE14			
5	IO_L75P_5/GCLK6P	AD14			
5	IO_L74N_5/GCLK5S	AC14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	VCCO_2	K2			
2	VCCO_2	K8			
2	VCCO_2	L9			
2	VCCO_2	M9			
2	VCCO_2	N9			
3	VCCO_3	P9			
3	VCCO_3	R9			
3	VCCO_3	T9			
3	VCCO_3	U2			
3	VCCO_3	U8			
3	VCCO_3	V8			
3	VCCO_3	Y2			
4	VCCO_4	W9			
4	VCCO_4	AD7			
4	VCCO_4	V11			
4	VCCO_4	V12			
4	VCCO_4	V13			
4	VCCO_4	W10			
4	VCCO_4	AD10			
5	VCCO_5	V14			
5	VCCO_5	V15			
5	VCCO_5	V16			
5	VCCO_5	W17			
5	VCCO_5	W18			
5	VCCO_5	AD17			
5	VCCO_5	AD20			
6	VCCO_6	P18			
6	VCCO_6	R18			
6	VCCO_6	T18			
6	VCCO_6	U19			
6	VCCO_6	U25			
6	VCCO_6	V19			
6	VCCO_6	Y25			
7	VCCO_7	G25			
7	VCCO_7	J19			
7	VCCO_7	K19			
7	VCCO_7	K25			

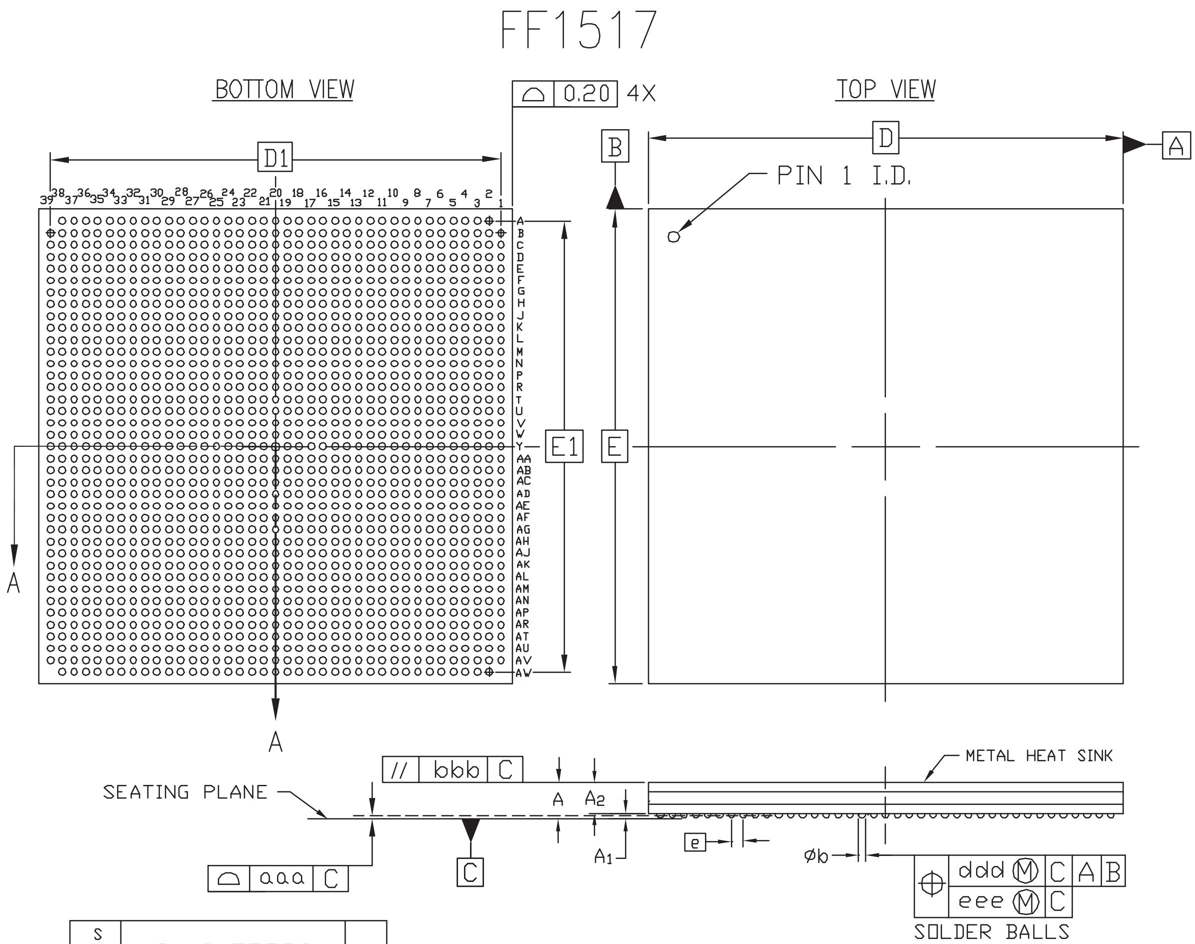
Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

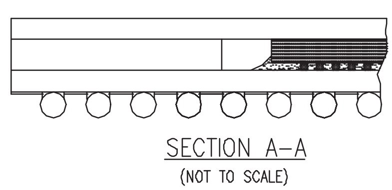
Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L36N_7		F27	NC		
7	IO_L35P_7		K24	NC		
7	IO_L35N_7		K23	NC		
7	IO_L34P_7		E30	NC		
7	IO_L34N_7/VREF_7		E29	NC		
7	IO_L33P_7		E28	NC		
7	IO_L33N_7		E27	NC		
7	IO_L32P_7		H26	NC		
7	IO_L32N_7		H25	NC		
7	IO_L31P_7		D30	NC		
7	IO_L31N_7		D29	NC		
7	IO_L06P_7		D28			
7	IO_L06N_7		C27			
7	IO_L05P_7		J24			
7	IO_L05N_7		J23			
7	IO_L04P_7		C30			
7	IO_L04N_7/VREF_7		C29			
7	IO_L03P_7		D26			
7	IO_L03N_7		C26			
7	IO_L02P_7		G26			
7	IO_L02N_7		G25			
7	IO_L01P_7/VRN_7		B28			
7	IO_L01N_7/VRP_7		A28			
0	VCCO_0		K21			
0	VCCO_0		K20			
0	VCCO_0		K19			
0	VCCO_0		K18			
0	VCCO_0		K17			
0	VCCO_0		K16			
0	VCCO_0		J21			
0	VCCO_0		J20			
0	VCCO_0		J19			
0	VCCO_0		J18			
1	VCCO_1		K15			
1	VCCO_1		K14			

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)





SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	—	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	—	—	2.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 8: **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L53N_3		AE10		
3	IO_L53P_3		AE11		
3	IO_L52N_3		AE1		
3	IO_L52P_3		AE2		
3	IO_L51N_3/VREF_3		AE4		
3	IO_L51P_3		AE5		
3	IO_L50N_3		AF11		
3	IO_L50P_3		AE12		
3	IO_L49N_3		AE7		
3	IO_L49P_3		AE8		
3	IO_L48N_3		AF1		
3	IO_L48P_3		AF2		
3	IO_L47N_3		AG12		
3	IO_L47P_3		AF12		
3	IO_L46N_3		AF3		
3	IO_L46P_3		AF4		
3	IO_L45N_3/VREF_3		AF5		
3	IO_L45P_3		AF6		
3	IO_L44N_3		AF7		
3	IO_L44P_3		AF8		
3	IO_L43N_3		AF9		
3	IO_L43P_3		AF10		
3	IO_L42N_3		AG2		
3	IO_L42P_3		AG3		
3	IO_L41N_3		AG10		
3	IO_L41P_3		AG11		
3	IO_L40N_3		AG4		
3	IO_L40P_3		AG5		
3	IO_L39N_3/VREF_3		AG6		
3	IO_L39P_3		AG7		
3	IO_L38N_3		AG8		
3	IO_L38P_3		AH8		
3	IO_L37N_3		AH1		
3	IO_L37P_3		AH2		
3	IO_L36N_3		AH3		
3	IO_L36P_3		AJ3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L52N_6		AE42		
6	IO_L53P_6		AE32		
6	IO_L53N_6		AE33		
6	IO_L54P_6		AD35		
6	IO_L54N_6		AD36		
6	IO_L55P_6		AD37		
6	IO_L55N_6		AD38		
6	IO_L56P_6		AD31		
6	IO_L56N_6		AD32		
6	IO_L57P_6		AD39		
6	IO_L57N_6/VREF_6		AD40		
6	IO_L58P_6		AD41		
6	IO_L58N_6		AD42		
6	IO_L59P_6		AD33		
6	IO_L59N_6		AD34		
6	IO_L60P_6		AC33		
6	IO_L60N_6		AC34		
6	IO_L85P_6		AC36		
6	IO_L85N_6		AC37		
6	IO_L86P_6		AC31		
6	IO_L86N_6		AC32		
6	IO_L87P_6		AC39		
6	IO_L87N_6/VREF_6		AC40		
6	IO_L88P_6		AB33		
6	IO_L88N_6		AB34		
6	IO_L89P_6		AB36		
6	IO_L89N_6		AB37		
6	IO_L90P_6		AB39		
6	IO_L90N_6		AB40		
7	IO_L90P_7		AA39		
7	IO_L90N_7		AA40		
7	IO_L89P_7		AB31		
7	IO_L89N_7		AA31		
7	IO_L88P_7		AA36		
7	IO_L88N_7/VREF_7		AA37		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L75N_2	C5	
2	IO_L75P_2	B5	
2	IO_L76N_2/VREF_2	D7	
2	IO_L76P_2	C6	
2	IO_L77N_2	H8	
2	IO_L77P_2	H9	
2	IO_L78N_2	C3	
2	IO_L78P_2	C4	
2	IO_L79N_2	D1	
2	IO_L79P_2	D2	
2	IO_L80N_2	J8	
2	IO_L80P_2	K9	
2	IO_L81N_2	E6	
2	IO_L81P_2	D5	
2	IO_L82N_2/VREF_2	E4	
2	IO_L82P_2	D4	
2	IO_L83N_2	L8	
2	IO_L83P_2	L9	
2	IO_L84N_2	E3	
2	IO_L84P_2	D3	
2	IO_L61N_2	F8	
2	IO_L61P_2	E8	
2	IO_L62N_2	M8	
2	IO_L62P_2	M9	
2	IO_L63N_2	F7	
2	IO_L63P_2	E7	
2	IO_L64N_2/VREF_2	F3	
2	IO_L64P_2	E2	
2	IO_L65N_2	N12	
2	IO_L65P_2	P12	
2	IO_L66N_2	F1	
2	IO_L66P_2	F2	
2	IO_L67N_2	G7	
2	IO_L67P_2	G8	
2	IO_L68N_2	N10	
2	IO_L68P_2	N11	
2	IO_L69N_2	G6	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L87P_7	AA37	
7	IO_L87N_7	AA38	
7	IO_L86P_7	AA33	
7	IO_L86N_7	AA34	
7	IO_L85P_7	Y40	
7	IO_L85N_7	Y41	
7	IO_L60P_7	W41	
7	IO_L60N_7	W42	
7	IO_L59P_7	AA31	
7	IO_L59N_7	AA32	
7	IO_L58P_7	V40	
7	IO_L58N_7/VREF_7	W40	
7	IO_L57P_7	W37	
7	IO_L57N_7	W38	
7	IO_L56P_7	Y36	
7	IO_L56N_7	Y37	
7	IO_L55P_7	V41	
7	IO_L55N_7	V42	
7	IO_L54P_7	V38	
7	IO_L54N_7	V39	
7	IO_L53P_7	Y31	
7	IO_L53N_7	Y32	
7	IO_L52P_7	U40	
7	IO_L52N_7/VREF_7	U41	
7	IO_L51P_7	T40	
7	IO_L51N_7	U39	
7	IO_L50P_7	Y35	
7	IO_L50N_7	W36	
7	IO_L49P_7	T37	
7	IO_L49N_7	U37	
7	IO_L48P_7	T41	
7	IO_L48N_7	T42	
7	IO_L47P_7	Y33	
7	IO_L47N_7	W34	
7	IO_L46P_7	T38	
7	IO_L46N_7/VREF_7	T39	
7	IO_L45P_7	R36	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	