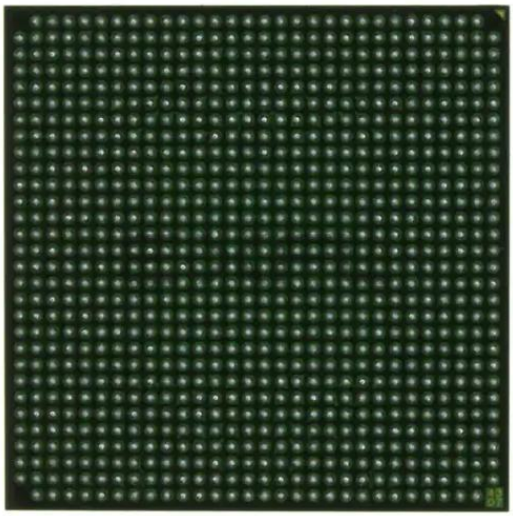

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-6ff896i

- Programmable Receiver Equalization
- Internal AC Coupling
- On-Chip 50Ω Termination
  - Eliminates the need for external termination resistors
- Pre- and Post-Driver Serial and Parallel TX-to-RX Internal Loopback Modes for Testing Operability
- Programmable Comma Detection
  - Allows for any protocol
  - Allows for detection of any 10-bit character
- 8B/10B and 64B/66B Encoding Blocks

RocketIO Transceiver Features (All Except XC2VPX20 and XC2VPX70)

- Full-Duplex Serial Transceiver (SERDES) Capable of Baud Rates from 600 Mb/s to 3.125 Gb/s
- 100 Gb/s Duplex Data Rate (20 Channels)
- Monolithic Clock Synthesis and Clock Recovery (CDR)
- Fibre Channel, 10G Fibre Channel, Gigabit Ethernet, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-Compliant Transceivers
- 8-, 16-, or 32-bit Selectable Internal FPGA Interface
- 8B/10B Encoder and Decoder (optional)
- 50Ω/75Ω on-chip Selectable Transmit and Receive Terminations
- Programmable Comma Detection
- Channel Bonding Support (from 2 to 20 Channels)
- Rate Matching via Insertion/Deletion Characters
- Four Levels of Selectable Pre-Emphasis
- Five Levels of Output Differential Voltage
- Per-Channel Internal Loopback Modes
- 2.5V Transceiver Supply Voltage

PowerPC RISC Processor Block Features (All Except XC2VP2)

- Embedded 300+ MHz Harvard Architecture Block
- Low Power Consumption: 0.9 mW/MHz
- Five-Stage Data Path Pipeline
- Hardware Multiply/Divide Unit
- Thirty-Two 32-bit General Purpose Registers
- 16 KB Two-Way Set-Associative Instruction Cache
- 16 KB Two-Way Set-Associative Data Cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 KB to 16 MB)
- Dedicated On-Chip Memory (OCM) Interface
- Supports IBM CoreConnect™ Bus Architecture
- Debug and Trace Support
- Timer Facilities

Virtex-II Pro Platform FPGA Technology (All Devices)

- SelectRAM+ Memory Hierarchy
  - Up to 8 Mb of True Dual-Port RAM in 18 Kb block SelectRAM+ resources
  - Up to 1,378 Kb of distributed SelectRAM+ resources
  - High-performance interfaces to external memory
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 88,192 internal registers/latches with Clock Enable
  - Up to 88,192 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-Performance Clock Management Circuitry
  - Up to twelve Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect Technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- SelectIO™-Ultra Technology
  - Up to 1,164 user I/Os
  - Twenty-two single-ended standards and ten differential standards
  - Programmable LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - XCITE Digitally Controlled Impedance (DCI) I/O
  - PCI/PCI-X support [1]
  - Differential signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - On-chip differential termination
    - Bus LVDS I/O

1. Refer to XAPP653 for more information.

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II Pro device configuration using Boundary-Scan is compatible with with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 32: **Virtex-II Pro Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 33 lists the default total number of bits required to configure each device.

Table 33: **Virtex-II Pro Default Bitstream Lengths**

Device	Number of Configuration Bits
XC2VP2	1,305,376
XC2VP4	3,006,496
XC2VP7	4,485,408
XC2VP20	8,214,560
XC2VPX20	8,214,560
XC2VP30	11,589,920
XC2VP40	15,868,192
XC2VP50	19,021,344
XC2VP70	26,098,976
XC2VPX70	26,098,976
XC2VP100	34,292,768

Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Master/Slave SelectMAP Parameters

Figure 10 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

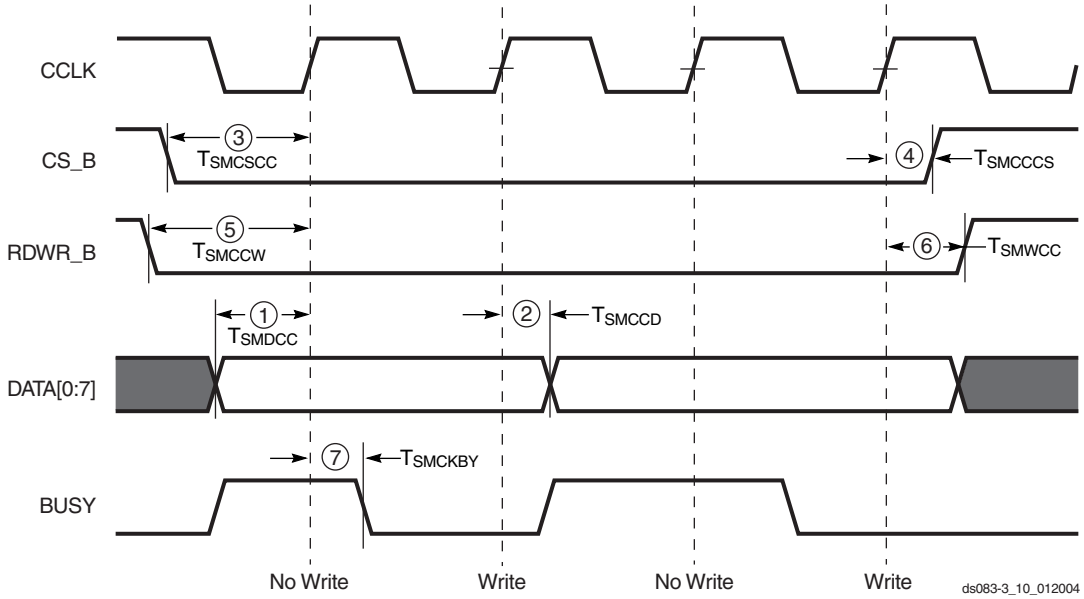

Figure 10: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 51: **SelectMAP Mode Write Timing Characteristics**

	Description	Device	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	XC2VP2	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
		XC2VP4			5.0/0.0	ns, min
		XC2VP7			5.0/0.0	ns, min
		XC2VP20			5.0/0.0	ns, min
		XC2VPX20			5.0/0.0	ns, min
		XC2VP30			5.0/0.0	ns, min
		XC2VP40			5.0/0.0	ns, min
		XC2VP50			5.0/0.0	ns, min
		XC2VP70			6.0/0.0	ns, min
		XC2VPX70			6.0/0.0	ns, min
		XC2VP100			7.5/0.0	ns, min
	CS_B setup/hold		3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold		5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay		7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency			$F_{CC_STARTUP}$	50	MHz, max
	Maximum frequency			$F_{CC_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake			F_{CCNH}	50	MHz, max

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package(1)									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L57P_3		Y1			
3	IO_L56N_3		U7			
3	IO_L56P_3		U8			
3	IO_L55N_3		V5			
3	IO_L55P_3		V6			
3	IO_L54N_3		Y2			
3	IO_L54P_3		AA2			
3	IO_L53N_3		V7			
3	IO_L53P_3		V8			
3	IO_L52N_3		W3			
3	IO_L52P_3		W4			
3	IO_L51N_3/VREF_3		AA1			
3	IO_L51P_3		AB1			
3	IO_L50N_3		W5			
3	IO_L50P_3		W6			
3	IO_L49N_3		Y4			
3	IO_L49P_3		Y5			
3	IO_L48N_3		AA3			
3	IO_L48P_3		AA4			
3	IO_L47N_3		W7			
3	IO_L47P_3		W8			
3	IO_L46N_3		AB3			
3	IO_L46P_3		AB4			
3	IO_L45N_3/VREF_3		AB2			
3	IO_L45P_3		AC2			
3	IO_L44N_3		AA5			
3	IO_L44P_3		AA6			
3	IO_L43N_3		AC3			
3	IO_L43P_3		AC4			
3	IO_L42N_3		AD1	NC		
3	IO_L42P_3		AD2	NC		
3	IO_L41N_3		Y7	NC		
3	IO_L41P_3		Y8	NC		
3	IO_L40N_3		AB5	NC		
3	IO_L40P_3		AB6	NC		
3	IO_L39N_3/VREF_3		AE1	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L36N_7		F27	NC		
7	IO_L35P_7		K24	NC		
7	IO_L35N_7		K23	NC		
7	IO_L34P_7		E30	NC		
7	IO_L34N_7/VREF_7		E29	NC		
7	IO_L33P_7		E28	NC		
7	IO_L33N_7		E27	NC		
7	IO_L32P_7		H26	NC		
7	IO_L32N_7		H25	NC		
7	IO_L31P_7		D30	NC		
7	IO_L31N_7		D29	NC		
7	IO_L06P_7		D28			
7	IO_L06N_7		C27			
7	IO_L05P_7		J24			
7	IO_L05N_7		J23			
7	IO_L04P_7		C30			
7	IO_L04N_7/VREF_7		C29			
7	IO_L03P_7		D26			
7	IO_L03N_7		C26			
7	IO_L02P_7		G26			
7	IO_L02N_7		G25			
7	IO_L01P_7/VRN_7		B28			
7	IO_L01N_7/VRP_7		A28			
0	VCCO_0		K21			
0	VCCO_0		K20			
0	VCCO_0		K19			
0	VCCO_0		K18			
0	VCCO_0		K17			
0	VCCO_0		K16			
0	VCCO_0		J21			
0	VCCO_0		J20			
0	VCCO_0		J19			
0	VCCO_0		J18			
1	VCCO_1		K15			
1	VCCO_1		K14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		AG19			
N/A	GND		AG12			
N/A	GND		AG9			
N/A	GND		AG4			
N/A	GND		AF26			
N/A	GND		AF5			
N/A	GND		AE25			
N/A	GND		AE18			
N/A	GND		AE13			
N/A	GND		AE6			
N/A	GND		AC30			
N/A	GND		AC1			
N/A	GND		Y28			
N/A	GND		Y25			
N/A	GND		Y20			
N/A	GND		Y11			
N/A	GND		Y6			
N/A	GND		Y3			
N/A	GND		W19			
N/A	GND		W18			
N/A	GND		W17			
N/A	GND		W16			
N/A	GND		W15			
N/A	GND		W14			
N/A	GND		W13			
N/A	GND		W12			
N/A	GND		V19			
N/A	GND		V18			
N/A	GND		V17			
N/A	GND		V16			
N/A	GND		V15			
N/A	GND		V14			
N/A	GND		V13			
N/A	GND		V12			
N/A	GND		U25			
N/A	GND		U19			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L37N_1	G13				
1	IO_L37P_1	H13				
1	IO_L27N_1/VREF_1	J13	NC	NC		
1	IO_L27P_1	K13	NC	NC		
1	IO_L26N_1	D8	NC	NC		
1	IO_L26P_1	E8	NC	NC		
1	IO_L25N_1	F12	NC	NC		
1	IO_L25P_1	G12	NC	NC		
1	IO_L21N_1	G11	NC	NC		
1	IO_L21P_1	H11	NC	NC		
1	IO_L20N_1	C7	NC	NC		
1	IO_L20P_1	D7	NC	NC		
1	IO_L19N_1	E11	NC	NC		
1	IO_L19P_1	F11	NC	NC		
1	IO_L09N_1/VREF_1	J12				
1	IO_L09P_1	K12				
1	IO_L08N_1	D6				
1	IO_L08P_1	D5				
1	IO_L07N_1	E9				
1	IO_L07P_1	F9				
1	IO_L06N_1	J11				
1	IO_L06P_1	K11				
1	IO_L05_1/No_Pair	J10				
1	IO_L03N_1/VREF_1	G10				
1	IO_L03P_1	H10				
1	IO_L02N_1	G9				
1	IO_L02P_1	H9				
1	IO_L01N_1/VRP_1	E7				
1	IO_L01P_1/VRN_1	E6				
2	IO_L01N_2/VRP_2	D2				
2	IO_L01P_2/VRN_2	D1				
2	IO_L02N_2	F8				
2	IO_L02P_2	F7				
2	IO_L03N_2	E4				
2	IO_L03P_2	E3				
2	IO_L04N_2/VREF_2	E2				
2	IO_L04P_2	E1				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	VCCO_1	H15		
1	VCCO_1	D15		
1	VCCO_1	M14		
1	VCCO_1	M13		
1	VCCO_1	L12		
1	VCCO_1	H11		
1	VCCO_1	D11		
0	VCCO_0	H24		
0	VCCO_0	D24		
0	VCCO_0	L23		
0	VCCO_0	M22		
0	VCCO_0	M21		
0	VCCO_0	M20		
0	VCCO_0	H20		
0	VCCO_0	D20		
0	VCCO_0	M19		
0	VCCO_0	M18		
N/A	CCLK	AG9		
N/A	PROG_B	G26		
N/A	DONE	AF10		
N/A	M0	AG25		
N/A	M1	AG26		
N/A	M2	AF25		
N/A	TCK	G9		
N/A	TDI	F26		
N/A	TDO	F9		
N/A	TMS	H10		
N/A	PWRDWN_B	AG10		
N/A	HSWAP_EN	H25		
N/A	RSVD	H9		
N/A	VBATT	J10		
N/A	DXP	J25		
N/A	DXN	H26		
N/A	VCCINT	AD24		
N/A	VCCINT	L24		
N/A	VCCINT	AC23		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L49N_2	U5		
2	IO_L49P_2	U6		
2	IO_L50N_2	U13		
2	IO_L50P_2	V13		
2	IO_L51N_2	U4		
2	IO_L51P_2	T4		
2	IO_L52N_2/VREF_2	U1		
2	IO_L52P_2	U2		
2	IO_L53N_2	V9		
2	IO_L53P_2	V10		
2	IO_L54N_2	V7		
2	IO_L54P_2	V8		
2	IO_L55N_2	V5		
2	IO_L55P_2	V6		
2	IO_L56N_2	V11		
2	IO_L56P_2	V12		
2	IO_L57N_2	V3		
2	IO_L57P_2	V4		
2	IO_L58N_2/VREF_2	V1		
2	IO_L58P_2	V2		
2	IO_L59N_2	W10		
2	IO_L59P_2	W11		
2	IO_L60N_2	W7		
2	IO_L60P_2	W8		
2	IO_L85N_2	W5		
2	IO_L85P_2	W6		
2	IO_L86N_2	W12		
2	IO_L86P_2	W13		
2	IO_L87N_2	W3		
2	IO_L87P_2	W4		
2	IO_L88N_2/VREF_2	Y7		
2	IO_L88P_2	Y8		
2	IO_L89N_2	W9		
2	IO_L89P_2	Y9		
2	IO_L90N_2	Y3		
2	IO_L90P_2	Y4		
3	IO_L90N_3	AA7		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L09P_3	AM3		
3	IO_L08N_3	AK8		
3	IO_L08P_3	AK9		
3	IO_L07N_3	AN6		
3	IO_L07P_3	AN7		
3	IO_L84N_3	AN3	NC	
3	IO_L84P_3	AN4	NC	
3	IO_L82N_3	AN1	NC	
3	IO_L82P_3	AN2	NC	
3	IO_L81N_3/VREF_3	AN5	NC	
3	IO_L81P_3	AP5	NC	
3	IO_L79N_3	AP3	NC	
3	IO_L79P_3	AP4	NC	
3	IO_L78N_3	AP1	NC	
3	IO_L78P_3	AP2	NC	
3	IO_L76N_3	AR2	NC	
3	IO_L76P_3	AR3	NC	
3	IO_L75N_3/VREF_3	AT1	NC	
3	IO_L75P_3	AT2	NC	
3	IO_L73N_3	AT5	NC	
3	IO_L73P_3	AU5	NC	
3	IO_L06N_3	AR6		
3	IO_L06P_3	AT6		
3	IO_L05N_3	AL9		
3	IO_L05P_3	AM8		
3	IO_L04N_3	AP7		
3	IO_L04P_3	AR7		
3	IO_L03N_3/VREF_3	AM9		
3	IO_L03P_3	AN9		
3	IO_L02N_3	AR8		
3	IO_L02P_3	AT8		
3	IO_L01N_3/VRP_3	AT7		
3	IO_L01P_3/VRN_3	AU7		
4	IO_L01N_4/BUSY/DOUT(1)	AT9		
4	IO_L01P_4/INIT_B	AR9		
4	IO_L02N_4/D0/DIN(1)	AK11		
4	IO_L02P_4/D1	AK12		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L43N_7	R37		
7	IO_L42P_7	R34		
7	IO_L42N_7	R35		
7	IO_L41P_7	U28		
7	IO_L41N_7	T28		
7	IO_L40P_7	R32		
7	IO_L40N_7/VREF_7	R33		
7	IO_L39P_7	P38		
7	IO_L39N_7	P39		
7	IO_L38P_7	T29		
7	IO_L38N_7	T30		
7	IO_L37P_7	N37		
7	IO_L37N_7	P37		
7	IO_L36P_7	P35		
7	IO_L36N_7	P36		
7	IO_L35P_7	T27		
7	IO_L35N_7	R27		
7	IO_L34P_7	P33		
7	IO_L34N_7/VREF_7	P34		
7	IO_L33P_7	N38		
7	IO_L33N_7	N39		
7	IO_L32P_7	R28		
7	IO_L32N_7	R29		
7	IO_L31P_7	N35		
7	IO_L31N_7	M36		
7	IO_L30P_7	N33		
7	IO_L30N_7	N34		
7	IO_L29P_7	R30		
7	IO_L29N_7	R31		
7	IO_L28P_7	M37		
7	IO_L28N_7/VREF_7	M38		
7	IO_L27P_7	M33		
7	IO_L27N_7	M34		
7	IO_L26P_7	P28		
7	IO_L26N_7	P29		
7	IO_L25P_7	L38		
7	IO_L25N_7	L39		
7	IO_L24P_7	L36		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L87P_7		AA33		
7	IO_L87N_7		AA34		
7	IO_L86P_7		Y31		
7	IO_L86N_7		Y32		
7	IO_L85P_7		Y39		
7	IO_L85N_7		Y40		
7	IO_L60P_7		Y36		
7	IO_L60N_7		Y37		
7	IO_L59P_7		Y33		
7	IO_L59N_7		Y34		
7	IO_L58P_7		W41		
7	IO_L58N_7/VREF_7		W42		
7	IO_L57P_7		W39		
7	IO_L57N_7		W40		
7	IO_L56P_7		W31		
7	IO_L56N_7		W32		
7	IO_L55P_7		W37		
7	IO_L55N_7		W38		
7	IO_L54P_7		W35		
7	IO_L54N_7		W36		
7	IO_L53P_7		W33		
7	IO_L53N_7		W34		
7	IO_L52P_7		V41		
7	IO_L52N_7/VREF_7		V42		
7	IO_L51P_7		V38		
7	IO_L51N_7		V39		
7	IO_L50P_7		V31		
7	IO_L50N_7		U32		
7	IO_L49P_7		V35		
7	IO_L49N_7		V36		
7	IO_L48P_7		V32		
7	IO_L48N_7		V33		
7	IO_L47P_7		U31		
7	IO_L47N_7		T31		
7	IO_L46P_7		U41		
7	IO_L46N_7/VREF_7		U42		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCAUX		AM11		
N/A	VCCAUX		AN33		
N/A	VCCAUX		AN10		
N/A	VCCAUX		AV39		
N/A	VCCAUX		AV4		
N/A	VCCAUX		AW38		
N/A	VCCAUX		AW22		
N/A	VCCAUX		AW21		
N/A	VCCAUX		AW5		
N/A	VCCAUX		AA42		
N/A	VCCAUX		AA41		
N/A	VCCAUX		AA2		
N/A	VCCAUX		AA1		
N/A	VCCAUX		Y42		
N/A	VCCAUX		Y1		
N/A	VCCAUX		L32		
N/A	VCCAUX		L11		
N/A	VCCAUX		K33		
N/A	VCCAUX		K10		
N/A	VCCAUX		E39		
N/A	VCCAUX		E4		
N/A	VCCAUX		D38		
N/A	VCCAUX		D22		
N/A	VCCAUX		D21		
N/A	VCCAUX		D5		
N/A	GND		AB38		
N/A	GND		AB35		
N/A	GND		AB32		
N/A	GND		AB26		
N/A	GND		AB25		
N/A	GND		AB24		
N/A	GND		AB23		
N/A	GND		AB22		
N/A	GND		AB21		
N/A	GND		AB20		
N/A	GND		AB19		

FF1696 Flip-Chip Fine-Pitch BGA Package

As shown in Table 14, XC2VP100 Virtex-II Pro devices are available in the FF1696 flip-chip fine-pitch BGA package. Following this table are the FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L01N_0/VRP_0	E33	
0	IO_L01P_0/VRN_0	F33	
0	IO_L02N_0	K32	
0	IO_L02P_0	L32	
0	IO_L03N_0	C32	
0	IO_L03P_0/VREF_0	C33	
0	IO_L05_0/No_Pair	G33	
0	IO_L06N_0	A33	
0	IO_L06P_0	B33	
0	IO_L07N_0	F32	
0	IO_L07P_0	G32	
0	IO_L08N_0	H32	
0	IO_L08P_0	J32	
0	IO_L09N_0	D32	
0	IO_L09P_0/VREF_0	E32	
0	IO_L19N_0	A32	
0	IO_L19P_0	B32	
0	IO_L20N_0	K31	
0	IO_L20P_0	L31	
0	IO_L21N_0	H30	
0	IO_L21P_0	G31	
0	IO_L25N_0	E31	
0	IO_L25P_0	F31	
0	IO_L26N_0	H31	
0	IO_L26P_0	J31	
0	IO_L27N_0	D30	
0	IO_L27P_0/VREF_0	D31	
0	IO_L28N_0	B31	
0	IO_L28P_0	C31	
0	IO_L29N_0	K30	
0	IO_L29P_0	L30	
0	IO_L30N_0	F30	
0	IO_L30P_0	G30	
0	IO_L34N_0	B30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L26P_4	AU12	
4	IO_L27N_4	AR12	
4	IO_L27P_4/VREF_4	AP12	
4	IO_L28N_4	AW13	
4	IO_L28P_4	AW12	
4	IO_L29N_4	BA12	
4	IO_L29P_4	AY12	
4	IO_L30N_4	AN13	
4	IO_L30P_4	AM13	
4	IO_L34N_4	AU13	
4	IO_L34P_4	AT13	
4	IO_L35N_4	BA13	
4	IO_L35P_4	AY13	
4	IO_L36N_4	AM14	
4	IO_L36P_4/VREF_4	AL14	
4	IO_L76N_4	AR15	
4	IO_L76P_4	AT14	
4	IO_L77N_4	AV14	
4	IO_L77P_4	AU14	
4	IO_L78N_4	AP14	
4	IO_L78P_4	AN14	
4	IO_L79N_4	AW15	
4	IO_L79P_4	AY14	
4	IO_L80_4/No_Pair	BB14	
4	IO_L83_4/No_Pair	BA14	
4	IO_L84N_4	AM15	
4	IO_L84P_4	AL15	
4	IO_L85N_4	AT16	
4	IO_L85P_4	AT15	
4	IO_L86N_4	AV15	
4	IO_L86P_4	AU15	
4	IO_L87N_4	AP15	
4	IO_L87P_4/VREF_4	AN15	
4	IO_L37N_4	AY16	
4	IO_L37P_4	AY15	
4	IO_L38N_4	BB15	
4	IO_L38P_4	BA15	