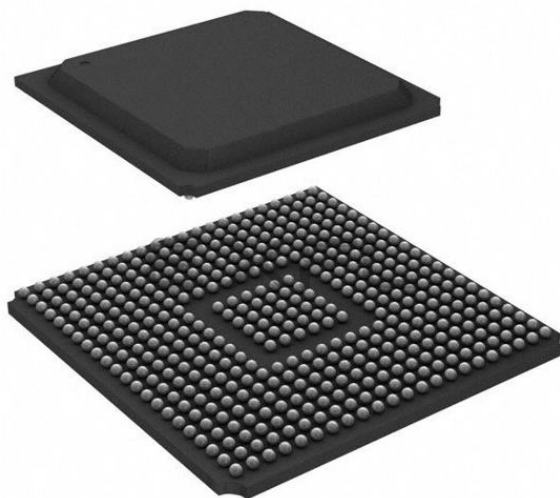




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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

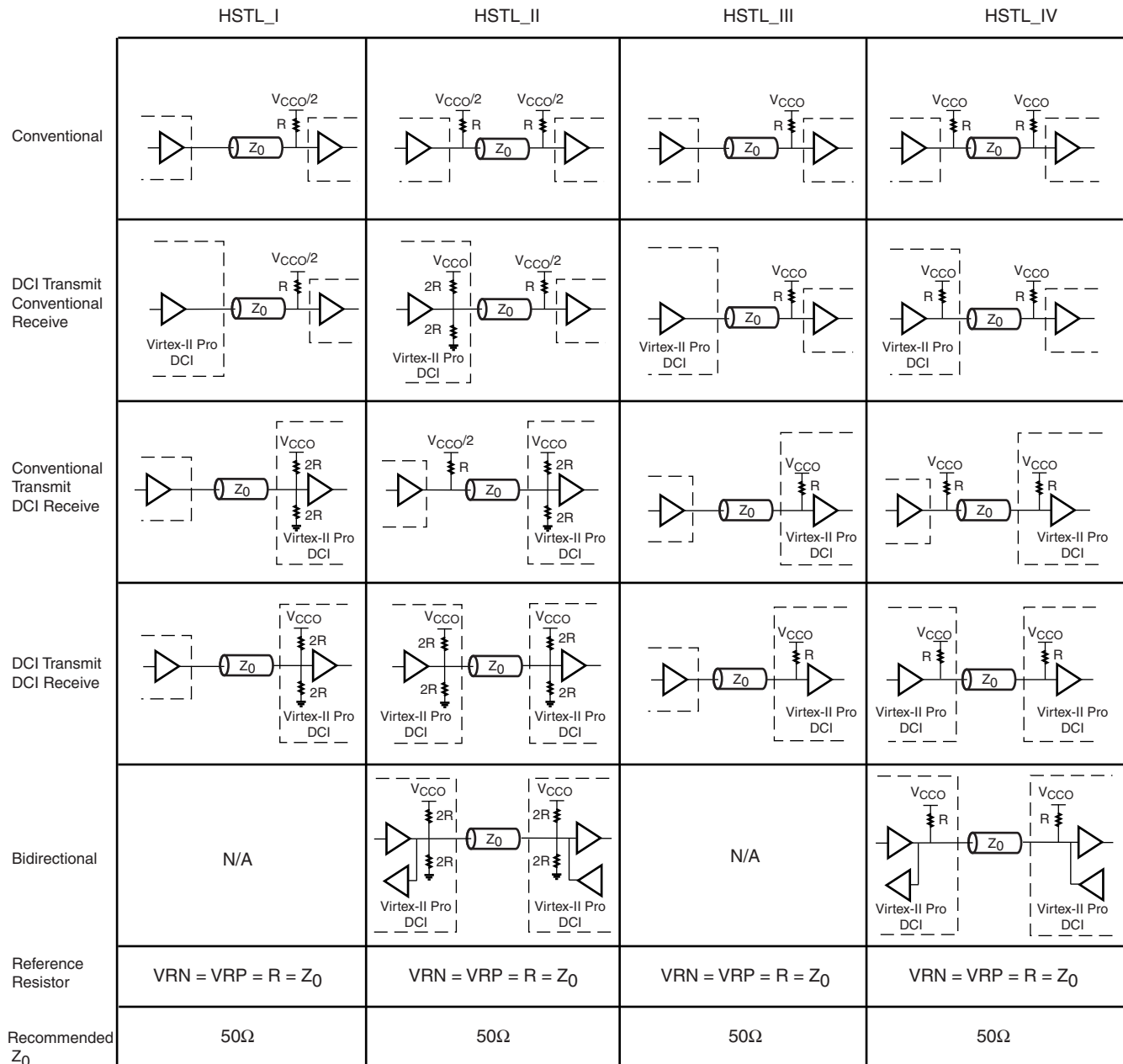
Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-6fg456c

Table 15: SelectIO-Ultra Differential Buffers With On-Chip Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).



DS083-2_65a_082102

Figure 28: HSTL DCI Usage Examples

Table 27: RocketIO Transmitter Switching Characteristics

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F _{GTX}	Flipchip packages	1.0		3.125 ⁽¹⁾	Gb/s
		Wirebond packages	1.0		2.5 ⁽¹⁾	Gb/s
Serial data rate, half-speed clock ⁽³⁾ (2X oversampling)		Flipchip packages	0.600		1.0	Gb/s
Wirebond packages		0.600		1.0	Gb/s	
Serial data output deterministic jitter	T _{DJ}	2.126 Gb/s – 3.125 Gb/s			0.17	UI ⁽²⁾
		1.0626 Gb/s – 2.125 Gb/s			0.08	UI
		1.0 Gb/s – 1.0625 Gb/s			0.05	UI
		600 Mb/s – 999 Mb/s			0.08 ⁽⁴⁾	UI
Serial data output random jitter	T _{RJ}	2.126 Gb/s – 3.125 Gb/s			0.18	UI
		1.0626 Gb/s – 2.125 Gb/s			0.19	UI
		1.0 Gb/s – 1.0625 Gb/s			0.18	UI
		600 Mb/s – 999 Mb/s			0.18 ⁽⁴⁾	UI
TX rise time	T _{RTX}	20% – 80%		120		ps
TX fall time	T _{FTX}			120		ps
Transmit latency ⁽⁵⁾	T _{TXLAT}	Including CRC		14	17	TXUSR CLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T _{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T _{TX2DC}		45	50	55	%

Notes:

1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in [XAPP572](#) are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in [XAPP572](#) are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to [RocketIO Transceiver User Guide](#) for more information on calculating latency.

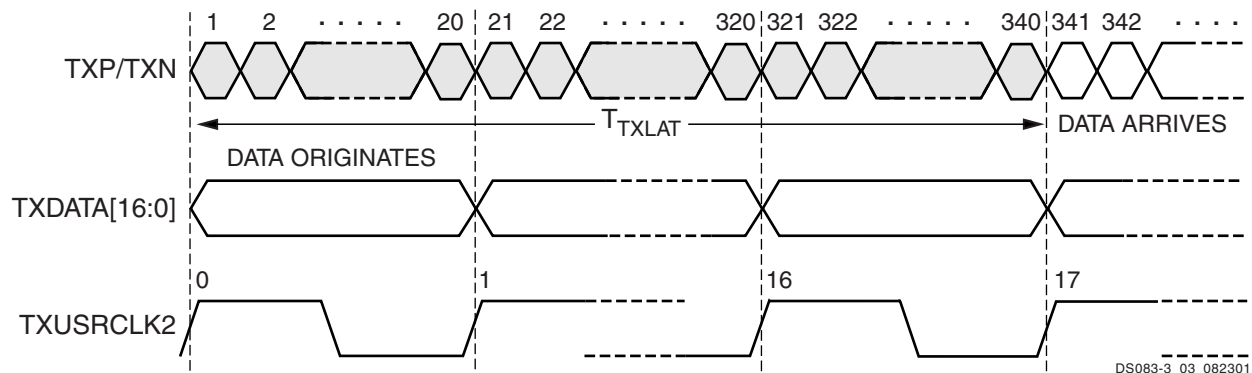


Figure 5: RocketIO Transmitter Latency (Maximum, Including CRC)

Table 36: IOB Input Switching Characteristics Standard Adjustments (Continued)

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSLVDCI, 1.8V	HSLVDCI_18	T _{IHSLVDCI_18}	0.59	0.68	0.75	ns
HSLVDCI, 2.5V	HSLVDCI_25	T _{IHSLVDCI_25}	0.59	0.68	0.75	ns
HSLVDCI, 3.3V	HSLVDCI_33	T _{IHSLVDCI_33}	0.59	0.68	0.75	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T _{IGTL_DCI}	0.49	0.57	0.62	ns
GTL Plus with DCI	GTLP_DCI	T _{IGTLP_DCI}	0.27	0.31	0.35	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	T _{IHSTL_I_DCI}	0.27	0.31	0.35	ns
HSTL, Class II, with DCI	HSTL_II_DCI	T _{IHSTL_II_DCI}	0.27	0.31	0.35	ns
HSTL, Class III, with DCI	HSTL_III_DCI	T _{IHSTL_III_DCI}	0.27	0.31	0.35	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	T _{IHSTL_IV_DCI}	0.27	0.31	0.35	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	T _{IHSTL_I_DCI_18}	0.27	0.31	0.35	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	T _{IHSTL_II_DCI_18}	0.27	0.31	0.35	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	T _{IHSTL_III_DCI_18}	0.27	0.31	0.35	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	T _{IHSTL_IV_DCI_18}	0.27	0.31	0.35	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	T _{ISSTL18_I_DCI}	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	T _{ISSTL18_II_DCI}	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	T _{ISSTL2_I_DCI}	0.17	0.20	0.22	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	T _{ISSTL2_II_DCI}	0.17	0.20	0.22	ns
LVDS, 2.5V, with DCI	LVDS_25_DCI	T _{ILVDS_25_DCI}	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DCI	LVDSEXT_25_DCI	T _{ILVDSEXT_25_DCI}	0.33	0.37	0.41	ns
LVDS, 2.5V, with Differential Termination (DT)	LVDS_25_DT	T _{ILVDS_25_DT}	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DT	LVDSEXT_25_DT	T _{ILVDSEXT_25_DT}	0.33	0.37	0.41	ns
ULVDS, 2.5V, with DT	ULVDS_25_DT	T _{IULVDS_25_DT}	0.31	0.36	0.40	ns
LDT, 2.5V, with DT	LDT_25_DT	T _{ILD_25_DT}	0.31	0.36	0.40	ns

Miscellaneous Timing Parameters

Table 61: Miscellaneous Timing Parameters

			Speed Grade			
Description	Symbol	Constraints F _{CLKIN}	-7	-6	-5	Units
Time Required to Achieve LOCK						
Using DLL outputs ⁽¹⁾	LOCK_DLL:					
	LOCK_DLL_60	> 60MHz	20.00	20.00	20.00	us
	LOCK_DLL_50_60	50 - 60 MHz	25.00	25.00	25.00	us
	LOCK_DLL_40_50	40 - 50 MHz	50.00	50.00	50.00	us
	LOCK_DLL_30_40	30 - 40 MHz	90.00	90.00	90.00	us
	LOCK_DLL_24_30	24 - 30 MHz	120.00	120.00	120.00	us
Using CLKFX outputs	LOCK_FX_MIN		10.00	10.00	10.00	ms
	LOCK_FX_MAX		10.00	10.00	10.00	ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT		50.00	50.00	50.00	us
Fine Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.00	10.00	10.00	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.00	30.00	30.00	ps
	DCM_TAP_MAX		50.00	50.00	50.00	ps

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Frequency Synthesis

Table 62: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross-Reference

Table 63: Parameter Cross-Reference

Libraries Guide	Data Sheet
DLL_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_{1X 2X DV}_LF
DFS_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_{1X DV}_HF
DFS_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_FX_HF

FG256/FGG256 Fine-Pitch BGA Package

As shown in [Table 5](#), XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the [FG256/FGG256 Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
4	IO_L54N_4	V15			
4	IO_L54P_4	W15			
4	IO_L55N_4	Y15			
4	IO_L55P_4	AA15			
4	IO_L57N_4	AB15			
4	IO_L57P_4/VREF_4	AA14			
4	IO_L67N_4	AC15			
4	IO_L67P_4	AD15			
4	IO_L69N_4	V14			
4	IO_L69P_4/VREF_4	W14			
4	IO_L74N_4/GCLK3S	AB14			
4	IO_L74P_4/GCLK2P	AC14			
4	IO_L75N_4/GCLK1S	AD14			
4	IO_L75P_4/GCLK0P	AE14			
5	IO_L75N_5/GCLK7S	AE13			
5	IO_L75P_5/GCLK6P	AD13			
5	IO_L74N_5/GCLK5S	AC13			
5	IO_L74P_5/GCLK4P	AB13			
5	IO_L69N_5/VREF_5	W13			
5	IO_L69P_5	V13			
5	IO_L67N_5	AD12			
5	IO_L67P_5	AC12			
5	IO_L57N_5/VREF_5	AA13			
5	IO_L57P_5	AB12			
5	IO_L55N_5	AA12			
5	IO_L55P_5	Y12			
5	IO_L54N_5	W12			
5	IO_L54P_5	V12			
5	IO_L53_5/No_Pair	AA11			
5	IO_L50_5/No_Pair	Y11			
5	IO_L49N_5	AD10			
5	IO_L49P_5	AC10			
5	IO_L48N_5	AB11			
5	IO_L48P_5	AB10			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VCCINT	U10			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U17			
N/A	VCCINT	U20			
N/A	VCCINT	V9			
N/A	VCCINT	V18			
N/A	VCCINT	Y10			
N/A	VCCINT	Y13			
N/A	VCCINT	Y14			
N/A	VCCINT	Y17			
N/A	VCCAUX	A2			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	A25			
N/A	VCCAUX	N1			
N/A	VCCAUX	N26			
N/A	VCCAUX	P1			
N/A	VCCAUX	P26			
N/A	VCCAUX	AF2			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	VCCAUX	AF25			
N/A	GND	A1			
N/A	GND	A26			
N/A	GND	B2			
N/A	GND	B25			
N/A	GND	C3			
N/A	GND	C24			
N/A	GND	D4			
N/A	GND	D8			
N/A	GND	D19			
N/A	GND	D23			
N/A	GND	F10			
N/A	GND	F17			

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 8](#), XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the [FF672 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	VCCO_1		K13			
1	VCCO_1		K12			
1	VCCO_1		K11			
1	VCCO_1		K10			
1	VCCO_1		J13			
1	VCCO_1		J12			
1	VCCO_1		J11			
1	VCCO_1		J10			
2	VCCO_2		R10			
2	VCCO_2		P10			
2	VCCO_2		N10			
2	VCCO_2		N9			
2	VCCO_2		M10			
2	VCCO_2		M9			
2	VCCO_2		L10			
2	VCCO_2		L9			
2	VCCO_2		K9			
2	VCCO_2		J9			
3	VCCO_3		AB9			
3	VCCO_3		AA9			
3	VCCO_3		Y10			
3	VCCO_3		Y9			
3	VCCO_3		W10			
3	VCCO_3		W9			
3	VCCO_3		V10			
3	VCCO_3		V9			
3	VCCO_3		U10			
3	VCCO_3		T10			
4	VCCO_4		AB13			
4	VCCO_4		AB12			
4	VCCO_4		AB11			
4	VCCO_4		AB10			
4	VCCO_4		AA15			
4	VCCO_4		AA14			
4	VCCO_4		AA13			
4	VCCO_4		AA12			

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L43P_1	B13		
1	IO_L39N_1	G13		
1	IO_L39P_1	F13		
1	IO_L38N_1	J15		
1	IO_L38P_1	J14		
1	IO_L37N_1	B12		
1	IO_L37P_1	A12		
1	IO_L27N_1/VREF_1	D13		
1	IO_L27P_1	D12		
1	IO_L26N_1	L13		
1	IO_L26P_1	K13		
1	IO_L25N_1	F12		
1	IO_L25P_1	E12		
1	IO_L21N_1	B11		
1	IO_L21P_1	A11		
1	IO_L20N_1	K12		
1	IO_L20P_1	J12		
1	IO_L19N_1	C12		
1	IO_L19P_1	C11		
1	IO_L09N_1/VREF_1	F11		
1	IO_L09P_1	E11		
1	IO_L08N_1	H13		
1	IO_L08P_1	H12		
1	IO_L07N_1	G12		
1	IO_L07P_1	G11		
1	IO_L06N_1	B10		
1	IO_L06P_1	A10		
1	IO_L05_1/No_Pair	G10		
1	IO_L03N_1/VREF_1	D10		
1	IO_L03P_1	C10		
1	IO_L02N_1	K11		
1	IO_L02P_1	J11		
1	IO_L01N_1/VRP_1	F10		
1	IO_L01P_1/VRN_1	E10		
2	IO_L01N_2/VRP_2	B8		
2	IO_L01P_2/VRN_2	B9		
2	IO_L02N_2	C9		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L36N_3	AE4		
3	IO_L36P_3	AF4		
3	IO_L35N_3	AC10		
3	IO_L35P_3	AD10		
3	IO_L34N_3	AE1		
3	IO_L34P_3	AE2		
3	IO_L33N_3/VREF_3	AF6		
3	IO_L33P_3	AF7		
3	IO_L32N_3	AC8		
3	IO_L32P_3	AC9		
3	IO_L31N_3	AF2		
3	IO_L31P_3	AF3		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AG6		
3	IO_L29N_3	AD9		
3	IO_L29P_3	AE9		
3	IO_L28N_3	AG4		
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AG2		
3	IO_L27P_3	AG3		
3	IO_L26N_3	AD7		
3	IO_L26P_3	AE7		
3	IO_L25N_3	AH6		
3	IO_L25P_3	AH7		
3	IO_L24N_3	AH5		
3	IO_L24P_3	AJ5		
3	IO_L23N_3	AE8		
3	IO_L23P_3	AF8		
3	IO_L22N_3	AH1		
3	IO_L22P_3	AH2		
3	IO_L21N_3/VREF_3	AJ6		
3	IO_L21P_3	AK6		
3	IO_L20N_3	AG7		
3	IO_L20P_3	AG8		
3	IO_L19N_3	AJ3		
3	IO_L19P_3	AJ4		
3	IO_L18N_3	AJ1		
3	IO_L18P_3	AJ2		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L47P_3	AC10		
3	IO_L46N_3	AE7		
3	IO_L46P_3	AE8		
3	IO_L45N_3/VREF_3	AE5		
3	IO_L45P_3	AE6		
3	IO_L44N_3	AB13		
3	IO_L44P_3	AC13		
3	IO_L43N_3	AE3		
3	IO_L43P_3	AE4		
3	IO_L42N_3	AE1		
3	IO_L42P_3	AE2		
3	IO_L41N_3	AD10		
3	IO_L41P_3	AD11		
3	IO_L40N_3	AF6		
3	IO_L40P_3	AF7		
3	IO_L39N_3/VREF_3	AF4		
3	IO_L39P_3	AF5		
3	IO_L38N_3	AC12		
3	IO_L38P_3	AD12		
3	IO_L37N_3	AF1		
3	IO_L37P_3	AF2		
3	IO_L36N_3	AG6		
3	IO_L36P_3	AG7		
3	IO_L35N_3	AE9		
3	IO_L35P_3	AE10		
3	IO_L34N_3	AF3		
3	IO_L34P_3	AG3		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AE11		
3	IO_L32P_3	AE12		
3	IO_L31N_3	AH6		
3	IO_L31P_3	AH7		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AH4		
3	IO_L29N_3	AD13		
3	IO_L29P_3	AE13		
3	IO_L28N_3	AH2		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L76N_6		AU42		
6	IO_L77P_6		AT39		
6	IO_L77N_6		AT40		
6	IO_L78P_6		AT41		
6	IO_L78N_6		AT42		
6	IO_L79P_6		AR38		
6	IO_L79N_6		AR39		
6	IO_L80P_6		AR37		
6	IO_L80N_6		AT38		
6	IO_L81P_6		AR40		
6	IO_L81N_6/VREF_6		AR41		
6	IO_L82P_6		AP36		
6	IO_L82N_6		AP37		
6	IO_L83P_6		AP35		
6	IO_L83N_6		AR36		
6	IO_L84P_6		AP38		
6	IO_L84N_6		AP39		
6	IO_L07P_6		AP41		
6	IO_L07N_6		AP42		
6	IO_L08P_6		AN35		
6	IO_L08N_6		AN36		
6	IO_L09P_6		AN37		
6	IO_L09N_6/VREF_6		AN38		
6	IO_L10P_6		AN41		
6	IO_L10N_6		AN42		
6	IO_L11P_6		AM33		
6	IO_L11N_6		AN34		
6	IO_L12P_6		AM36		
6	IO_L12N_6		AM37		
6	IO_L13P_6		AM38		
6	IO_L13N_6		AM39		
6	IO_L14P_6		AM34		
6	IO_L14N_6		AM35		
6	IO_L15P_6		AN40		
6	IO_L15N_6/VREF_6		AM40		
6	IO_L16P_6		AM41		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AB18		
N/A	GND		AB17		
N/A	GND		AB11		
N/A	GND		AB8		
N/A	GND		AB5		
N/A	GND		AC41		
N/A	GND		AC26		
N/A	GND		AC25		
N/A	GND		AC24		
N/A	GND		AC23		
N/A	GND		AC22		
N/A	GND		AC21		
N/A	GND		AC20		
N/A	GND		AC19		
N/A	GND		AC18		
N/A	GND		AC17		
N/A	GND		AC2		
N/A	GND		AD26		
N/A	GND		AD25		
N/A	GND		AD24		
N/A	GND		AD23		
N/A	GND		AD22		
N/A	GND		AD21		
N/A	GND		AD20		
N/A	GND		AD19		
N/A	GND		AD18		
N/A	GND		AD17		
N/A	GND		AE37		
N/A	GND		AE34		
N/A	GND		AE26		
N/A	GND		AE25		
N/A	GND		AE24		
N/A	GND		AE23		
N/A	GND		AE22		
N/A	GND		AE21		
N/A	GND		AE20		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L57P_1	E19	
1	IO_L56N_1	K18	
1	IO_L56P_1	J18	
1	IO_L55N_1	H19	
1	IO_L55P_1	H20	
1	IO_L54N_1	B18	
1	IO_L54P_1	A18	
1	IO_L53_1/No_Pair	L18	
1	IO_L50_1/No_Pair	L19	
1	IO_L49N_1	C18	
1	IO_L49P_1	C19	
1	IO_L48N_1	F18	
1	IO_L48P_1	E18	
1	IO_L47N_1	L17	
1	IO_L47P_1	K17	
1	IO_L46N_1	G18	
1	IO_L46P_1	G19	
1	IO_L18N_1/VREF_1	C17	NC
1	IO_L18P_1	B17	NC
1	IO_L12N_1	G17	NC
1	IO_L12P_1	F17	NC
1	IO_L11N_1	M17	NC
1	IO_L11P_1	M18	NC
1	IO_L10N_1	B16	NC
1	IO_L10P_1	A16	NC
1	IO_L45N_1/VREF_1	D16	
1	IO_L45P_1	D17	
1	IO_L44N_1	K16	
1	IO_L44P_1	J16	
1	IO_L43N_1	F16	
1	IO_L43P_1	E16	
1	IO_L39N_1	H16	
1	IO_L39P_1	H17	
1	IO_L38N_1	M16	
1	IO_L38P_1	L16	
1	IO_L37N_1	B15	
1	IO_L37P_1	A15	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L75N_2	C5	
2	IO_L75P_2	B5	
2	IO_L76N_2/VREF_2	D7	
2	IO_L76P_2	C6	
2	IO_L77N_2	H8	
2	IO_L77P_2	H9	
2	IO_L78N_2	C3	
2	IO_L78P_2	C4	
2	IO_L79N_2	D1	
2	IO_L79P_2	D2	
2	IO_L80N_2	J8	
2	IO_L80P_2	K9	
2	IO_L81N_2	E6	
2	IO_L81P_2	D5	
2	IO_L82N_2/VREF_2	E4	
2	IO_L82P_2	D4	
2	IO_L83N_2	L8	
2	IO_L83P_2	L9	
2	IO_L84N_2	E3	
2	IO_L84P_2	D3	
2	IO_L61N_2	F8	
2	IO_L61P_2	E8	
2	IO_L62N_2	M8	
2	IO_L62P_2	M9	
2	IO_L63N_2	F7	
2	IO_L63P_2	E7	
2	IO_L64N_2/VREF_2	F3	
2	IO_L64P_2	E2	
2	IO_L65N_2	N12	
2	IO_L65P_2	P12	
2	IO_L66N_2	F1	
2	IO_L66P_2	F2	
2	IO_L67N_2	G7	
2	IO_L67P_2	G8	
2	IO_L68N_2	N10	
2	IO_L68P_2	N11	
2	IO_L69N_2	G6	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L38P_3	AE9	
3	IO_L37N_3	AH3	
3	IO_L37P_3	AJ3	
3	IO_L36N_3	AJ1	
3	IO_L36P_3	AJ2	
3	IO_L35N_3	AE6	
3	IO_L35P_3	AE7	
3	IO_L34N_3	AK6	
3	IO_L34P_3	AK7	
3	IO_L33N_3/VREF_3	AK3	
3	IO_L33P_3	AK4	
3	IO_L32N_3	AE12	
3	IO_L32P_3	AF12	
3	IO_L31N_3	AL5	
3	IO_L31P_3	AL6	
3	IO_L30N_3	AL3	
3	IO_L30P_3	AL4	
3	IO_L29N_3	AF10	
3	IO_L29P_3	AF11	
3	IO_L28N_3	AK2	
3	IO_L28P_3	AL2	
3	IO_L27N_3/VREF_3	AL7	
3	IO_L27P_3	AM6	
3	IO_L26N_3	AF7	
3	IO_L26P_3	AF8	
3	IO_L25N_3	AM4	
3	IO_L25P_3	AM5	
3	IO_L24N_3	AM1	
3	IO_L24P_3	AM2	
3	IO_L23N_3	AG10	
3	IO_L23P_3	AG11	
3	IO_L22N_3	AM7	
3	IO_L22P_3	AN7	
3	IO_L21N_3/VREF_3	AN5	
3	IO_L21P_3	AN6	
3	IO_L20N_3	AG8	
3	IO_L20P_3	AG9	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	M2	AM33	
N/A	TCK	K10	
N/A	TDI	M32	
N/A	TDO	M11	
N/A	TMS	L10	
N/A	PWRDWN_B	AP10	
N/A	HSWAP_EN	K33	
N/A	RSVD	J10	
N/A	VBATT	M12	
N/A	DXP	M31	
N/A	DXN	L33	
N/A	VCCINT	AK30	
N/A	VCCINT	N30	
N/A	VCCINT	AJ29	
N/A	VCCINT	P29	
N/A	VCCINT	AJ28	
N/A	VCCINT	AH28	
N/A	VCCINT	R28	
N/A	VCCINT	P28	
N/A	VCCINT	AJ27	
N/A	VCCINT	AH27	
N/A	VCCINT	AG27	
N/A	VCCINT	AF27	
N/A	VCCINT	AE27	
N/A	VCCINT	AD27	
N/A	VCCINT	AC27	
N/A	VCCINT	AB27	
N/A	VCCINT	AA27	
N/A	VCCINT	Y27	
N/A	VCCINT	W27	
N/A	VCCINT	V27	
N/A	VCCINT	U27	
N/A	VCCINT	T27	
N/A	VCCINT	R27	
N/A	VCCINT	P27	
N/A	VCCINT	AH26	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	W16	
N/A	VCCINT	V16	
N/A	VCCINT	U16	
N/A	VCCINT	T16	
N/A	VCCINT	R16	
N/A	VCCINT	P16	
N/A	VCCINT	AJ15	
N/A	VCCINT	AH15	
N/A	VCCINT	R15	
N/A	VCCINT	P15	
N/A	VCCINT	AJ14	
N/A	VCCINT	P14	
N/A	VCCINT	AK13	
N/A	VCCINT	N13	
N/A	VCCAUX	BA42	
N/A	VCCAUX	AY42	
N/A	VCCAUX	AL42	
N/A	VCCAUX	AB42	
N/A	VCCAUX	AA42	
N/A	VCCAUX	M42	
N/A	VCCAUX	C42	
N/A	VCCAUX	B42	
N/A	VCCAUX	BB41	
N/A	VCCAUX	A41	
N/A	VCCAUX	BB40	
N/A	VCCAUX	A40	
N/A	VCCAUX	BB31	
N/A	VCCAUX	A31	
N/A	VCCAUX	BB22	
N/A	VCCAUX	A22	
N/A	VCCAUX	BB21	
N/A	VCCAUX	A21	
N/A	VCCAUX	BB12	
N/A	VCCAUX	A12	
N/A	VCCAUX	BB3	
N/A	VCCAUX	A3	
N/A	VCCAUX	BB2	