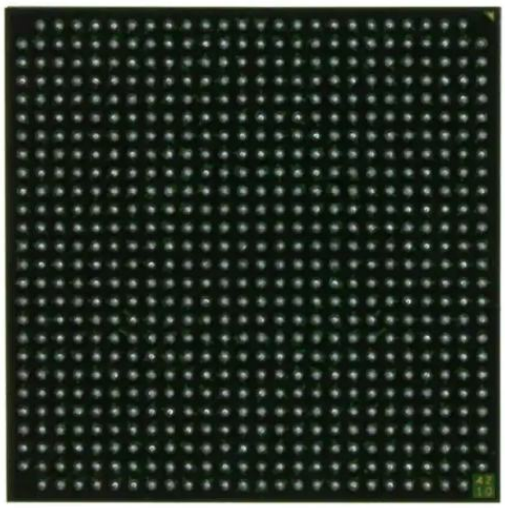

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-7ff672c

  - HyperTransport (LDT) I/O with current driver buffers
  - Built-in DDR input and output registers
- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13 µm Nine-Layer Copper Process with 90 nm High-Speed Transistors
- 1.5V (V_{CCINT}) core power supply, dedicated 2.5V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Standard 1.00 mm Pitch.
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- Each Device 100% Factory Tested

General Description

The Virtex-II Pro and Virtex-II Pro X families contain platform FPGAs for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU blocks in Virtex-II Pro Series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13 µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gate arrays.

Architecture

Array Overview

Virtex-II Pro and Virtex-II Pro X devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high-density and high-performance system designs. Virtex-II Pro devices implement the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel (RocketIO) or 6.25 Gb/s (RocketIO X).
- Embedded IBM PowerPC 405 RISC processor blocks provide performance up to 400 MHz.
- SelectIO-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM+ memory modules provide large 18 Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and supports high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Features

This section briefly describes Virtex-II Pro / Virtex-II Pro X features. For more details, refer to Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description.

RocketIO / RocketIO X MGT Cores

The RocketIO and RocketIO X Multi-Gigabit Transceivers are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 100 Gb/s (RocketIO) or 170 Gb/s (RocketIO X) of full-duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s (RocketIO) or 6.25 Gb/s (RocketIO X).

implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test Boundary-Scan instructions. In test mode, Boundary-Scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II Pro / Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Enviornment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See **DS080**, *System ACE CompactFlash Solution* for more information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II Pro / Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops and latches, distributed SelectRAM+, and block SelectRAM+ memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro / Virtex-II Pro X by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to **www.xilinx.com/ipcenter** for the latest and most complete list of cores.

Hardware Cores

- Bus Infrastructure cores (arbiters, bridges, and more)
- Memory cores (DDR, Flash, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

RXP and RXN as shown in Figure 5. This supports multiple termination styles, including high-side, low-side, and differential (floating or active). This configuration supports receiver termination compatible to Virtex-II Pro devices, using a CML (high-side) termination to an active supply of 1.8V – 2.5V. For DC coupling of two Virtex-II Pro X devices, a 1.5V CML termination for VTRX is recommended.

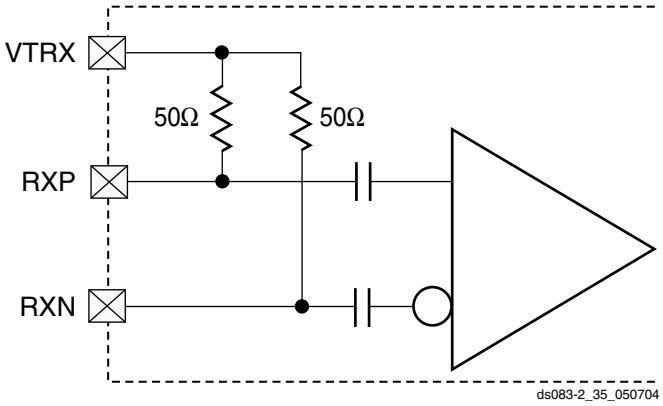

Figure 5: **RocketIO X Receive Termination**

PCS

Fabric Data Interface

Internally, the PCS operates in either 2-byte mode (16/20 bits) or 4-byte mode (32/40 bits). When in 2-byte mode, the FPGA fabric interface can either be 1, 2, or 4 bytes wide. When in 4-byte mode, the FPGA fabric interface can either be 4 or 8 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 2 summarizes the USRCLK2-to-USRCLK ratios for the different possible combinations of data widths.

Table 2: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2	
	2-Byte Internal Data Width	4-Byte Internal Data Width
1 byte	1:2 (1)	N/A
2 byte	1:1	N/A
4 byte	2:1 (1)	1:1
8 byte	N/A	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

As a general guide, use 2-byte internal data width mode when the serial speed is below 5 Gb/s, and 4-byte internal data width mode when the serial speed is greater than 5 Gb/s. In 2-byte mode, the PCS processes 4-byte data every other byte.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

64B/66B Encoder/Decoder

The RocketIO X PCS features a 64B/66B encoder/decoder, scrambler/descrambler, and gearbox functions that can be bypassed as needed. The encoder is compliant with IEEE 802.3ae specifications.

Scrambler/Gearbox

The bypassable scrambler operates on the read side of the transmit FIFO. The scrambler uses the following generator polynomial to scramble 64B/66B payload data:

$$G(x) = 1 + x^{39} + x^{58}$$

The scrambler works in conjunction with the gearbox, which frames 64B/66B data for the PMA. The gearbox should always be enabled when using the 64B/66B protocal.

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

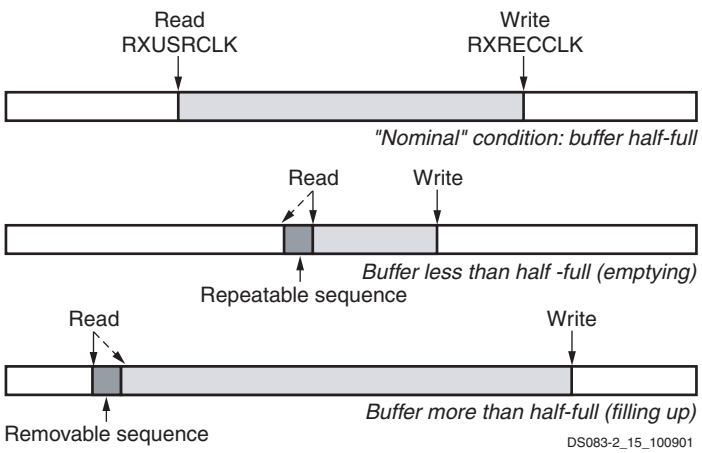

Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

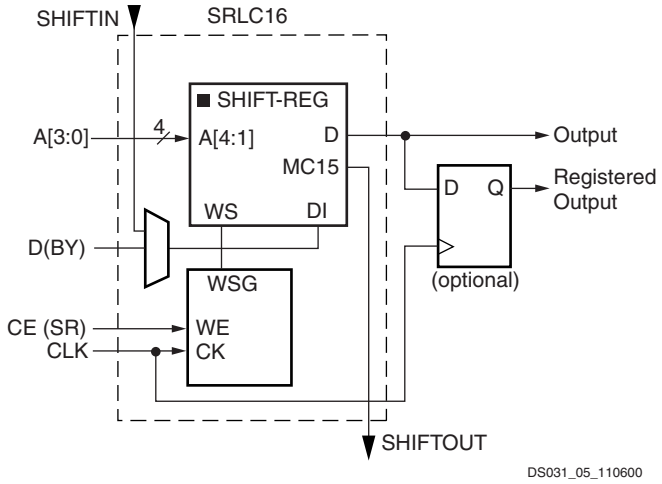

Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

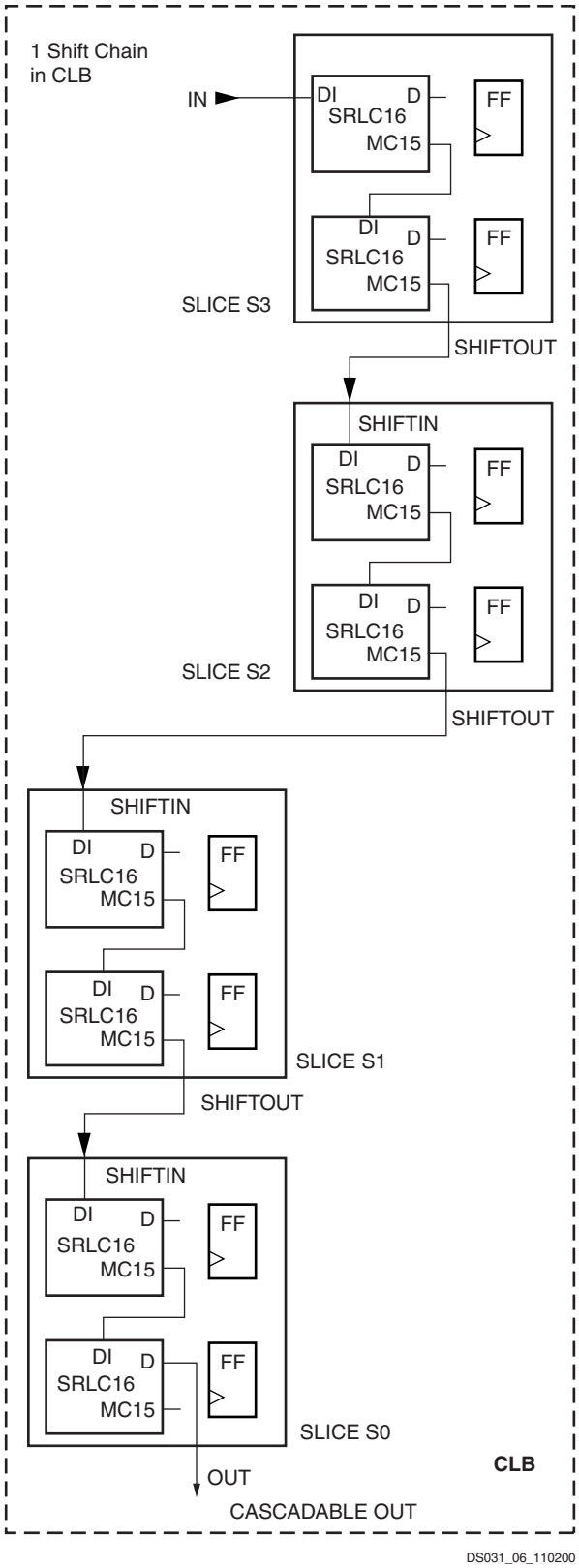

Figure 40: **Cascadable Shift Register**

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
VTRXPAD#	Input	Receive termination supply for the RocketIO multi-gigabit transceiver (1.8V - 2.8V).
VTTXPAD#	Input	Transmit termination supply for the RocketIO multi-gigabit transceiver (1.8V - 2.8V).
GNDA#	Input	Ground for the analog circuitry of the RocketIO multi-gigabit transceiver.
RXPPAD#	Input	Positive differential receive port of the RocketIO multi-gigabit transceiver.
RXNPAD#	Input	Negative differential receive port of the RocketIO multi-gigabit transceiver.
TXPPAD#	Output	Positive differential transmit port of the RocketIO multi-gigabit transceiver.
TXNPAD#	Output	Negative differential transmit port of the RocketIO multi-gigabit transceiver.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).
2. Virtex-II Pro X devices XC2VPX20 and XC2VPX70 only. Each BREFCLK(N/P) differential clock input pair takes the place of one regular Virtex-II Pro dual-function IO/GCLKx(S/P) pair on each side of the chip (top or bottom). For RocketIO BREFCLK, see section BREFCLK Pin Definitions (RocketIO Only) immediately following.

BREFCLK Pin Definitions (RocketIO Only)

These dedicated clocks use the same clock inputs for all packages:

Top	BREFCLK	P	GCLK4S	Bottom	BREFCLK	P	GCLK6P
		N	GCLK5P			N	GCLK7S
	BREFCLK2	P	GCLK2S		BREFCLK2	P	GCLK0P
		N	GCLK3P			N	GCLK1S

For detailed information about using BREFCLK/BREFCLK2, including routing considerations and pin numbers for all package types, refer to Chapter 2, "Digital Design Considerations," in the **RocketIO Transceiver User Guide**.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	R15			
N/A	GND	R16			
N/A	GND	R24			
N/A	GND	T11			
N/A	GND	T12			
N/A	GND	T13			
N/A	GND	T14			
N/A	GND	T15			
N/A	GND	T16			
N/A	GND	U6			
N/A	GND	U21			
N/A	GND	W4			
N/A	GND	W23			
N/A	GND	AA10			
N/A	GND	AA17			
N/A	GND	AC4			
N/A	GND	AC8			
N/A	GND	AC19			
N/A	GND	AC23			
N/A	GND	AD3			
N/A	GND	AD24			
N/A	GND	AE2			
N/A	GND	AE25			
N/A	GND	AF1			
N/A	GND	AF26			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L59N_2		P8			
2	IO_L59P_2		P7			
2	IO_L60N_2		N4			
2	IO_L60P_2		N3			
2	IO_L85N_2		P3			
2	IO_L85P_2		P2			
2	IO_L86N_2		R8			
2	IO_L86P_2		R7			
2	IO_L87N_2		P5			
2	IO_L87P_2		P4			
2	IO_L88N_2/VREF_2		R2			
2	IO_L88P_2		T2			
2	IO_L89N_2		R6			
2	IO_L89P_2		R5			
2	IO_L90N_2		R4			
2	IO_L90P_2		R3			
3	IO_L90N_3		U1			
3	IO_L90P_3		V1			
3	IO_L89N_3		T5			
3	IO_L89P_3		T6			
3	IO_L88N_3		T3			
3	IO_L88P_3		T4			
3	IO_L87N_3/VREF_3		U2			
3	IO_L87P_3		U3			
3	IO_L86N_3		T7			
3	IO_L86P_3		T8			
3	IO_L85N_3		U4			
3	IO_L85P_3		U5			
3	IO_L60N_3		V2			
3	IO_L60P_3		W2			
3	IO_L59N_3		T9			
3	IO_L59P_3		U9			
3	IO_L58N_3		V3			
3	IO_L58P_3		V4			
3	IO_L57N_3/VREF_3		W1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	M0		AD24			
N/A	M1		AC24			
N/A	M2		AC23			
N/A	TCK		G7			
N/A	TDI		F26			
N/A	TDO		F5			
N/A	TMS		H8			
N/A	PWRDWN_B		AD7			
N/A	HSWAP_EN		H23			
N/A	RSVD		D6			
N/A	VBATT		H7			
N/A	DXP		H24			
N/A	DXN		D25			
N/A	AVCCAUXTX4		B26			
N/A	VTTXPAD4		B27			
N/A	TXNPAD4		A27			
N/A	TXPPAD4		A26			
N/A	GNDA4		C25			
N/A	RXPPAD4		A25			
N/A	RXNPAD4		A24			
N/A	VTRXPAD4		B25			
N/A	AVCCAUXRX4		B24			
N/A	AVCCAUXTX6		B19			
N/A	VTTXPAD6		B20			
N/A	TXNPAD6		A20			
N/A	TXPPAD6		A19			
N/A	GNDA6		C19			
N/A	RXPPAD6		A18			
N/A	RXNPAD6		A17			
N/A	VTRXPAD6		B18			
N/A	AVCCAUXRX6		B17			
N/A	AVCCAUXTX7		B13			
N/A	VTTXPAD7		B14			
N/A	TXNPAD7		A14			
N/A	TXPPAD7		A13			
N/A	GNDA7		C12			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	RXPPAD7		A12			
N/A	RXNPAD7		A11			
N/A	VTRXPAD7		B12			
N/A	AVCCAUXRX7		B11			
N/A	AVCCAUXTX9		B6			
N/A	VTTXPAD9		B7			
N/A	TXNPAD9		A7			
N/A	TXPPAD9		A6			
N/A	GNDA9		C6			
N/A	RXPPAD9		A5			
N/A	RXNPAD9		A4			
N/A	VTRXPAD9		B5			
N/A	AVCCAUXRX9		B4			
N/A	AVCCAUXRX16		AJ4			
N/A	VTRXPAD16		AJ5			
N/A	RXNPAD16		AK4			
N/A	RXPPAD16		AK5			
N/A	GNDA16		AH6			
N/A	TXPPAD16		AK6			
N/A	TXNPAD16		AK7			
N/A	VTTXPAD16		AJ7			
N/A	AVCCAUXTX16		AJ6			
N/A	AVCCAUXRX18		AJ11			
N/A	VTRXPAD18		AJ12			
N/A	RXNPAD18		AK11			
N/A	RXPPAD18		AK12			
N/A	GNDA18		AH12			
N/A	TXPPAD18		AK13			
N/A	TXNPAD18		AK14			
N/A	VTTXPAD18		AJ14			
N/A	AVCCAUXTX18		AJ13			
N/A	AVCCAUXRX19		AJ17			
N/A	VTRXPAD19		AJ18			
N/A	RXNPAD19		AK17			
N/A	RXPPAD19		AK18			
N/A	GNDA19		AH19			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L74N_1/GCLK1P	D17				
1	IO_L74P_1/GCLK0S	E17				
1	IO_L73N_1	F17				
1	IO_L73P_1	G17				
1	IO_L69N_1/VREF_1	K17				
1	IO_L69P_1	L17				
1	IO_L68N_1	D16				
1	IO_L68P_1	E16				
1	IO_L67N_1	F16				
1	IO_L67P_1	G16				
1	IO_L57N_1/VREF_1	H16				
1	IO_L57P_1	J16				
1	IO_L56N_1	D15				
1	IO_L56P_1	D14				
1	IO_L55N_1	F15				
1	IO_L55P_1	G15				
1	IO_L54N_1	K16				
1	IO_L54P_1	L16				
1	IO_L53_1/No_Pair	C13				
1	IO_L50_1/No_Pair	C14				
1	IO_L49N_1	E14				
1	IO_L49P_1	F14				
1	IO_L48N_1	J15				
1	IO_L48P_1	K15				
1	IO_L47N_1	C11				
1	IO_L47P_1	D11				
1	IO_L46N_1	D12				
1	IO_L46P_1	D13				
1	IO_L45N_1/VREF_1	G14				
1	IO_L45P_1	H14				
1	IO_L44N_1	D10				
1	IO_L44P_1	E10				
1	IO_L43N_1	E13				
1	IO_L43P_1	F13				
1	IO_L39N_1	J14				
1	IO_L39P_1	K14				
1	IO_L38N_1	C9				
1	IO_L38P_1	D9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L39P_3	AD4				
3	IO_L38N_3	AB9				
3	IO_L38P_3	AB10				
3	IO_L37N_3	AD5				
3	IO_L37P_3	AD6				
3	IO_L36N_3	AE2				
3	IO_L36P_3	AF2				
3	IO_L35N_3	AD7				
3	IO_L35P_3	AD8				
3	IO_L34N_3	AE4				
3	IO_L34P_3	AE5				
3	IO_L33N_3/VREF_3	AG1				
3	IO_L33P_3	AG2				
3	IO_L32N_3	AC9				
3	IO_L32P_3	AC10				
3	IO_L31N_3	AF3				
3	IO_L31P_3	AF4				
3	IO_L24N_3	AH1	NC			
3	IO_L24P_3	AH2	NC			
3	IO_L23N_3	AE7	NC			
3	IO_L23P_3	AE8	NC			
3	IO_L22N_3	AF5	NC			
3	IO_L22P_3	AF6	NC			
3	IO_L21N_3/VREF_3	AG3	NC			
3	IO_L21P_3	AG4	NC			
3	IO_L20N_3	AD9	NC			
3	IO_L20P_3	AD10	NC			
3	IO_L19N_3	AH3	NC			
3	IO_L19P_3	AH4	NC			
3	IO_L18N_3	AJ1	NC			
3	IO_L18P_3	AJ2	NC			
3	IO_L17N_3	AF7	NC			
3	IO_L17P_3	AF8	NC			
3	IO_L16N_3	AK1	NC			
3	IO_L16P_3	AK2	NC			
3	IO_L15N_3/VREF_3	AG5	NC			
3	IO_L15P_3	AG6	NC			
3	IO_L06N_3	AL1				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
4	IO_L47N_4	AE15		
4	IO_L47P_4	AD15		
4	IO_L48N_4	AM14		
4	IO_L48P_4	AL14		
4	IO_L49N_4	AP14		
4	IO_L49P_4	AN14		
4	IO_L50_4/No_Pair	AH15		
4	IO_L53_4/No_Pair	AG16		
4	IO_L54N_4	AK15		
4	IO_L54P_4	AJ15		
4	IO_L55N_4	AM15		
4	IO_L55P_4	AL16		
4	IO_L56N_4	AE16		
4	IO_L56P_4	AD16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AN15		
4	IO_L66N_4	AJ16	NC	
4	IO_L66P_4/VREF_4	AH16	NC	
4	IO_L67N_4	AN16		
4	IO_L67P_4	AM16		
4	IO_L68N_4	AG17		
4	IO_L68P_4	AF17		
4	IO_L69N_4	AJ17		
4	IO_L69P_4/VREF_4	AH17		
4	IO_L73N_4	AL17		
4	IO_L73P_4	AK17		
4	IO_L74N_4/GCLK3S	AE17		
4	IO_L74P_4/GCLK2P	AD17		
4	IO_L75N_4/GCLK1S	AN17		
4	IO_L75P_4/GCLK0P	AM17		
5	IO_L75N_5/GCLK7S	AM18		
5	IO_L75P_5/GCLK6P	AN18		
5	IO_L74N_5/GCLK5S	AD18		
5	IO_L74P_5/GCLK4P	AE18		
5	IO_L73N_5	AK18		
5	IO_L73P_5	AL18		
5	IO_L69N_5/VREF_5	AH18		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
4	VCCO_4	AD12		
4	VCCO_4	AL11		
4	VCCO_4	AG11		
3	VCCO_3	AB12		
3	VCCO_3	AA12		
3	VCCO_3	Y12		
3	VCCO_3	W12		
3	VCCO_3	V12		
3	VCCO_3	AC11		
3	VCCO_3	AF9		
3	VCCO_3	AM8		
3	VCCO_3	AH8		
3	VCCO_3	AD8		
3	VCCO_3	Y8		
3	VCCO_3	AM4		
3	VCCO_3	AH4		
3	VCCO_3	AD4		
3	VCCO_3	Y4		
3	VCCO_3	AK2		
2	VCCO_2	U12		
2	VCCO_2	T12		
2	VCCO_2	R12		
2	VCCO_2	P12		
2	VCCO_2	N12		
2	VCCO_2	M11		
2	VCCO_2	J9		
2	VCCO_2	R8		
2	VCCO_2	L8		
2	VCCO_2	G8		
2	VCCO_2	C8		
2	VCCO_2	R4		
2	VCCO_2	L4		
2	VCCO_2	G4		
2	VCCO_2	C4		
2	VCCO_2	E2		
1	VCCO_1	M17		
1	VCCO_1	M16		
1	VCCO_1	M15		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L59P_0	N21		
0	IO_L60N_0	E23		
0	IO_L60P_0	F22		
0	IO_L64N_0	D22		
0	IO_L64P_0	E22		
0	IO_L65N_0	H21		
0	IO_L65P_0	H20		
0	IO_L66N_0	G22		
0	IO_L66P_0/VREF_0	G21		
0	IO_L67N_0	D21		
0	IO_L67P_0	E21		
0	IO_L68N_0	J21		
0	IO_L68P_0	K21		
0	IO_L69N_0	C22		
0	IO_L69P_0/VREF_0	C21		
0	IO_L73N_0	F21		
0	IO_L73P_0	F20		
0	IO_L74N_0/GCLK7P	L21		
0	IO_L74P_0/GCLK6S	M21		
0	IO_L75N_0/GCLK5P	D20		
0	IO_L75P_0/GCLK4S	E20		
1	IO_L75N_1/GCLK3P	K20		
1	IO_L75P_1/GCLK2S	J20		
1	IO_L74N_1/GCLK1P	N20		
1	IO_L74P_1/GCLK0S	M20		
1	IO_L73N_1	E19		
1	IO_L73P_1	D19		
1	IO_L69N_1/VREF_1	G19		
1	IO_L69P_1	F19		
1	IO_L68N_1	L19		
1	IO_L68P_1	K19		
1	IO_L67N_1	J19		
1	IO_L67P_1	H19		
1	IO_L66N_1/VREF_1	C19		
1	IO_L66P_1	C18		
1	IO_L65N_1	N19		
1	IO_L65P_1	M19		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L47P_3	AC10		
3	IO_L46N_3	AE7		
3	IO_L46P_3	AE8		
3	IO_L45N_3/VREF_3	AE5		
3	IO_L45P_3	AE6		
3	IO_L44N_3	AB13		
3	IO_L44P_3	AC13		
3	IO_L43N_3	AE3		
3	IO_L43P_3	AE4		
3	IO_L42N_3	AE1		
3	IO_L42P_3	AE2		
3	IO_L41N_3	AD10		
3	IO_L41P_3	AD11		
3	IO_L40N_3	AF6		
3	IO_L40P_3	AF7		
3	IO_L39N_3/VREF_3	AF4		
3	IO_L39P_3	AF5		
3	IO_L38N_3	AC12		
3	IO_L38P_3	AD12		
3	IO_L37N_3	AF1		
3	IO_L37P_3	AF2		
3	IO_L36N_3	AG6		
3	IO_L36P_3	AG7		
3	IO_L35N_3	AE9		
3	IO_L35P_3	AE10		
3	IO_L34N_3	AF3		
3	IO_L34P_3	AG3		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AE11		
3	IO_L32P_3	AE12		
3	IO_L31N_3	AH6		
3	IO_L31P_3	AH7		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AH4		
3	IO_L29N_3	AD13		
3	IO_L29P_3	AE13		
3	IO_L28N_3	AH2		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		