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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-7ff896c

RocketIO and RocketIO X Feature Comparison

Table 7 summarizes the major differences between the RocketIO and RocketIO X MGTs. The [RocketIO X Transceiver User Guide](#) has more details, including a design migration guide in the Appendix.

Table 7: RocketIO PMA versus RocketIO X PMA

	RocketIO X Transceiver	RocketIO Transceiver
PCS Features:		
FPGA interface	1, 2, 4, and 8 byte width	1, 2, and 4 byte width
Coding support	8B/10B and 64B/66B bypassable	8B/10B bypassable
Gearbox/scrambler support	Yes	N/A
CRC Support	No	Yes
Half rate	No	Yes
PMA Features:		
Baud rate	2.488 Gb/s - 6.25 Gb/s ⁽²⁾	622 Mb/s - 3.125 Gb/s
Reference clock frequency tolerance	350 PPM	100 PPM
Reference clock multiplier	x16, x20, x32, x40	x20
Max run length	75	75
Receive equalization	Built-in analog linear, programmable	None
Output swing (differential p-p)	200 mV to 1600 mV, programmable	800 mV to 1600 mV, programmable
Pre-emphasis	0% to 500%, programmable	4 selectable levels from 10% to 33%
Slew rate control	2 selectable levels	None
Termination	On-chip internal, 50Ω	On-chip internal, 50Ω/75Ω selectable
AC coupling capacitor	On-chip internal. Can be AC- or DC-coupled externally	None
Transmit supply voltage (AVCCAUXTX)	2.5V	2.5V
Receive supply voltage (AVCCAUXRX)	1.5V, 1.8V ⁽¹⁾	2.5V
PMA configuration support	Direct, dynamic, and partial configuration	Partial configuration
Others:		
JTAG support	Input only	None
Process technology	0.13 μm	0.25 μm
Available packages	Flip-chip only	Flip-chip and wire-bond

Notes:

- AVCCAUXRX for RocketIO X MGT is 1.5V (nominal) for 8B/10B-encoded data. For all other encoding protocols, AVCCAUXRX is 1.8V (nominal).
- The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.

Table 9: Supported Differential Signal I/O Standards

I/O Standard	Output V _{CCO}	Input V _{CCO}	Input V _{REF}	Output V _{OD}
LDT_25	2.5	N/R	N/R	0.500 – 0.740
LVDS_25	2.5	N/R	N/R	0.247 – 0.454
LVDS_EXT_25	2.5	N/R	N/R	0.440 – 0.820
BLVDS_25	2.5	N/R	N/R	0.250 – 0.450
ULVDS_25	2.5	N/R	N/R	0.500 – 0.740
LVPECL_25	2.5	N/R	N/R	0.345 – 1.185
LDT_25_DT ⁽¹⁾	2.5	2.5	N/R	0.500 – 0.740
LVDS_25_DT ⁽¹⁾	2.5	2.5	N/R	0.247 – 0.454
LVDS_EXT_25_DT ⁽¹⁾	2.5	2.5	N/R	0.330 – 0.700
ULVDS_25_DT ⁽¹⁾	2.5	2.5	N/R	0.500 – 0.740

Notes:

1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

Table 10: Supported DCI I/O Standards

I/O Standard	Output V _{CCO}	Input V _{CCO}	Input V _{REF}	Termination Type
LVDCI_33 ⁽¹⁾	3.3	3.3	N/R	Series
LVDCI_25	2.5	2.5	N/R	Series
LVDCI_DV2_25	2.5	2.5	N/R	Series
LVDCI_18	1.8	1.8	N/R	Series
LVDCI_DV2_18	1.8	1.8	N/R	Series
LVDCI_15	1.5	1.5	N/R	Series
LVDCI_DV2_15	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL2_I_DCI ⁽²⁾	2.5	2.5	1.25	Split
SSTL2_II_DCI ⁽²⁾	2.5	2.5	1.25	Split
SSTL18_I_DCI ⁽³⁾	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split

Table 10: Supported DCI I/O Standards (Continued)

I/O Standard	Output V _{CCO}	Input V _{CCO}	Input V _{REF}	Termination Type
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDS_EXT_25_DCI	2.5	2.5	N/R	Split

Notes:

1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

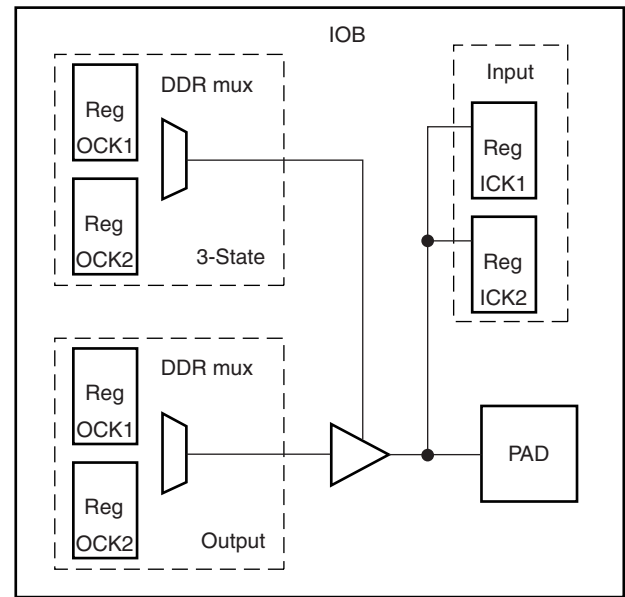


Figure 19: Virtex-II Pro IOB Block

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

Table 17: Processor Block Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	T _{PCCK_DCR} /T _{PCKC_DCR}	0.38/−0.18	0.44/−0.20	0.48/−0.23	ns, min
Device Control Register Bus data inputs	T _{PDCK_DCR} /T _{PCKD_DCR}	0.65/−0.01	0.75/−0.01	0.82/−0.02	ns, min
Clock and Power Management control inputs	T _{PCCK_CPM} /T _{PCKC_CPM}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	T _{PCCK_RST} /T _{PCKC_RST}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	T _{PCCK_DBG} /T _{PCKC_DBG}	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	T _{PCCK_TRC} /T _{PCKC_TRC}	1.37/−0.41	1.57/−0.48	1.73/−0.52	ns, min
External Interrupt Controller control inputs	T _{PCCK_EIC} /T _{PCKC_EIC}	0.57/−0.22	0.66/−0.25	0.72/−0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	T _{PCKCO_DCR}	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	T _{PCKAO_DCR}	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	T _{PCKDO_DCR}	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	T _{PCKCO_CPM}	1.26	1.45	1.59	ns, max
Reset control outputs	T _{PCKCO_RST}	1.32	1.51	1.66	ns, max
Debug control outputs	T _{PCKCO_DBG}	1.94	2.22	2.44	ns, max
Trace control outputs	T _{PCKCO_TRC}	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T _{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T _{CPWL}	1.25	1.42	1.66	ns, min

Table 18: Processor Block PLB Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	T _{PCCK} _PLB/T _{PCKC} _PLB	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	T _{PDCK} _PLB/T _{PCKD} _PLB	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	T _{PCKCO} _PLB	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	T _{PCKAO} _PLB	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	T _{PCKDO} _PLB	1.44	1.65	1.81	ns, max

Date	Version	Revision
12/03/02	2.5	Updated parametric information in: Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from $-0.5V$ to $-0.3V$ for 3.3V. Table 2: Add footnote (2) regarding V_{CCAUX} voltage droop. Renumbered other notes. Table 12: Add waveform diagrams (Figure 1 and Figure 2) illustrating DV_{OUT} (single-ended) and DV_{PPOUT} (differential). Table 23: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct T_{RCLK} and T_{FCLK} values and unit of measurement. Table 60: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL.
01/20/03	2.6	Updated parametric information in: Table 12: Correct DV_{IN} Min (200 mV to 175 mV) and DV_{IN} Max (1000 mV to 2000 mV). Table 23: Correct T_{RCLK}/T_{FCLK} Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max T_{GJT} parameter. Table 59: Correct hyperlink in footnote (1) to point directly to Answer Record 13645. - Move clock parameters from Table 18, Table 19, Table 20, and Table 21 to Table 16.
03/24/03	2.7	- Added/updated timing parameters from speedsfile v1.76. Table 2: Delete first table footnote and renumber all others. Table 3: Add "sample-tested" to I_L. Remove "Device" column, unnecessary. Table 8: Update V_{OCM} (Typ) to 1.250V. Table 10: Update LVPECL_25 DC parameters. Table 23: Update F_{GCLK} frequency ranges. Break out T_{GJT} by operating speed. Table 27: Update F_{GTx} frequency ranges. Correct T_{DJ} to 0.17 UI, T_{RJ} to 0.18 UI. Table 39: Update V_{REF} (Typ) for HSTL Class I/II from 1.08V to 0.90V. Table 43, Table 44: Correct parameter name "CE input (WS)" to "SR input". Table 64: Break out T_{DCD_CLK0} by device type.
05/27/03	2.8	- Updated time and frequency parameters as per speedsfile v1.78. Table 3: Added values for I_{REF}, I_L, I_{RPU}, I_{RPD} - Corrected I_{CCINTQ} (Table 4) and $I_{CCINTMIN}$ (Table 5) for XC2VP20 to 600 mA. Table 4: Updated/Added Typ and Max quiescent current values for XC2VP7 and XC2VP20. Added footnote specifying parameters are for Commercial Grade parts. Table 5: Added footnote specifying parameters are for Commercial Grade parts. Table 6: Corrected V_{IH} (Max) for LVTTL and LVCMOS33 standards from 3.6V to 3.45V. Changed V_{IL} (Min) for all standards to $-0.2V$. Corrected V_{IL} (Max) for LVCMOS15 and LVCMOS18 from 20% V_{CC0} to 30% V_{CC0}. Table 10: Corrected LVPECL_25 Min and Max values for V_{IH} and V_{IL}. Added explanatory text above table. Table 13 and Table 14 (pin-pin and reg-reg performance): Changed device specified from XC2VP7FF672-6 to XC2VP20FF1152-6. Table 15: Updated to show devices XC2VP7 and XC2VP20 as Preliminary for the -6 speed grade and Production for the -5 speed grade. - Removed former Table 32, Standard Capacitive Loads. Table 52: Updated T_{TAPCK} from 4.0 ns to 5.5 ns. Table 59: Modified footnote referenced at CLKFX/CLKFX180 to point to the online Jitter Calculator. - Added Figure 6 and accompanying procedure for measuring standard adjustments.
05/27/03 (cont'd)	2.8 (cont'd)	Table 1: Footnote (2) rewritten to specify "one or more banks." Table 57: Some DCM parameters were erroneously missing from v2.8 (single-module version) due to a document compilation error. The concatenated full data sheet version was not affected. These parameters have been restored.

Table 4: Virtex-II Pro Pin Definitions (Continued)

Pin Name	Direction	Description
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. These pins can be used to clock the RocketIO transceiver. See the RocketIO Transceiver User Guide for design guidelines and BREFCLK-specific pins, by device.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
V _{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins: ⁽¹⁾		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection. Pin is biased by V _{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used. The mode pins are not to be toggled (changed) while in operation during and after configuration.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock. This pin is 3.3V compatible.
TDI	Input	Boundary Scan Data Input. This pin is 3.3V compatible.
TDO	Output (open-drain)	Boundary Scan Data Output. Pin is open-drain and can be pulled up to 3.3V. It is recommended that the external pull-up be greater than 200Ω. There is no internal pull-up.
TMS	Input	Boundary Scan Mode Select. This pin is 3.3V compatible.
PWRDWN_B	Input (unsupported)	Active Low power-down pin (unsupported). <i>Driving this pin Low can adversely affect device operation and configuration.</i> PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins:		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V _{BATT}	Input	Decryptor key memory backup supply. (Connect to V _{CCAUX} or GND if battery not used.)
RSVD	N/A	Reserved pin - do not connect.
V _{CCO}	Input	Power-supply pins for the output drivers (per bank).
V _{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V _{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the RocketIO MGT (2.5V).
AVCCAUTX#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (2.5V).
BREFCLKN, BREFCLKP ⁽²⁾	Input	Differential clock input that clocks the RocketIO X MGTs populating the same side of the chip (top or bottom). Can also drive DCMs for RocketIO X MGT use.

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	RSVD	C23			
N/A	VBATT	A24			
N/A	TMS	B24			
N/A	TCK	B26			
N/A	TDO	D24			
N/A	CCLK	AE24			
N/A	PWRDWN_B	AF24			
N/A	DONE	AD23			
N/A	AVCCAUXRX16	AE23			
N/A	VTRXPAD16	AE22			
N/A	RXNPAD16	AF23			
N/A	RXPPAD16	AF22			
N/A	GNDA16	AD21			
N/A	TXPPAD16	AF21			
N/A	TXNPAD16	AF20			
N/A	VTTXPAD16	AE20			
N/A	AVCCAUTX16	AE21			
N/A	AVCCAUXRX18	AE18			
N/A	VTRXPAD18	AE17			
N/A	RXNPAD18	AF18			
N/A	RXPPAD18	AF17			
N/A	GNDA18	AD16			
N/A	TXPPAD18	AF16			
N/A	TXNPAD18	AF15			
N/A	VTTXPAD18	AE15			
N/A	AVCCAUTX18	AE16			
N/A	AVCCAUXRX19	AE12			
N/A	VTRXPAD19	AE11			
N/A	RXNPAD19	AF12			
N/A	RXPPAD19	AF11			
N/A	GNDA19	AD11			
N/A	TXPPAD19	AF10			
N/A	TXNPAD19	AF9			
N/A	VTTXPAD19	AE9			
N/A	AVCCAUTX19	AE10			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L57P_3		Y1			
3	IO_L56N_3		U7			
3	IO_L56P_3		U8			
3	IO_L55N_3		V5			
3	IO_L55P_3		V6			
3	IO_L54N_3		Y2			
3	IO_L54P_3		AA2			
3	IO_L53N_3		V7			
3	IO_L53P_3		V8			
3	IO_L52N_3		W3			
3	IO_L52P_3		W4			
3	IO_L51N_3/VREF_3		AA1			
3	IO_L51P_3		AB1			
3	IO_L50N_3		W5			
3	IO_L50P_3		W6			
3	IO_L49N_3		Y4			
3	IO_L49P_3		Y5			
3	IO_L48N_3		AA3			
3	IO_L48P_3		AA4			
3	IO_L47N_3		W7			
3	IO_L47P_3		W8			
3	IO_L46N_3		AB3			
3	IO_L46P_3		AB4			
3	IO_L45N_3/VREF_3		AB2			
3	IO_L45P_3		AC2			
3	IO_L44N_3		AA5			
3	IO_L44P_3		AA6			
3	IO_L43N_3		AC3			
3	IO_L43P_3		AC4			
3	IO_L42N_3		AD1	NC		
3	IO_L42P_3		AD2	NC		
3	IO_L41N_3		Y7	NC		
3	IO_L41P_3		Y8	NC		
3	IO_L40N_3		AB5	NC		
3	IO_L40P_3		AB6	NC		
3	IO_L39N_3/VREF_3		AE1	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	IO_L05_4/No_Pair		AD8			
4	IO_L06N_4/VRP_4		AG8			
4	IO_L06P_4/VRN_4		AH8			
4	IO_L07N_4		AC10			
4	IO_L07P_4/VREF_4		AD10			
4	IO_L08N_4		AE7			
4	IO_L08P_4		AE8			
4	IO_L09N_4		AJ8			
4	IO_L09P_4/VREF_4		AK8			
4	IO_L37N_4		AC11			
4	IO_L37P_4		AD11			
4	IO_L38N_4		AF8			
4	IO_L38P_4		AF9			
4	IO_L39N_4		AF10			
4	IO_L39P_4		AG10			
4	IO_L43N_4		AC12			
4	IO_L43P_4		AD12			
4	IO_L44N_4		AE9			
4	IO_L44P_4		AE10			
4	IO_L45N_4		AH9			
4	IO_L45P_4/VREF_4		AJ9			
4	IO_L46N_4		AC13	NC		
4	IO_L46P_4		AD13	NC		
4	IO_L47N_4		AE11	NC		
4	IO_L47P_4		AE12	NC		
4	IO_L48N_4		AH10	NC		
4	IO_L48P_4		AH11	NC		
4	IO_L49N_4		AB14	NC		
4	IO_L49P_4		AC14	NC		
4	IO_L50_4/No_Pair		AF11	NC		
4	IO_L53_4/No_Pair		AG11	NC		
4	IO_L54N_4		AJ10	NC		
4	IO_L54P_4		AK10	NC		
4	IO_L56N_4		AF12	NC		
4	IO_L56P_4		AF13	NC		
4	IO_L57N_4		AG13	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	RXPPAD7		A12			
N/A	RXNPAD7		A11			
N/A	VTRXPAD7		B12			
N/A	AVCCAUXRX7		B11			
N/A	AVCCAUXTX9		B6			
N/A	VTTXPAD9		B7			
N/A	TXNPAD9		A7			
N/A	TXPPAD9		A6			
N/A	GND A9		C6			
N/A	RXPPAD9		A5			
N/A	RXNPAD9		A4			
N/A	VTRXPAD9		B5			
N/A	AVCCAUXRX9		B4			
N/A	AVCCAUXRX16		AJ4			
N/A	VTRXPAD16		AJ5			
N/A	RXNPAD16		AK4			
N/A	RXPPAD16		AK5			
N/A	GND A16		AH6			
N/A	TXPPAD16		AK6			
N/A	TXNPAD16		AK7			
N/A	VTTXPAD16		AJ7			
N/A	AVCCAUXTX16		AJ6			
N/A	AVCCAUXRX18		AJ11			
N/A	VTRXPAD18		AJ12			
N/A	RXNPAD18		AK11			
N/A	RXPPAD18		AK12			
N/A	GND A18		AH12			
N/A	TXPPAD18		AK13			
N/A	TXNPAD18		AK14			
N/A	VTTXPAD18		AJ14			
N/A	AVCCAUXTX18		AJ13			
N/A	AVCCAUXRX19		AJ17			
N/A	VTRXPAD19		AJ18			
N/A	RXNPAD19		AK17			
N/A	RXPPAD19		AK18			
N/A	GND A19		AH19			

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 11](#), XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the [FF1148 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L69P_5	AJ18		
5	IO_L68N_5	AF18		
5	IO_L68P_5	AG18		
5	IO_L67N_5	AM19		
5	IO_L67P_5	AN19		
5	IO_L66N_5/VREF_5	AH19	NC	
5	IO_L66P_5	AJ19	NC	
5	IO_L57N_5/VREF_5	AN20		
5	IO_L57P_5	AP20		
5	IO_L56N_5	AD19		
5	IO_L56P_5	AE19		
5	IO_L55N_5	AL19		
5	IO_L55P_5	AM20		
5	IO_L54N_5	AJ20		
5	IO_L54P_5	AK20		
5	IO_L53_5/No_Pair	AG19		
5	IO_L50_5/No_Pair	AH20		
5	IO_L49N_5	AN21		
5	IO_L49P_5	AP21		
5	IO_L48N_5	AL21		
5	IO_L48P_5	AM21		
5	IO_L47N_5	AD20		
5	IO_L47P_5	AE20		
5	IO_L46N_5	AJ21		
5	IO_L46P_5	AK21		
5	IO_L45N_5/VREF_5	AG21		
5	IO_L45P_5	AH21		
5	IO_L44N_5	AD21		
5	IO_L44P_5	AE21		
5	IO_L43N_5	AM22		
5	IO_L43P_5	AN22		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AJ22		
5	IO_L38N_5	AF20		
5	IO_L38P_5	AF21		
5	IO_L37N_5	AN23		
5	IO_L37P_5	AP23		
5	IO_L27N_5/VREF_5	AL22		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M12		
N/A	VCCINT	AD11		
N/A	VCCINT	L11		
N/A	VCCAUX	AN34		
N/A	VCCAUX	AG34		
N/A	VCCAUX	U34		
N/A	VCCAUX	H34		
N/A	VCCAUX	B34		
N/A	VCCAUX	AP33		
N/A	VCCAUX	A33		
N/A	VCCAUX	AP27		
N/A	VCCAUX	A27		
N/A	VCCAUX	AP17		
N/A	VCCAUX	A17		
N/A	VCCAUX	AP8		
N/A	VCCAUX	A8		
N/A	VCCAUX	AP2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AN1		
N/A	VCCAUX	AG1		
N/A	VCCAUX	U1		
N/A	VCCAUX	H1		
N/A	VCCAUX	B1		
N/A	GND	AK34		
N/A	GND	AF34		
N/A	GND	AB34		
N/A	GND	W34		
N/A	GND	V34		
N/A	GND	T34		
N/A	GND	N34		
N/A	GND	J34		
N/A	GND	E34		
N/A	GND	AN33		
N/A	GND	B33		
N/A	GND	AM32		
N/A	GND	C32		
N/A	GND	AP30		
N/A	GND	AK30		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L03N_4/D2	AN10		
4	IO_L03P_4/D3	AM10		
4	IO_L05_4/No_Pair	AK10		
4	IO_L06N_4/VRP_4	AR10		
4	IO_L06P_4/VRN_4	AP10		
4	IO_L07N_4	AU10		
4	IO_L07P_4/VREF_4	AT10		
4	IO_L08N_4	AJ12		
4	IO_L08P_4	AJ13		
4	IO_L09N_4	AL10		
4	IO_L09P_4/VREF_4	AL11		
4	IO_L19N_4	AN11		
4	IO_L19P_4	AM11		
4	IO_L20N_4	AH13		
4	IO_L20P_4	AH14		
4	IO_L21N_4	AR11		
4	IO_L21P_4	AP11		
4	IO_L25N_4	AU11		
4	IO_L25P_4	AT11		
4	IO_L26N_4	AL14		
4	IO_L26P_4	AK14		
4	IO_L27N_4	AM12		
4	IO_L27P_4/VREF_4	AL12		
4	IO_L28N_4	AT12	NC	
4	IO_L28P_4	AR12	NC	
4	IO_L29N_4	AJ14	NC	
4	IO_L29P_4	AJ15	NC	
4	IO_L30N_4	AM13	NC	
4	IO_L30P_4	AL13	NC	
4	IO_L34N_4	AP12	NC	
4	IO_L34P_4	AN13	NC	
4	IO_L35N_4	AL15	NC	
4	IO_L35P_4	AK15	NC	
4	IO_L36N_4	AT13	NC	
4	IO_L36P_4/VREF_4	AR13	NC	
4	IO_L37N_4	AN14		
4	IO_L37P_4	AM14		
4	IO_L38N_4	AH15		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L82N_7/VREF_7	G37	NC	
7	IO_L81P_7	G33	NC	
7	IO_L81N_7	G34	NC	
7	IO_L79P_7	F38	NC	
7	IO_L79N_7	F39	NC	
7	IO_L78P_7	F36	NC	
7	IO_L78N_7	F37	NC	
7	IO_L76P_7	G35	NC	
7	IO_L76N_7/VREF_7	F35	NC	
7	IO_L75P_7	E37	NC	
7	IO_L75N_7	E38	NC	
7	IO_L73P_7	D38	NC	
7	IO_L73N_7	D39	NC	
7	IO_L06P_7	F33		
7	IO_L06N_7	E33		
7	IO_L05P_7	J31		
7	IO_L05N_7	H32		
7	IO_L04P_7	E34		
7	IO_L04N_7/VREF_7	D34		
7	IO_L03P_7	D35		
7	IO_L03N_7	C35		
7	IO_L02P_7	H31		
7	IO_L02N_7	G31		
7	IO_L01P_7/VRN_7	D33		
7	IO_L01N_7/VRP_7	C33		
7	VCCO_7	E39		
7	VCCO_7	U37		
7	VCCO_7	N36		
7	VCCO_7	J36		
7	VCCO_7	E36		
7	VCCO_7	Y35		
7	VCCO_7	U33		
7	VCCO_7	N32		
7	VCCO_7	J32		
7	VCCO_7	F32		
7	VCCO_7	U29		
7	VCCO_7	N28		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AE19		
N/A	GND		AE18		
N/A	GND		AE17		
N/A	GND		AE9		
N/A	GND		AE6		
N/A	GND		AF25		
N/A	GND		AF24		
N/A	GND		AF23		
N/A	GND		AF22		
N/A	GND		AF21		
N/A	GND		AF20		
N/A	GND		AF19		
N/A	GND		AF18		
N/A	GND		AG42		
N/A	GND		AG1		
N/A	GND		AH39		
N/A	GND		AH36		
N/A	GND		AH7		
N/A	GND		AH4		
N/A	GND		AL42		
N/A	GND		AL1		
N/A	GND		AM22		
N/A	GND		AM21		
N/A	GND		AN39		
N/A	GND		AN4		
N/A	GND		AP34		
N/A	GND		AP9		
N/A	GND		AR42		
N/A	GND		AR35		
N/A	GND		AR22		
N/A	GND		AR21		
N/A	GND		AR8		
N/A	GND		AR1		
N/A	GND		AT36		
N/A	GND		AT7		
N/A	GND		AU37		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AU25		
N/A	GND		AU18		
N/A	GND		AU6		
N/A	GND		AV38		
N/A	GND		AV22		
N/A	GND		AV21		
N/A	GND		AV5		
N/A	GND		AW39		
N/A	GND		AW32		
N/A	GND		AW28		
N/A	GND		AW15		
N/A	GND		AW11		
N/A	GND		AW4		
N/A	GND		AY42		
N/A	GND		AY41		
N/A	GND		AY40		
N/A	GND		AY3		
N/A	GND		AY2		
N/A	GND		AY1		
N/A	GND		BA42		
N/A	GND		BA1		
N/A	GND		AA38		
N/A	GND		AA35		
N/A	GND		AA32		
N/A	GND		AA26		
N/A	GND		AA25		
N/A	GND		AA24		
N/A	GND		AA23		
N/A	GND		AA22		
N/A	GND		AA21		
N/A	GND		AA20		
N/A	GND		AA19		
N/A	GND		AA18		
N/A	GND		AA17		
N/A	GND		AA11		
N/A	GND		AA8		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L75N_2	C5	
2	IO_L75P_2	B5	
2	IO_L76N_2/VREF_2	D7	
2	IO_L76P_2	C6	
2	IO_L77N_2	H8	
2	IO_L77P_2	H9	
2	IO_L78N_2	C3	
2	IO_L78P_2	C4	
2	IO_L79N_2	D1	
2	IO_L79P_2	D2	
2	IO_L80N_2	J8	
2	IO_L80P_2	K9	
2	IO_L81N_2	E6	
2	IO_L81P_2	D5	
2	IO_L82N_2/VREF_2	E4	
2	IO_L82P_2	D4	
2	IO_L83N_2	L8	
2	IO_L83P_2	L9	
2	IO_L84N_2	E3	
2	IO_L84P_2	D3	
2	IO_L61N_2	F8	
2	IO_L61P_2	E8	
2	IO_L62N_2	M8	
2	IO_L62P_2	M9	
2	IO_L63N_2	F7	
2	IO_L63P_2	E7	
2	IO_L64N_2/VREF_2	F3	
2	IO_L64P_2	E2	
2	IO_L65N_2	N12	
2	IO_L65P_2	P12	
2	IO_L66N_2	F1	
2	IO_L66P_2	F2	
2	IO_L67N_2	G7	
2	IO_L67P_2	G8	
2	IO_L68N_2	N10	
2	IO_L68P_2	N11	
2	IO_L69N_2	G6	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	VCCO_7	AA29	
7	VCCO_7	Y29	
7	VCCO_7	W29	
7	VCCO_7	V29	
7	VCCO_7	U29	
7	VCCO_7	T29	
7	VCCO_7	R29	
7	VCCO_7	AA28	
7	VCCO_7	Y28	
7	VCCO_7	W28	
7	VCCO_7	V28	
7	VCCO_7	U28	
7	VCCO_7	T28	
6	VCCO_6	AU39	
6	VCCO_6	AN39	
6	VCCO_6	AJ39	
6	VCCO_6	AD39	
6	VCCO_6	AW37	
6	VCCO_6	AN35	
6	VCCO_6	AJ35	
6	VCCO_6	AD35	
6	VCCO_6	AR33	
6	VCCO_6	AL33	
6	VCCO_6	AH29	
6	VCCO_6	AG29	
6	VCCO_6	AF29	
6	VCCO_6	AE29	
6	VCCO_6	AD29	
6	VCCO_6	AC29	
6	VCCO_6	AB29	
6	VCCO_6	AG28	
6	VCCO_6	AF28	
6	VCCO_6	AE28	
6	VCCO_6	AD28	
6	VCCO_6	AC28	
6	VCCO_6	AB28	
5	VCCO_5	AW33	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	VCCO_2	F4	
1	VCCO_1	R21	
1	VCCO_1	P21	
1	VCCO_1	R20	
1	VCCO_1	P20	
1	VCCO_1	R19	
1	VCCO_1	P19	
1	VCCO_1	R18	
1	VCCO_1	P18	
1	VCCO_1	H18	
1	VCCO_1	D18	
1	VCCO_1	P17	
1	VCCO_1	H14	
1	VCCO_1	D14	
1	VCCO_1	M13	
1	VCCO_1	D10	
0	VCCO_0	D33	
0	VCCO_0	M30	
0	VCCO_0	H29	
0	VCCO_0	D29	
0	VCCO_0	P26	
0	VCCO_0	R25	
0	VCCO_0	P25	
0	VCCO_0	H25	
0	VCCO_0	D25	
0	VCCO_0	R24	
0	VCCO_0	P24	
0	VCCO_0	R23	
0	VCCO_0	P23	
0	VCCO_0	R22	
0	VCCO_0	P22	
N/A	CCLK	AM10	
N/A	PROG_B	J33	
N/A	DONE	AN10	
N/A	M0	AP33	
N/A	M1	AN33	