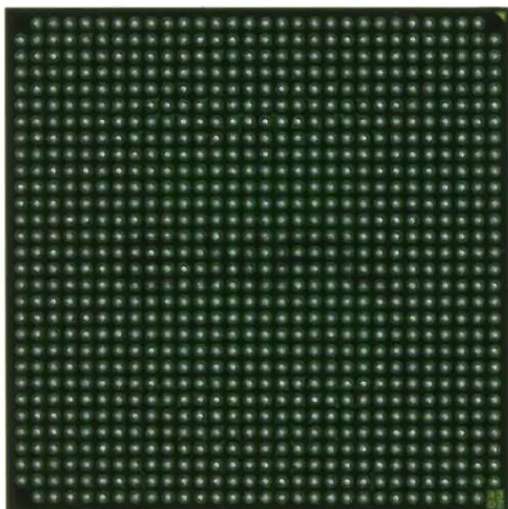




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	11088
Total RAM Bits	811008
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp7-7ffg896c

Each RocketIO or RocketIO X core implements the following technology:

- Serializer and deserializer (SERDES)
- Monolithic clock synthesis and clock recovery (CDR)
- 10 Gigabit Attachment Unit Interface (XAUI) Fibre Channel (3.1875 Gb/s XAUI), Infiniband, PCI Express, Aurora, SXI-5 (SFI-5, SPI-5), and OC-48 compatibility⁽¹⁾
- 8/16/32-bit (RocketIO) or 8/16/32/64-bit (RocketIO X) selectable FPGA interface
- 8B/10B (RocketIO) or 8B/10B and 64B/66B (RocketIO X) encoder and decoder with bypassing option on each channel
- Channel bonding support (two to twenty channels)
 - Elastic buffers for inter-chip deskewing and channel-to-channel alignment
- Receiver clock recovery tolerance of up to 75 non-transitioning bits
- 50Ω (RocketIO X) or 50Ω / 75Ω selectable (RocketIO) on-chip transmit and receive terminations
- Programmable comma detection and word alignment
- Rate matching via insertion/deletion characters
- Automatic lock-to-reference function
- Programmable pre-emphasis support
- Per-channel serial and parallel transmitter-to-receiver internal loopback modes
- Optional transmit and receive data inversion
- Cyclic Redundancy Check support (RocketIO only)

PowerPC 405 Processor Block

The PPC405 RISC CPU can execute instructions at a sustained rate of one instruction per cycle. On-chip instruction and data cache reduce design complexity and improve system throughput.

The PPC405 features include:

- PowerPC RISC CPU
 - Implements the PowerPC User Instruction Set Architecture (UISA) and extensions for embedded applications
 - Thirty-two 32-bit general purpose registers (GPRs)
 - Static branch prediction
 - Five-stage pipeline with single-cycle execution of most instructions, including loads/stores
 - Unaligned and aligned load/store support to cache, main memory, and on-chip memory
 - Hardware multiply/divide for faster integer arithmetic (4-cycle multiply, 35-cycle divide)
 - Enhanced string and multiple-word handling
 - Big/little endian operation support
- Storage Control

- Separate instruction and data cache units, both two-way set-associative and non-blocking
- Eight words (32 bytes) per cache line
- 16 KB array Instruction Cache Unit (ICU), 16 KB array Data Cache Unit (DCU)
- Operand forwarding during instruction cache line fill
- Copy-back or write-through DCU strategy
- Doubleword instruction fetch from cache improves branch latency
- Virtual mode memory management unit (MMU)
 - Translation of the 4 GB logical address space into physical addresses
 - Software control of page replacement strategy
 - Supports multiple simultaneous page sizes ranging from 1 KB to 16 MB
- OCM controllers provide dedicated interfaces between Block SelectRAM+ memory and processor block instruction and data paths for high-speed access
- PowerPC timer facilities
 - 64-bit time base
 - Programmable interval timer (PIT)
 - Fixed interval timer (FIT)
 - Watchdog timer (WDT)
- Debug Support
 - Internal debug mode
 - External debug mode
 - Debug Wait mode
 - Real Time Trace debug mode
 - Enhanced debug support with logical operators
 - Instruction trace and trace-back support
 - Forward or backward trace
- Two hardware interrupt levels support
- Advanced power management support

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register and an optional 3-state buffer to be driven directly or through an SDR or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS (3.3V,⁽²⁾ 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V⁽³⁾
- PCI compliant (66 MHz and 33 MHz) at 3.3V⁽³⁾
- GTL and GTLP

1. Refer to [Table 4, Module 2](#) for detailed information about RocketIO and RocketIO X transceiver compatible protocols.

2. Refer to [XAPP659](#) for more information.

3. Refer to [XAPP653](#) for more information.

Virtex-II Pro Ordering Examples

Virtex-II Pro ordering examples are shown in **Figure 1** (flip-chip package) and **Figure 2** (Pb-free wire-bond package).

Example: XC2VP40 -7 FF 1152 C

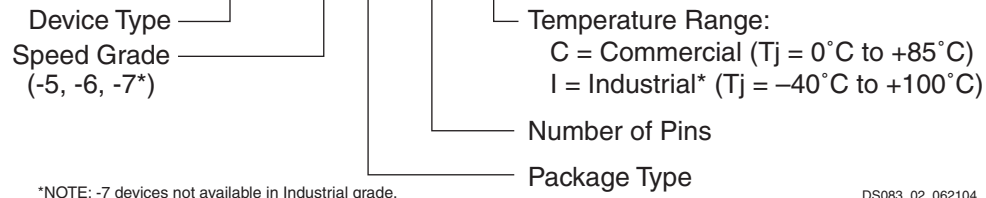


Figure 1: Virtex-II Pro Ordering Example, Flip-Chip Package

Example: XC2VP40 -6 FG G 676 I

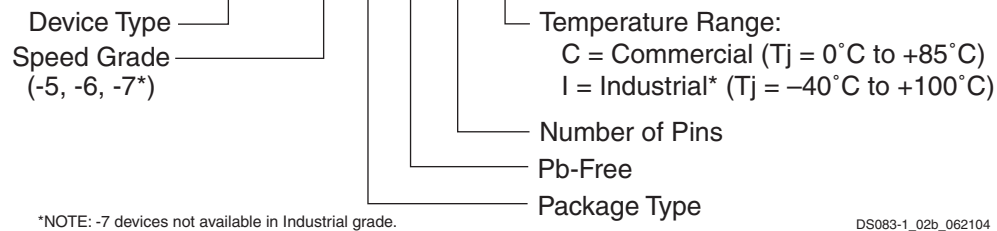


Figure 2: Virtex-II Pro Ordering Example, Pb-Free Wire-Bond Package

Virtex-II Pro X Ordering Example

A Virtex-II Pro X ordering example is shown in **Figure 3**.

Example: XC2VPX20 -6 FF 896 C

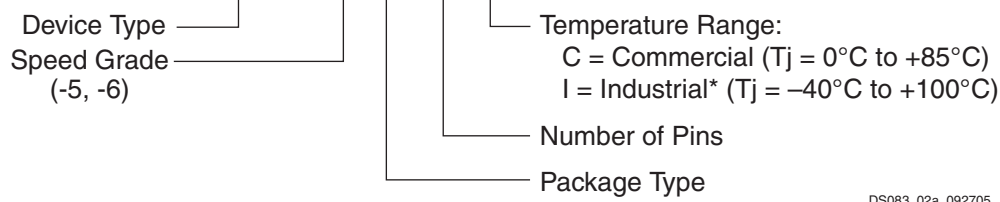
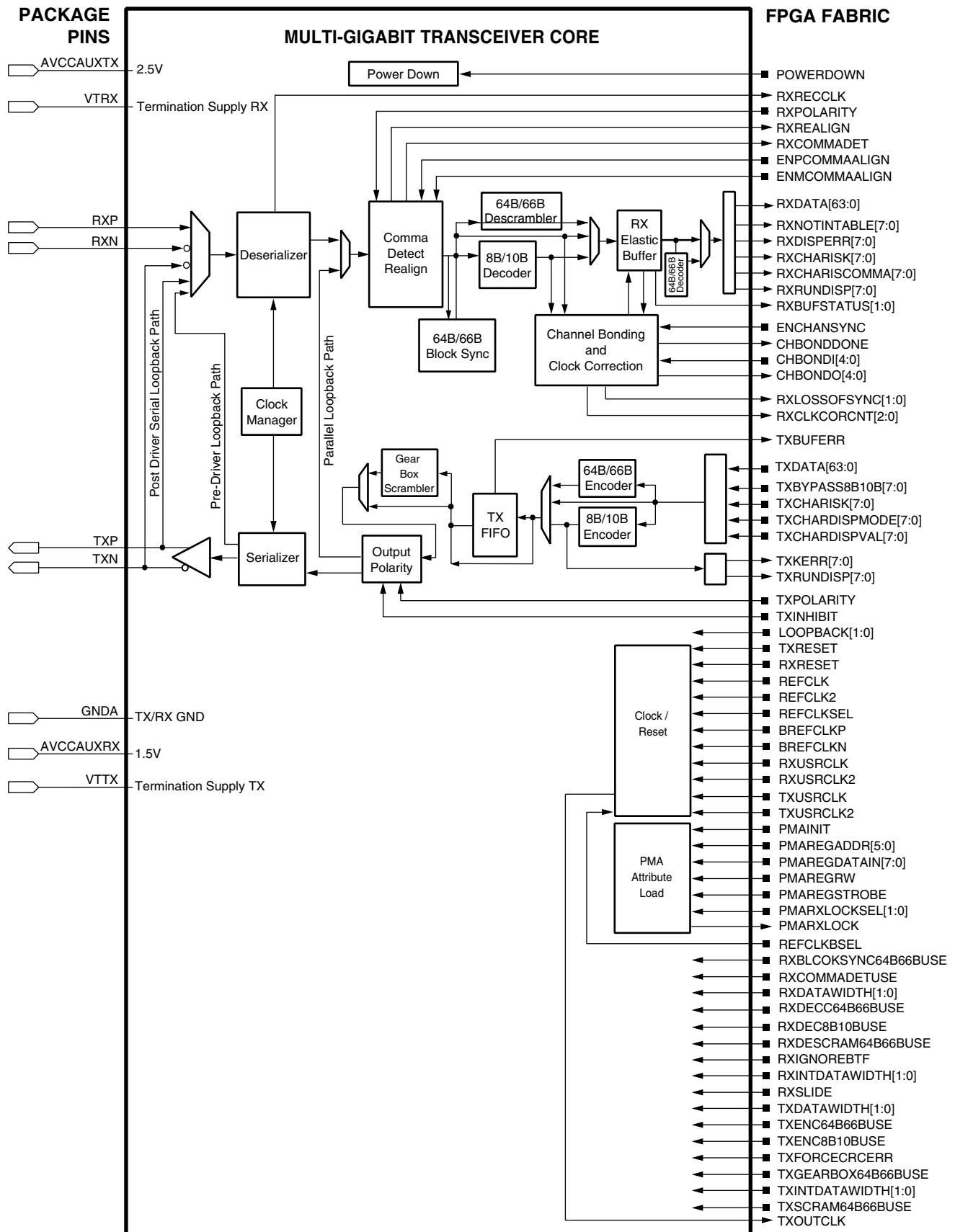


Figure 3: Virtex-II Pro X Ordering Example, Flip-Chip Package



DS083-2_37_050704

Figure 4: RocketIO X Transceiver Block Diagram

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 39**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

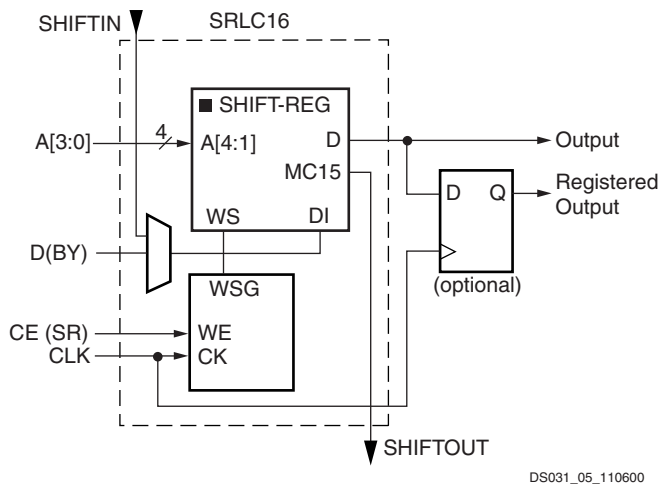


Figure 39: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 40**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

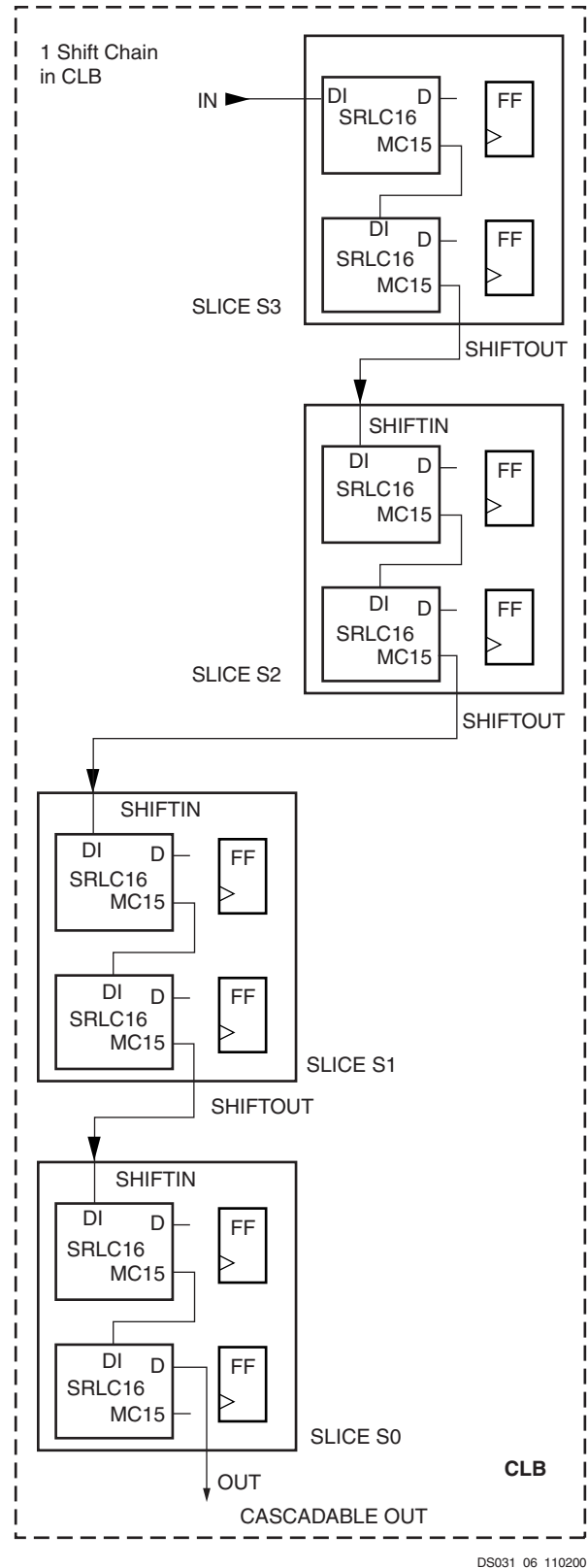


Figure 40: Cascadable Shift Register

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that **Virtex-II Pro Performance Characteristics** are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. **Table 15** correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: Virtex-II Pro Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: Processor Clocks Absolute AC Characteristics

	Speed Grade						
	-7		-6		-5		
Description	Min	Max	Min	Max	Min	Max	Units
CPMC405CLOCK frequency	0	400 ⁽¹⁾	0	350 ⁽¹⁾	0	300	MHz
JTAGC405TCK frequency ⁽²⁾	0	200	0	175	0	150	MHz
PLBCLK ⁽³⁾	0	400	0	350	0	300	MHz
BRAMDSOCMCLK ⁽³⁾	0	400	0	350	0	300	MHz
BRAMISOCMCLK ⁽³⁾	0	400	0	350	0	300	MHz

Notes:

- IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in [XAPP755](#), "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to [Table 1](#), [Module 1](#) to identify dual-processor devices.
- The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
- The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see [PowerPC 405 Processor Block Reference Guide](#) and [XAPP640](#) for more information.

Table 19: Processor Block JTAG Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	T _{PCKK_JTAG} / T _{PCKC_JTAG}	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
JTAG reset input	T _{PCKK_JTAGRST} / T _{PCKC_JTAGRST}	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
Clock to Out					
JTAG control outputs	T _{PCKCO_JTAG}	1.34	1.54	1.69	ns, max

Table 20: PowerPC 405 Data-Side On-Chip Memory Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (BRAMDSOCCLK)					
Data-Side On-Chip Memory data bus inputs	T _{PDCK_DSOCM} / T _{PCKD_DSOCM}	0.73/ 0.83	0.84/ 0.95	0.92/ 1.05	ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	T _{PCKCO_DSOCM}	1.58	1.82	1.99	ns, max
Data-Side On-Chip Memory address bus outputs	T _{PCKAO_DSOCM}	1.46	1.68	1.84	ns, max
Data-Side On-Chip Memory data bus outputs	T _{PCKDO_DSOCM}	0.90	1.03	1.13	ns, max

Table 21: PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (BRAMISOCCLK)					
Instruction-Side On-Chip Memory data bus inputs	T _{PDCK_ISOCM} / T _{PCKD_ISOCM}	0.81/ 0.68	0.93/ 0.78	1.02/ 0.86	ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	T _{PCKCO_ISOCM}	1.33	1.53	1.68	ns, max
Instruction-Side On-Chip Memory address bus outputs	T _{PCKAO_ISOCM}	1.52	1.75	1.92	ns, max
Instruction-Side On-Chip Memory data bus outputs	T _{PCKDO_ISOCM}	1.35	1.55	1.70	ns, max

Table 38: IOB Output Switching Characteristics Standard Adjustments (Continued)

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVC MOS, 2.5V, Fast, 6 mA	LVC MOS25_F6	T _{OLVCMOS25_F6}	0.62	0.71	0.78	ns
LVC MOS, 2.5V, Fast, 8 mA	LVC MOS25_F8	T _{OLVCMOS25_F8}	0.20	0.23	0.25	ns
LVC MOS, 2.5V, Fast, 12 mA	LVC MOS25_F12	T _{OLVCMOS25_F12}	0.00	0.00	0.00	ns
LVC MOS, 2.5V, Fast, 16 mA	LVC MOS25_F16	T _{OLVCMOS25_F16}	−0.03	−0.03	−0.04	ns
LVC MOS, 2.5V, Fast, 24 mA	LVC MOS25_F24	T _{OLVCMOS25_F24}	−0.15	−0.15	−0.15	ns
LVC MOS, 1.8V, Slow, 2 mA	LVC MOS18_S2	T _{OLVCMOS18_S2}	4.20	4.83	5.31	ns
LVC MOS, 1.8V, Slow, 4 mA	LVC MOS18_S4	T _{OLVCMOS18_S4}	2.76	3.18	3.49	ns
LVC MOS, 1.8V, Slow, 6 mA	LVC MOS18_S6	T _{OLVCMOS18_S6}	1.91	2.20	2.41	ns
LVC MOS, 1.8V, Slow, 8 mA	LVC MOS18_S8	T _{OLVCMOS18_S8}	1.92	2.20	2.42	ns
LVC MOS, 1.8V, Slow, 12 mA	LVC MOS18_S12	T _{OLVCMOS18_S12}	1.58	1.81	1.99	ns
LVC MOS, 1.8V, Slow, 16 mA	LVC MOS18_S16	T _{OLVCMOS18_S16}	0.76	0.87	0.96	ns
LVC MOS, 1.8V, Fast, 2 mA	LVC MOS18_F2	T _{OLVCMOS18_F2}	2.34	2.69	2.95	ns
LVC MOS, 1.8V, Fast, 4 mA	LVC MOS18_F4	T _{OLVCMOS18_F4}	0.71	0.81	0.89	ns
LVC MOS, 1.8V, Fast, 6 mA	LVC MOS18_F6	T _{OLVCMOS18_F6}	0.50	0.57	0.63	ns
LVC MOS, 1.8V, Fast, 8 mA	LVC MOS18_F8	T _{OLVCMOS18_F8}	0.48	0.55	0.61	ns
LVC MOS, 1.8V, Fast, 12 mA	LVC MOS18_F12	T _{OLVCMOS18_F12}	0.30	0.34	0.38	ns
LVC MOS, 1.8V, Fast, 16 mA	LVC MOS18_F16	T _{OLVCMOS18_F16}	0.11	0.12	0.13	ns
LVC MOS, 1.5V, Slow, 2 mA	LVC MOS15_S2	T _{OLVCMOS15_S2}	6.19	7.12	7.83	ns
LVC MOS, 1.5V, Slow, 4 mA	LVC MOS15_S4	T _{OLVCMOS15_S4}	4.28	4.93	5.42	ns
LVC MOS, 1.5V, Slow, 6 mA	LVC MOS15_S6	T _{OLVCMOS15_S6}	2.81	3.24	3.56	ns
LVC MOS, 1.5V, Slow, 8 mA	LVC MOS15_S8	T _{OLVCMOS15_S8}	2.55	2.93	3.23	ns
LVC MOS, 1.5V, Slow, 12 mA	LVC MOS15_S12	T _{OLVCMOS15_S12}	1.31	1.51	1.66	ns
LVC MOS, 1.5V, Slow, 16 mA	LVC MOS15_S16	T _{OLVCMOS15_S16}	1.28	1.47	1.62	ns
LVC MOS, 1.5V, Fast, 2 mA	LVC MOS15_F2	T _{OLVCMOS15_F2}	2.26	2.60	2.86	ns
LVC MOS, 1.5V, Fast, 4 mA	LVC MOS15_F4	T _{OLVCMOS15_F4}	1.66	1.90	2.09	ns
LVC MOS, 1.5V, Fast, 6 mA	LVC MOS15_F6	T _{OLVCMOS15_F6}	0.65	0.75	0.82	ns
LVC MOS, 1.5V, Fast, 8 mA	LVC MOS15_F8	T _{OLVCMOS15_F8}	0.94	1.08	1.19	ns
LVC MOS, 1.5V, Fast, 12 mA	LVC MOS15_F12	T _{OLVCMOS15_F12}	0.25	0.29	0.32	ns
LVC MOS, 1.5V, Fast, 16 mA	LVC MOS15_F16	T _{OLVCMOS15_F16}	0.28	0.32	0.35	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T _{OLVDS_25}	0.01	0.01	0.01	ns
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	T _{OLVDS EXT_25}	0.13	0.15	0.16	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T _{OLVDS_25}	0.13	0.14	0.16	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T _{OLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T _{OLDT_25}	0.13	0.14	0.16	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	T _{OLVPECL_25}	0.17	0.19	0.21	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T _{OPCI33_3}	0.83	0.93	1.01	ns
PCI, 66 MHz, 3.3V	PCI66_3	T _{OPCI66_3}	0.89	0.97	1.05	ns
PCI-X, 133 MHz, 3.3V	PCIX	T _{OPCIX}	0.92	1.02	1.10	ns
GTL (Gunning Transceiver Logic)	GTL	T _{OGTL}	0.08	0.10	0.11	ns
GTL Plus	GTL P	T _{OGTL P}	0.04	0.05	0.06	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T _{OHSTL_I}	0.56	0.64	0.70	ns

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II Pro source-synchronous transmitter and receiver data-valid windows.

Table 64: Duty Cycle Distortion and Clock-Tree Skew

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Duty Cycle Distortion ⁽¹⁾	T_{DCD_LOCAL}	All	0.10	0.10	0.20	ns
	T_{DCD_CLK180}		0.10	0.11	0.13	ns
Clock Tree Skew ⁽²⁾	T_{CKSKEW}	XC2VP2	0.13	0.13	0.13	ns
		XC2VP4	0.13	0.13	0.13	ns
		XC2VP7	0.13	0.13	0.13	ns
		XC2VP20	0.20	0.21	0.22	ns
		XC2VPX20	0.20	0.21	0.22	ns
		XC2VP30	0.20	0.22	0.24	ns
		XC2VP40	0.33	0.34	0.35	ns
		XC2VP50	0.40	0.41	0.42	ns
		XC2VP70	0.54	0.59	0.64	ns
		XC2VPX70	0.54	0.59	0.64	ns
		XC2VP100	N/A	0.79	0.87	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
 T_{DCD_LOCAL} applies to cases where the dedicated path from the DCM to the BUFG is bypassed and where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O. Users must follow the implementation guidelines contained in [XAPP685](#) for these specifications to apply.
 T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
- This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L23N_6	Y6	NC		
6	IO_L24P_6	AA4	NC		
6	IO_L24N_6	AA3	NC		
6	IO_L31P_6	AA2			
6	IO_L31N_6	AA1			
6	IO_L33P_6	Y5			
6	IO_L33N_6/VREF_6	W5			
6	IO_L35P_6	Y4			
6	IO_L35N_6	Y3			
6	IO_L36P_6	Y2			
6	IO_L36N_6	Y1			
6	IO_L37P_6	W7			
6	IO_L37N_6	W6			
6	IO_L39P_6	W2			
6	IO_L39N_6/VREF_6	W1			
6	IO_L41P_6	V8			
6	IO_L41N_6	V7			
6	IO_L42P_6	V6			
6	IO_L42N_6	V5			
6	IO_L43P_6	V4			
6	IO_L43N_6	V3			
6	IO_L45P_6	V2			
6	IO_L45N_6/VREF_6	V1			
6	IO_L47P_6	U8			
6	IO_L47N_6	T8			
6	IO_L48P_6	U5			
6	IO_L48N_6	U4			
6	IO_L49P_6	U3			
6	IO_L49N_6	T3			
6	IO_L51P_6	U2			
6	IO_L51N_6/VREF_6	U1			
6	IO_L53P_6	T7			
6	IO_L53N_6	R7			
6	IO_L54P_6	T6			
6	IO_L54N_6	T5			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		C14			
N/A	GND		C3			
N/A	GND		B29			
N/A	GND		B2			
N/A	GND		A22			
N/A	GND		A9			

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	VCCINT	Y13				
N/A	VCCINT	Y22				
N/A	VCCINT	AA13				
N/A	VCCINT	AA22				
N/A	VCCINT	AB13				
N/A	VCCINT	AB14				
N/A	VCCINT	AB15				
N/A	VCCINT	AB16				
N/A	VCCINT	AB17				
N/A	VCCINT	AB18				
N/A	VCCINT	AB19				
N/A	VCCINT	AB20				
N/A	VCCINT	AB21				
N/A	VCCINT	AB22				
N/A	VCCINT	AC12				
N/A	VCCINT	AC23				
N/A	VCCINT	AD11				
N/A	VCCINT	AD24				
N/A	VCCAUX	C3				
N/A	VCCAUX	C4				
N/A	VCCAUX	C17				
N/A	VCCAUX	C18				
N/A	VCCAUX	C31				
N/A	VCCAUX	C32				
N/A	VCCAUX	D3				
N/A	VCCAUX	D32				
N/A	VCCAUX	U1				
N/A	VCCAUX	V1				
N/A	VCCAUX	U34				
N/A	VCCAUX	V34				
N/A	VCCAUX	AL3				
N/A	VCCAUX	AL32				
N/A	VCCAUX	AM3				
N/A	VCCAUX	AM4				
N/A	VCCAUX	AM17				
N/A	VCCAUX	AM18				
N/A	VCCAUX	AM31				
N/A	VCCAUX	AM32				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L17N_3	AH9		
3	IO_L17P_3	AJ9		
3	IO_L16N_3	AK7		
3	IO_L16P_3	AL7		
3	IO_L15N_3/VREF_3	AK4		
3	IO_L15P_3	AL4		
3	IO_L14N_3	AJ7		
3	IO_L14P_3	AJ8		
3	IO_L13N_3	AK3		
3	IO_L13P_3	AL3		
3	IO_L12N_3	AL5		
3	IO_L12P_3	AL6		
3	IO_L11N_3	AK8		
3	IO_L11P_3	AL8		
3	IO_L10N_3	AL1		
3	IO_L10P_3	AL2		
3	IO_L09N_3/VREF_3	AM6		
3	IO_L09P_3	AM7		
3	IO_L08N_3	AL9		
3	IO_L08P_3	AM9		
3	IO_L07N_3	AM5		
3	IO_L07P_3	AN5		
3	IO_L06N_3	AM1		
3	IO_L06P_3	AM2		
3	IO_L05N_3	AN8		
3	IO_L05P_3	AN9		
3	IO_L04N_3	AN6		
3	IO_L04P_3	AP6		
3	IO_L03N_3/VREF_3	AN4		
3	IO_L03P_3	AP4		
3	IO_L02N_3	AN7		
3	IO_L02P_3	AP7		
3	IO_L01N_3/VRP_3	AN3		
3	IO_L01P_3/VRN_3	AP3		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AK10		
4	IO_L01P_4/INIT_B	AJ10		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AF11		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L27P_5	AL23		
5	IO_L26N_5	AD22		
5	IO_L26P_5	AE22		
5	IO_L25N_5	AJ23		
5	IO_L25P_5	AK23		
5	IO_L21N_5	AN24		
5	IO_L21P_5	AP24		
5	IO_L20N_5	AE23		
5	IO_L20P_5	AF23		
5	IO_L19N_5	AM23		
5	IO_L19P_5	AM24		
5	IO_L09N_5/VREF_5	AJ24		
5	IO_L09P_5	AK24		
5	IO_L08N_5	AG22		
5	IO_L08P_5	AG23		
5	IO_L07N_5/VREF_5	AH23		
5	IO_L07P_5	AH24		
5	IO_L06N_5/VRP_5	AN25		
5	IO_L06P_5/VRN_5	AP25		
5	IO_L05_5/No_Pair	AH25		
5	IO_L03N_5/D4	AL25		
5	IO_L03P_5/D5	AM25		
5	IO_L02N_5/D6	AE24		
5	IO_L02P_5/D7	AF24		
5	IO_L01N_5/RDWR_B	AJ25		
5	IO_L01P_5/CS_B	AK25		
6	IO_L01P_6/VRN_6	AP32		
6	IO_L01N_6/VRP_6	AN32		
6	IO_L02P_6	AP28		
6	IO_L02N_6	AN28		
6	IO_L03P_6	AP31		
6	IO_L03N_6/VREF_6	AN31		
6	IO_L04P_6	AP29		
6	IO_L04N_6	AN29		
6	IO_L05P_6	AN26		
6	IO_L05N_6	AN27		
6	IO_L06P_6	AM33		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AP5		
N/A	GND	AK5		
N/A	GND	AF5		
N/A	GND	AB5		
N/A	GND	W5		
N/A	GND	T5		
N/A	GND	N5		
N/A	GND	J5		
N/A	GND	E5		
N/A	GND	A5		
N/A	GND	AM3		
N/A	GND	C3		
N/A	GND	AN2		
N/A	GND	B2		
N/A	GND	AK1		
N/A	GND	AF1		
N/A	GND	AB1		
N/A	GND	W1		
N/A	GND	V1		
N/A	GND	T1		
N/A	GND	N1		
N/A	GND	J1		
N/A	GND	E1		

Notes:

1. See [Table 4](#) for an explanation of the signals available on this pin.

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	AVCCAUXTX6	B23		
N/A	VTTXPAD6	B24		
N/A	TXNPAD6	A24		
N/A	TXPPAD6	A23		
N/A	GND A6	C24		
N/A	RXPPAD6	A22		
N/A	RXNPAD6	A21		
N/A	VTRXPAD6	B22		
N/A	AVCCAUXRX6	B21		
N/A	AVCCAUXTX7	B18		
N/A	VTTXPAD7	B19		
N/A	TXNPAD7	A19		
N/A	TXPPAD7	A18		
N/A	GND A7	C16		
N/A	RXPPAD7	A17		
N/A	RXNPAD7	A16		
N/A	VTRXPAD7	B17		
N/A	AVCCAUXRX7	B16		
N/A	AVCCAUXTX8	B14		
N/A	VTTXPAD8	B15		
N/A	TXNPAD8	A15		
N/A	TXPPAD8	A14		
N/A	GND A8	C13		
N/A	RXPPAD8	A13		
N/A	RXNPAD8	A12		
N/A	VTRXPAD8	B13		
N/A	AVCCAUXRX8	B12		
N/A	AVCCAUXTX9	B10		
N/A	VTTXPAD9	B11		
N/A	TXNPAD9	A11		
N/A	TXPPAD9	A10		
N/A	GND A9	C9		
N/A	RXPPAD9	A9		
N/A	RXNPAD9	A8		
N/A	VTRXPAD9	B9		
N/A	AVCCAUXRX9	B8		
N/A	AVCCAUXTX11	B6		
N/A	VTTXPAD11	B7		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L87P_4/VREF_4		AP15	NC	
4	IO_L37N_4		AV15		
4	IO_L37P_4		AU15		
4	IO_L38N_4		AY14		
4	IO_L38P_4		AY15		
4	IO_L39N_4		AM16		
4	IO_L39P_4		AL16		
4	IO_L43N_4		AP16		
4	IO_L43P_4		AN16		
4	IO_L44N_4		AR16		
4	IO_L44P_4		AT16		
4	IO_L45N_4		AV16		
4	IO_L45P_4/VREF_4		AU16		
4	IO_L46N_4		AL18		
4	IO_L46P_4		AL17		
4	IO_L47N_4		AM17		
4	IO_L47P_4		AN17		
4	IO_L48N_4		AR17		
4	IO_L48P_4		AP17		
4	IO_L49N_4		AU17		
4	IO_L49P_4		AT17		
4	IO_L50_4/No_Pair		AW16		
4	IO_L53_4/No_Pair		AW17		
4	IO_L54N_4		AN18		
4	IO_L54P_4		AM18		
4	IO_L55N_4		AT18		
4	IO_L55P_4		AR18		
4	IO_L56N_4		AV17		
4	IO_L56P_4		AV18		
4	IO_L57N_4		AY18		
4	IO_L57P_4/VREF_4		AY17		
4	IO_L58N_4		AM19		
4	IO_L58P_4		AL19		
4	IO_L59N_4		AP19		
4	IO_L59P_4		AN19		
4	IO_L60N_4		AT19		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L59N_2	AA11	
2	IO_L59P_2	AA12	
2	IO_L60N_2	W1	
2	IO_L60P_2	W2	
2	IO_L85N_2	Y2	
2	IO_L85P_2	Y3	
2	IO_L86N_2	AA9	
2	IO_L86P_2	AA10	
2	IO_L87N_2	AA5	
2	IO_L87P_2	AA6	
2	IO_L88N_2/VREF_2	AA4	
2	IO_L88P_2	Y4	
2	IO_L89N_2	AA7	
2	IO_L89P_2	AA8	
2	IO_L90N_2	AA2	
2	IO_L90P_2	AA3	
3	IO_L90N_3	AB5	
3	IO_L90P_3	AB6	
3	IO_L89N_3	AB11	
3	IO_L89P_3	AB12	
3	IO_L88N_3	AB2	
3	IO_L88P_3	AB3	
3	IO_L87N_3/VREF_3	AB4	
3	IO_L87P_3	AC4	
3	IO_L86N_3	AB9	
3	IO_L86P_3	AB10	
3	IO_L85N_3	AC2	
3	IO_L85P_3	AC3	
3	IO_L60N_3	AD5	
3	IO_L60P_3	AD6	
3	IO_L59N_3	AB7	
3	IO_L59P_3	AB8	
3	IO_L58N_3	AD1	
3	IO_L58P_3	AD2	
3	IO_L57N_3/VREF_3	AE4	
3	IO_L57P_3	AE5	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	

Date	Version	Revision
11/17/04	4.1	Table 4: Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
03/01/05	4.2	Table 3: Corrected number of Differential I/O Pairs for XC2VP30-FF1152 from 340 to 316. Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”.
06/20/05	4.3	<i>No changes in Module 4 for this revision.</i>
09/15/05	4.4	<i>No changes in Module 4 for this revision.</i>
10/10/05	4.5	<i>No changes in Module 4 for this revision.</i>
03/05/07	4.6	Figure 2, page 29: Corrected NOTE 3. Figure 7, page 161: Updated with drawing showing correct heat sink profile and detail.
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added <i>Product Not Recommended for New Designs</i> banner. Updated Figure 3, page 50 , with the newest FG676/FGG676 mechanical drawing.

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Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)