AMD Xilinx - XC2VP70-5FF1517C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-5ff1517c

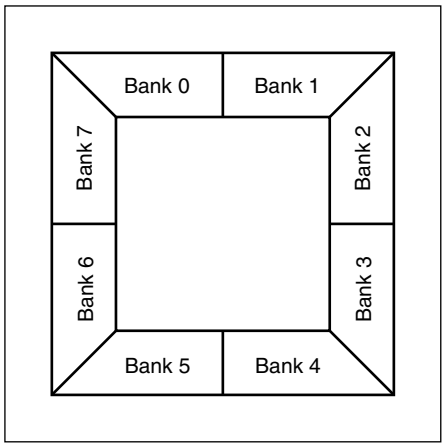


Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

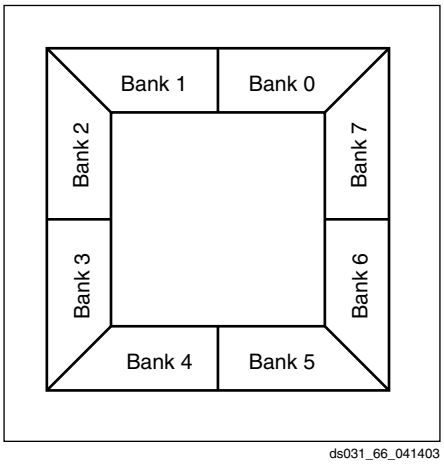


Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

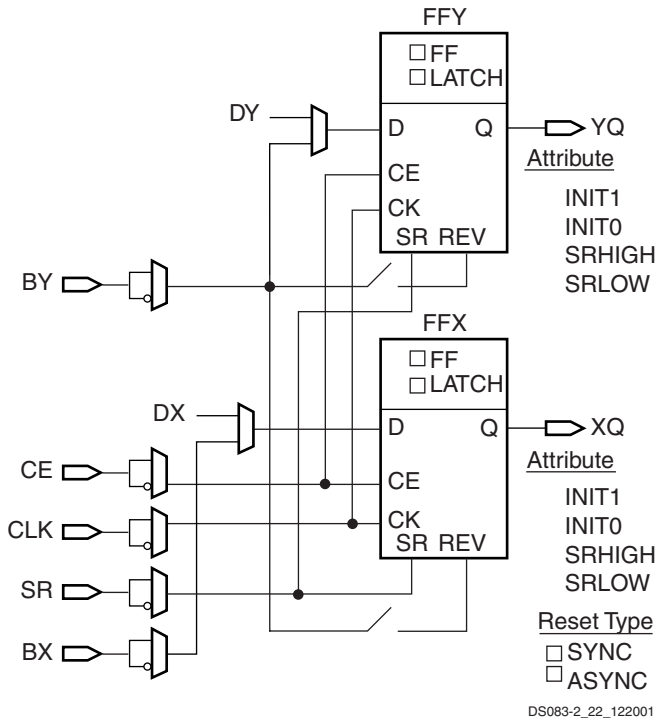


Figure 35: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM
- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: **Distributed SelectRAM+ Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

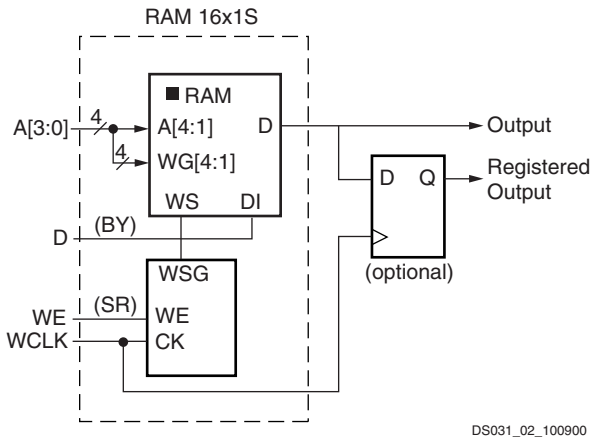


Figure 36: **Distributed SelectRAM+ (RAM16x1S)**

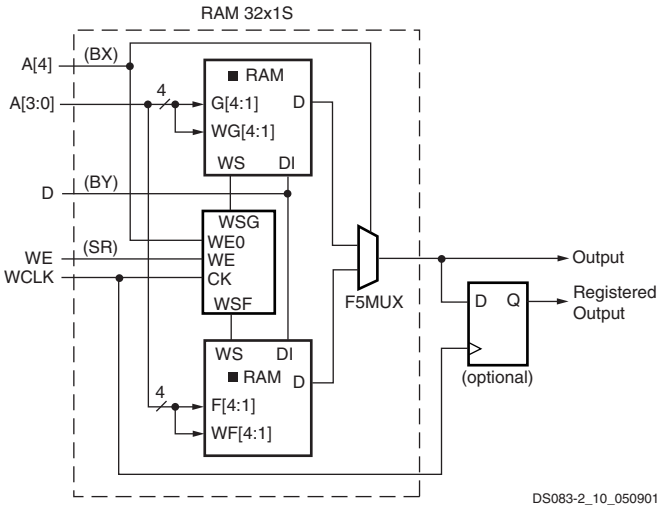


Figure 37: **Single-Port Distributed SelectRAM+ (RAM32x1S)**

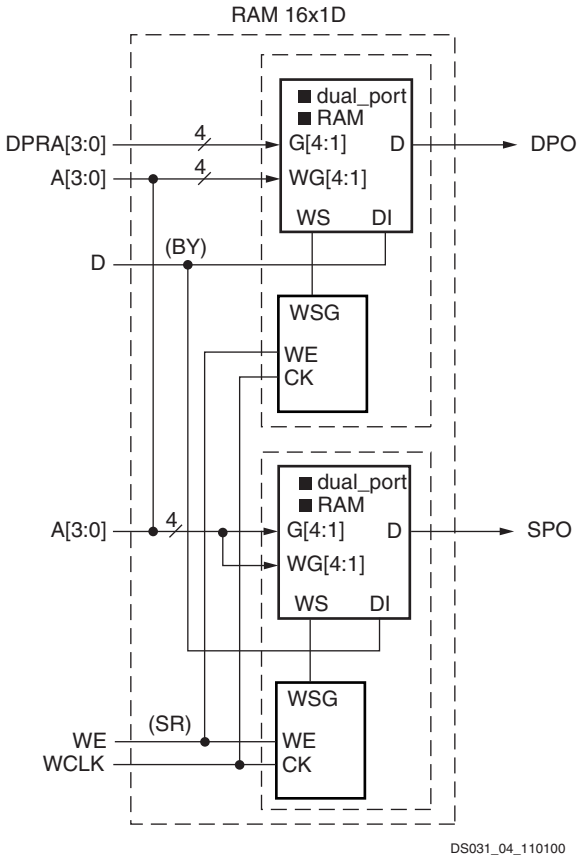


Figure 38: **Dual-Port Distributed SelectRAM+ (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

Table 17: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Multiplexers

Virtex-II Pro function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II Pro slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 41. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Pro Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

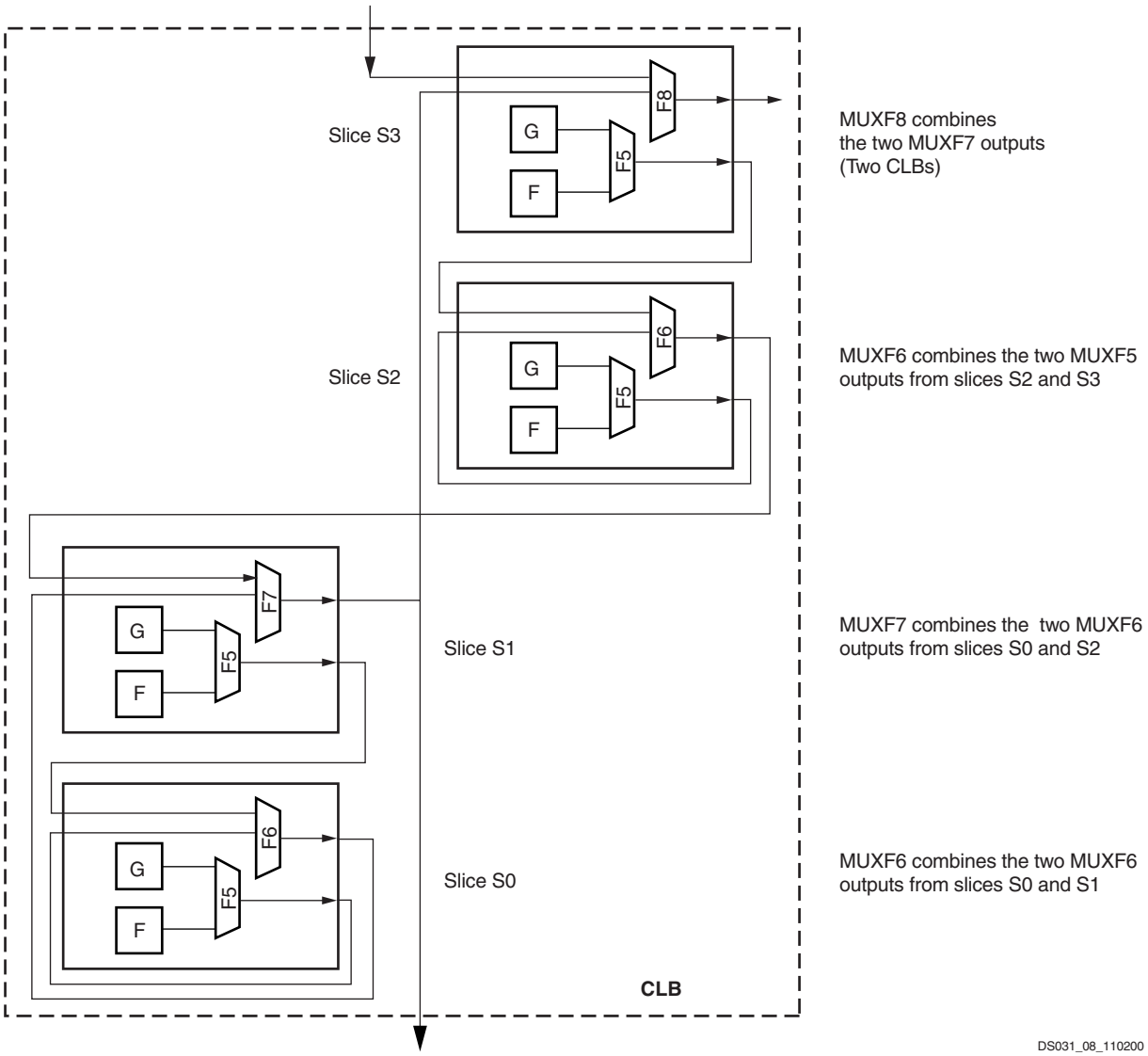


Figure 41: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II Pro CLB has two separate carry chains, as shown in the Figure 42.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II Pro device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 34) improves the efficiency of multiplier implementation.

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

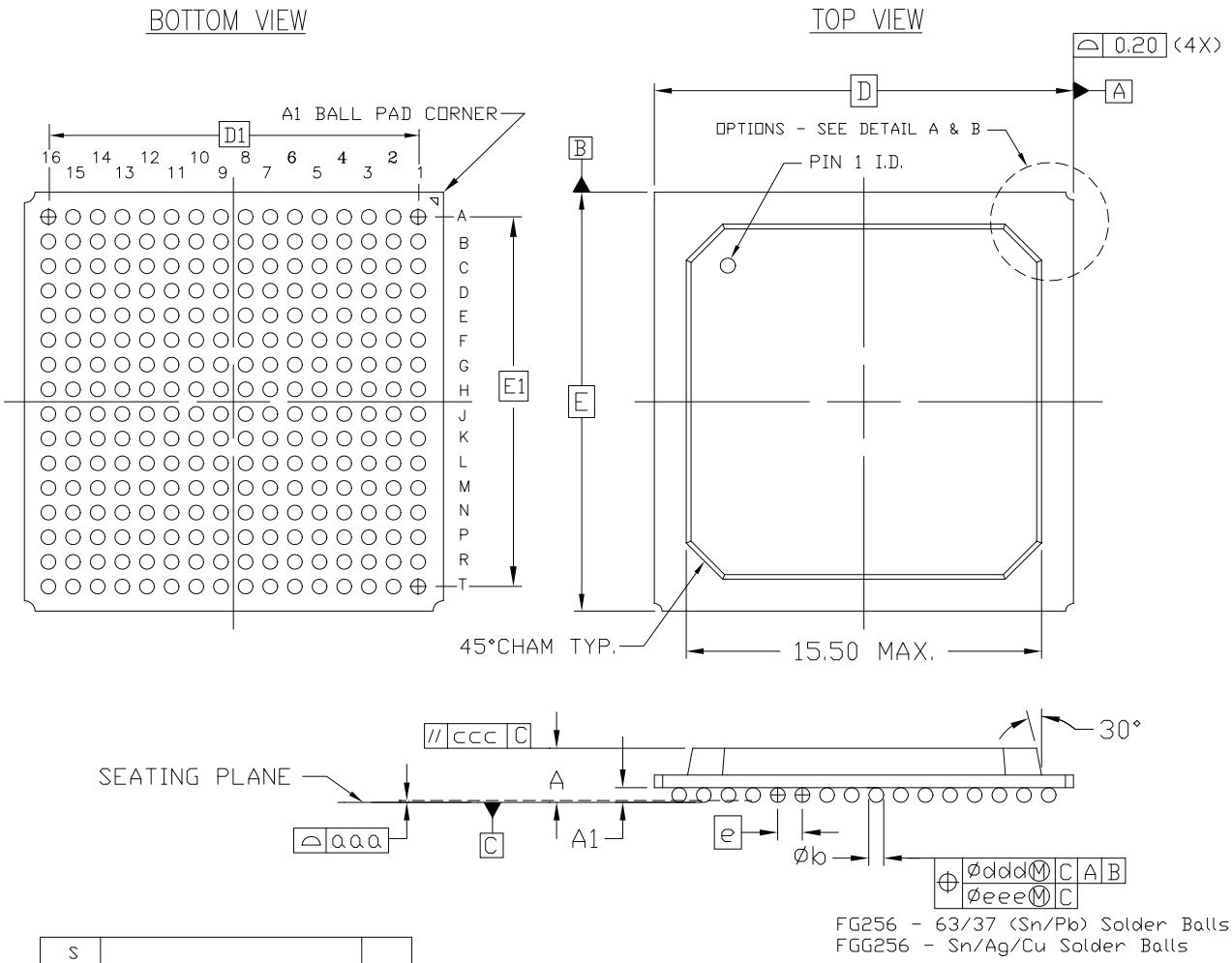
Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

Figure 1: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCAUX	L1			
N/A	VCCAUX	B21			
N/A	VCCAUX	B2			
N/A	VCCAUX	AB11			
N/A	VCCAUX	AA21			
N/A	VCCAUX	AA2			
N/A	VCCAUX	A12			
N/A	GND	Y3			
N/A	GND	Y20			
N/A	GND	W4			
N/A	GND	W19			
N/A	GND	V5			
N/A	GND	V18			
N/A	GND	P9			
N/A	GND	P14			
N/A	GND	P13			
N/A	GND	P12			
N/A	GND	P11			
N/A	GND	P10			
N/A	GND	N9			
N/A	GND	N14			
N/A	GND	N13			
N/A	GND	N12			
N/A	GND	N11			
N/A	GND	N10			
N/A	GND	M9			
N/A	GND	M14			
N/A	GND	M13			
N/A	GND	M12			
N/A	GND	M11			
N/A	GND	M10			
N/A	GND	M1			
N/A	GND	L9			
N/A	GND	L22			
N/A	GND	L14			
N/A	GND	L13			
N/A	GND	L12			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L44P_7	G24	NC		
7	IO_L44N_7	G23	NC		
7	IO_L43P_7	G22	NC		
7	IO_L43N_7	G21	NC		
7	IO_L42P_7	F25	NC	NC	NC
7	IO_L42N_7	F24	NC	NC	NC
7	IO_L40P_7	F23	NC	NC	NC
7	IO_L40N_7/VREF_7	F22	NC	NC	NC
7	IO_L06P_7	E26			
7	IO_L06N_7	E25			
7	IO_L05P_7	E24			
7	IO_L05N_7	E23			
7	IO_L04P_7	D26			
7	IO_L04N_7/VREF_7	D25			
7	IO_L03P_7	C26			
7	IO_L03N_7	C25			
7	IO_L02P_7	B26			
7	IO_L02N_7	A25			
7	IO_L01P_7/VRN_7	D24			
7	IO_L01N_7/VRP_7	C23			
0	VCCO_0	C17			
0	VCCO_0	C20			
0	VCCO_0	H17			
0	VCCO_0	H18			
0	VCCO_0	J14			
0	VCCO_0	J15			
0	VCCO_0	J16			
1	VCCO_1	C7			
1	VCCO_1	H9			
1	VCCO_1	C10			
1	VCCO_1	H10			
1	VCCO_1	J11			
1	VCCO_1	J12			
1	VCCO_1	J13			
2	VCCO_2	G2			
2	VCCO_2	J8			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	R15			
N/A	GND	R16			
N/A	GND	R17			
N/A	GND	T11			
N/A	GND	T12			
N/A	GND	T13			
N/A	GND	T14			
N/A	GND	T15			
N/A	GND	T16			
N/A	GND	U10			
N/A	GND	U12			
N/A	GND	U13			
N/A	GND	U14			
N/A	GND	U15			
N/A	GND	U17			
N/A	GND	Y20			
N/A	GND	AA21			
N/A	GND	AB22			
N/A	GND	AC23			
N/A	GND	AD24			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L36N_7		F27	NC		
7	IO_L35P_7		K24	NC		
7	IO_L35N_7		K23	NC		
7	IO_L34P_7		E30	NC		
7	IO_L34N_7/VREF_7		E29	NC		
7	IO_L33P_7		E28	NC		
7	IO_L33N_7		E27	NC		
7	IO_L32P_7		H26	NC		
7	IO_L32N_7		H25	NC		
7	IO_L31P_7		D30	NC		
7	IO_L31N_7		D29	NC		
7	IO_L06P_7		D28			
7	IO_L06N_7		C27			
7	IO_L05P_7		J24			
7	IO_L05N_7		J23			
7	IO_L04P_7		C30			
7	IO_L04N_7/VREF_7		C29			
7	IO_L03P_7		D26			
7	IO_L03N_7		C26			
7	IO_L02P_7		G26			
7	IO_L02N_7		G25			
7	IO_L01P_7/VRN_7		B28			
7	IO_L01N_7/VRP_7		A28			
0	VCCO_0		K21			
0	VCCO_0		K20			
0	VCCO_0		K19			
0	VCCO_0		K18			
0	VCCO_0		K17			
0	VCCO_0		K16			
0	VCCO_0		J21			
0	VCCO_0		J20			
0	VCCO_0		J19			
0	VCCO_0		J18			
1	VCCO_1		K15			
1	VCCO_1		K14			

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E29				
0	IO_L01P_0/VRN_0	E28				
0	IO_L02N_0	H26				
0	IO_L02P_0	G26				
0	IO_L03N_0	H25				
0	IO_L03P_0/VREF_0	G25				
0	IO_L05_0/No_Pair	J25				
0	IO_L06N_0	K24				
0	IO_L06P_0	J24				
0	IO_L07N_0	F26				
0	IO_L07P_0	E26				
0	IO_L08N_0	D30				
0	IO_L08P_0	D29				
0	IO_L09N_0	K23				
0	IO_L09P_0/VREF_0	J23				
0	IO_L19N_0	F24	NC	NC		
0	IO_L19P_0	E24	NC	NC		
0	IO_L20N_0	D28	NC	NC		
0	IO_L20P_0	C28	NC	NC		
0	IO_L21N_0	H24	NC	NC		
0	IO_L21P_0	G24	NC	NC		
0	IO_L25N_0	G23	NC	NC		
0	IO_L25P_0	F23	NC	NC		
0	IO_L26N_0	E27	NC	NC		
0	IO_L26P_0	D27	NC	NC		
0	IO_L27N_0	K22	NC	NC		
0	IO_L27P_0/VREF_0	J22	NC	NC		
0	IO_L37N_0	H22				
0	IO_L37P_0	G22				
0	IO_L38N_0	D26				
0	IO_L38P_0	C26				
0	IO_L39N_0	K21				
0	IO_L39P_0	J21				
0	IO_L43N_0	F22				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L34P_6	AE30				
6	IO_L34N_6	AE31				
6	IO_L35P_6	AD27				
6	IO_L35N_6	AD28				
6	IO_L36P_6	AF33				
6	IO_L36N_6	AE33				
6	IO_L37P_6	AD29				
6	IO_L37N_6	AD30				
6	IO_L38P_6	AB25				
6	IO_L38N_6	AB26				
6	IO_L39P_6	AD31				
6	IO_L39N_6/VREF_6	AD32				
6	IO_L40P_6	AC28				
6	IO_L40N_6	AC29				
6	IO_L41P_6	AB27				
6	IO_L41N_6	AB28				
6	IO_L42P_6	AE34				
6	IO_L42N_6	AD34				
6	IO_L43P_6	AC31				
6	IO_L43N_6	AC32				
6	IO_L44P_6	AA25				
6	IO_L44N_6	AA26				
6	IO_L45P_6	AD33				
6	IO_L45N_6/VREF_6	AC33				
6	IO_L46P_6	AB29				
6	IO_L46N_6	AB30				
6	IO_L47P_6	AA27				
6	IO_L47N_6	AA28				
6	IO_L48P_6	AB31				
6	IO_L48N_6	AB32				
6	IO_L49P_6	AA29				
6	IO_L49N_6	AA30				
6	IO_L50P_6	Y25				
6	IO_L50N_6	Y26				
6	IO_L51P_6	AC34				
6	IO_L51N_6/VREF_6	AB34				
6	IO_L52P_6	AA31				
6	IO_L52N_6	AA32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	VCCINT	Y13				
N/A	VCCINT	Y22				
N/A	VCCINT	AA13				
N/A	VCCINT	AA22				
N/A	VCCINT	AB13				
N/A	VCCINT	AB14				
N/A	VCCINT	AB15				
N/A	VCCINT	AB16				
N/A	VCCINT	AB17				
N/A	VCCINT	AB18				
N/A	VCCINT	AB19				
N/A	VCCINT	AB20				
N/A	VCCINT	AB21				
N/A	VCCINT	AB22				
N/A	VCCINT	AC12				
N/A	VCCINT	AC23				
N/A	VCCINT	AD11				
N/A	VCCINT	AD24				
N/A	VCCAUX	C3				
N/A	VCCAUX	C4				
N/A	VCCAUX	C17				
N/A	VCCAUX	C18				
N/A	VCCAUX	C31				
N/A	VCCAUX	C32				
N/A	VCCAUX	D3				
N/A	VCCAUX	D32				
N/A	VCCAUX	U1				
N/A	VCCAUX	V1				
N/A	VCCAUX	U34				
N/A	VCCAUX	V34				
N/A	VCCAUX	AL3				
N/A	VCCAUX	AL32				
N/A	VCCAUX	AM3				
N/A	VCCAUX	AM4				
N/A	VCCAUX	AM17				
N/A	VCCAUX	AM18				
N/A	VCCAUX	AM31				
N/A	VCCAUX	AM32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AF34				
N/A	GND	B34				
N/A	GND	C1				
N/A	GND	C2				
N/A	GND	C10				
N/A	GND	C16				
N/A	GND	C19				
N/A	GND	C25				
N/A	GND	C33				
N/A	GND	C34				
N/A	GND	D4				
N/A	GND	D31				
N/A	GND	E5				
N/A	GND	E12				
N/A	GND	E23				
N/A	GND	E30				
N/A	GND	F6				
N/A	GND	F29				
N/A	GND	G7				
N/A	GND	G28				
N/A	GND	B1				
N/A	GND	H8				
N/A	GND	H12				
N/A	GND	H15				
N/A	GND	H20				
N/A	GND	J1				
N/A	GND	H27				
N/A	GND	AF1				
N/A	GND	K3				
N/A	GND	K32				
N/A	GND	M5				
N/A	GND	M8				
N/A	GND	M27				
N/A	GND	M30				
N/A	GND	P14				
N/A	GND	P15				
N/A	GND	P16				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AG8				
N/A	GND	AG12				
N/A	GND	AG15				
N/A	GND	AG20				
N/A	GND	AG23				
N/A	GND	AG27				
N/A	GND	J34				
N/A	GND	AH7				
N/A	GND	AH28				
N/A	GND	AJ6				
N/A	GND	AJ29				
N/A	GND	AK5				
N/A	GND	AK12				
N/A	GND	AK23				
N/A	GND	AK30				
N/A	GND	AL4				
N/A	GND	AL31				
N/A	GND	AM1				
N/A	GND	AM2				
N/A	GND	AM10				
N/A	GND	AM16				
N/A	GND	AM19				
N/A	GND	AM25				
N/A	GND	AM33				
N/A	GND	AM34				
N/A	GND	AN1				
N/A	GND	AN34				

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L69P_5	AJ18		
5	IO_L68N_5	AF18		
5	IO_L68P_5	AG18		
5	IO_L67N_5	AM19		
5	IO_L67P_5	AN19		
5	IO_L66N_5/VREF_5	AH19	NC	
5	IO_L66P_5	AJ19	NC	
5	IO_L57N_5/VREF_5	AN20		
5	IO_L57P_5	AP20		
5	IO_L56N_5	AD19		
5	IO_L56P_5	AE19		
5	IO_L55N_5	AL19		
5	IO_L55P_5	AM20		
5	IO_L54N_5	AJ20		
5	IO_L54P_5	AK20		
5	IO_L53_5/No_Pair	AG19		
5	IO_L50_5/No_Pair	AH20		
5	IO_L49N_5	AN21		
5	IO_L49P_5	AP21		
5	IO_L48N_5	AL21		
5	IO_L48P_5	AM21		
5	IO_L47N_5	AD20		
5	IO_L47P_5	AE20		
5	IO_L46N_5	AJ21		
5	IO_L46P_5	AK21		
5	IO_L45N_5/VREF_5	AG21		
5	IO_L45P_5	AH21		
5	IO_L44N_5	AD21		
5	IO_L44P_5	AE21		
5	IO_L43N_5	AM22		
5	IO_L43P_5	AN22		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AJ22		
5	IO_L38N_5	AF20		
5	IO_L38P_5	AF21		
5	IO_L37N_5	AN23		
5	IO_L37P_5	AP23		
5	IO_L27N_5/VREF_5	AL22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L44N_6	AA28		
6	IO_L45P_6	AC31		
6	IO_L45N_6/VREF_6	AC32		
6	IO_L46P_6	AC29		
6	IO_L46N_6	AC30		
6	IO_L47P_6	AA24		
6	IO_L47N_6	AA25		
6	IO_L48P_6	AB32		
6	IO_L48N_6	AB33		
6	IO_L49P_6	AB28		
6	IO_L49N_6	AB29		
6	IO_L50P_6	AA26		
6	IO_L50N_6	Y26		
6	IO_L51P_6	AA33		
6	IO_L51N_6/VREF_6	AA34		
6	IO_L52P_6	AB31		
6	IO_L52N_6	AA31		
6	IO_L53P_6	Y24		
6	IO_L53N_6	Y25		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AA30		
6	IO_L55P_6	Y33		
6	IO_L55N_6	Y34		
6	IO_L56P_6	Y28		
6	IO_L56N_6	W27		
6	IO_L57P_6	AA32		
6	IO_L57N_6/VREF_6	Y32		
6	IO_L58P_6	Y29		
6	IO_L58N_6	Y30		
6	IO_L59P_6	W24		
6	IO_L59N_6	W25		
6	IO_L60P_6	W31		
6	IO_L60N_6	W32		
6	IO_L85P_6	W28		
6	IO_L85N_6	W29		
6	IO_L86P_6	V26		
6	IO_L86N_6	V27		
6	IO_L87P_6	W33		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L02P_6	BA34	
6	IO_L02N_6	AY34	
6	IO_L03P_6	BB37	
6	IO_L03N_6/VREF_6	BA37	
6	IO_L04P_6	BB36	
6	IO_L04N_6	BA36	
6	IO_L05P_6	AW34	
6	IO_L05N_6	AW35	
6	IO_L06P_6	BB35	
6	IO_L06N_6	BA35	
6	IO_L73P_6	BA38	
6	IO_L73N_6	AY38	
6	IO_L74P_6	AU34	
6	IO_L74N_6	AT34	
6	IO_L75P_6	AY39	
6	IO_L75N_6/VREF_6	AY40	
6	IO_L76P_6	AY37	
6	IO_L76N_6	AW36	
6	IO_L77P_6	AR34	
6	IO_L77N_6	AR35	
6	IO_L78P_6	AY35	
6	IO_L78N_6	AY36	
6	IO_L79P_6	AW41	
6	IO_L79N_6	AW42	
6	IO_L80P_6	AP35	
6	IO_L80N_6	AN34	
6	IO_L81P_6	AW40	
6	IO_L81N_6/VREF_6	AV40	
6	IO_L82P_6	AW39	
6	IO_L82N_6	AV39	
6	IO_L83P_6	AM34	
6	IO_L83N_6	AM35	
6	IO_L84P_6	AW38	
6	IO_L84N_6	AV37	
6	IO_L61P_6	AV41	
6	IO_L61N_6	AU40	
6	IO_L62P_6	AL34	