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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-5ff1517i

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: **Processor Clocks Absolute AC Characteristics**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	400(1)	0	350(1)	0	300	MHz
JTAGC405TCK frequency(2)	0	200	0	175	0	150	MHz
PLBCLK(3)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(3)	0	400	0	350	0	300	MHz
BRAMISOCMCLK(3)	0	400	0	350	0	300	MHz

Notes:

1. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1, Module 1 to identify dual-processor devices.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PowerPC 405 Processor Block Reference Guide*** and **XAPP640** for more information.

Table 38: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.62	0.71	0.78	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.20	0.23	0.25	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.00	0.00	0.00	ns
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.03	–0.03	–0.04	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.15	–0.15	–0.15	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	4.20	4.83	5.31	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	2.76	3.18	3.49	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	1.91	2.20	2.41	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	1.92	2.20	2.42	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	1.58	1.81	1.99	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	0.76	0.87	0.96	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	2.34	2.69	2.95	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	0.71	0.81	0.89	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.50	0.57	0.63	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.48	0.55	0.61	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.30	0.34	0.38	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.11	0.12	0.13	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	6.19	7.12	7.83	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	4.28	4.93	5.42	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	2.81	3.24	3.56	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	2.55	2.93	3.23	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	1.31	1.51	1.66	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	1.28	1.47	1.62	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	2.26	2.60	2.86	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	1.66	1.90	2.09	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	0.65	0.75	0.82	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.94	1.08	1.19	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.25	0.29	0.32	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.28	0.32	0.35	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	0.01	0.01	0.01	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	0.13	0.15	0.16	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	0.13	0.14	0.16	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	0.13	0.14	0.16	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{OLVPECL\_25}$	0.17	0.19	0.21	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	0.83	0.93	1.01	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	0.89	0.97	1.05	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	0.92	1.02	1.10	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	0.08	0.10	0.11	ns
GTL Plus	GTLP	T_{OGTLP}	0.04	0.05	0.06	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.56	0.64	0.70	ns

Date	Version	Revision
11/17/04	4.1	• Figure 8, Figure 9: Corrected T_{CCO} / DOUT to refer to the falling edge of CCLK. • Table 23: Added Footnote (4) to T_{PHASE} indicating an 8B/10B-type bitstream. Corrected T_{LOCK} from Typ to Max specification. Additional description of "2X oversampling" added to half-rate operation condition for F_{GCLK}, and added Footnote (2) requiring use of oversampling techniques in XAPP572 for serial bit rates under 1 Gb/s. • Table 25: Converted bit rate conditions for jitter parameters into four ranges. Added Footnote (2) requiring use of oversampling techniques in XAPP572 for serial bit rates under 1 Gb/s. • Table 27: Additional description of "2X oversampling" added to half-speed clock description for F_{GGTX}. Converted bit rate conditions for jitter parameters into four ranges. Added Footnotes (3) and (4) requiring use of oversampling techniques in XAPP572 for serial bit rates under 1 Gb/s. • Table 40: Changed capacitance C_{REF} for all PCI/PCI-X standards from 0 pF to 10 pF. • Table 49: Added Min/Max specifications for T_{ICCK}. • Section Power-On Power Supply Requirements, page 5: Added word "monotonically" to description of V_{CCINT} ramp-on requirements. Removed requirement that V_{CCAUX} must be powered on before or with V_{CCO}.
03/01/05	4.2	• Updated values in Virtex-II Pro Performance Characteristics and Virtex-II Pro Switching Characteristics tables, based on values extracted from **speedsfile version 1.90**. • Table 1 and Table 2: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 3: Further clarified P_{RXTX} (MGT power dissipation) by explaining measurement method in Footnote (3). • Table 5: Added power-on current specifications for XC2VPX70 device. • Table 22: Changed F_{GTOL} from ±100 ppm to ±350 ppm. • Table 22 and Table 23: Changed T_{GJTT} bit rate qualifiers from fixed bit rates to bit rate ranges. • Table 36, Table 38, Table 39, and Table 40: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in the Xilinx ICE™ software) for all I/O standards. • Table 36: Rearranged I/O standards in a more logical order. • Table 37: Added parameter T_{RPW} (Minimum Pulse Width, SR Input). • Table 38: Changed "Csl" to "C_{REF}" to agree with Figure 6 and Table 40. Rearranged I/O standards in a more logical order. • Table 39: Added footnote defining equivalents for DCI standards. • Table 40: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load (C_{REF}) values. • Table 47: Added parameter T_{BCCS}, CLKA to CLKB Setup Time. • Table 50: Added Footnote (1) indicating that F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$ if CCLK frequency is not adjustable. • Table 52: T_{TCKTDO} corrected from a "Min" to a "Max" specification.
06/20/05	4.3	• Table 12: Added specifications for Differential Input Impedance.

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 5, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/BUSY/DOUT(1)	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0/DIN(1)	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L88N_7/VREF_7	L5			
7	IO_L86P_7	L6			
7	IO_L86N_7	K6			
7	IO_L85P_7	K1			
7	IO_L85N_7	K2			
7	IO_L60P_7	K3	NC		
7	IO_L60N_7	K4	NC		
7	IO_L58P_7	K5	NC		
7	IO_L58N_7/VREF_7	J5	NC		
7	IO_L56P_7	J1	NC		
7	IO_L56N_7	J2	NC		
7	IO_L55P_7	J3	NC		
7	IO_L55N_7	J4	NC		
7	IO_L54P_7	J6	NC		
7	IO_L54N_7	H5	NC		
7	IO_L52P_7	H1	NC		
7	IO_L52N_7/VREF_7	H2	NC		
7	IO_L50P_7	H3	NC		
7	IO_L50N_7	H4	NC		
7	IO_L49P_7	G1	NC		
7	IO_L49N_7	G2	NC		
7	IO_L48P_7	G3	NC		
7	IO_L48N_7	G4	NC		
7	IO_L46P_7	G5	NC		
7	IO_L46N_7/VREF_7	F5	NC		
7	IO_L43P_7	F1	NC		
7	IO_L43N_7	F2	NC		
7	IO_L06P_7	F3			
7	IO_L06N_7	F4			
7	IO_L04P_7	E1			
7	IO_L04N_7/VREF_7	E2			
7	IO_L03P_7	E3			
7	IO_L03N_7	E4			
7	IO_L02P_7	D1			
7	IO_L02N_7	D2			
7	IO_L01P_7/VRN_7	C1			
7	IO_L01N_7/VRP_7	C2			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VCCINT	U10			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U17			
N/A	VCCINT	U20			
N/A	VCCINT	V9			
N/A	VCCINT	V18			
N/A	VCCINT	Y10			
N/A	VCCINT	Y13			
N/A	VCCINT	Y14			
N/A	VCCINT	Y17			
N/A	VCCAUX	A2			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	A25			
N/A	VCCAUX	N1			
N/A	VCCAUX	N26			
N/A	VCCAUX	P1			
N/A	VCCAUX	P26			
N/A	VCCAUX	AF2			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	VCCAUX	AF25			
N/A	GND	A1			
N/A	GND	A26			
N/A	GND	B2			
N/A	GND	B25			
N/A	GND	C3			
N/A	GND	C24			
N/A	GND	D4			
N/A	GND	D8			
N/A	GND	D19			
N/A	GND	D23			
N/A	GND	F10			
N/A	GND	F17			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	VCCO_1		K13			
1	VCCO_1		K12			
1	VCCO_1		K11			
1	VCCO_1		K10			
1	VCCO_1		J13			
1	VCCO_1		J12			
1	VCCO_1		J11			
1	VCCO_1		J10			
2	VCCO_2		R10			
2	VCCO_2		P10			
2	VCCO_2		N10			
2	VCCO_2		N9			
2	VCCO_2		M10			
2	VCCO_2		M9			
2	VCCO_2		L10			
2	VCCO_2		L9			
2	VCCO_2		K9			
2	VCCO_2		J9			
3	VCCO_3		AB9			
3	VCCO_3		AA9			
3	VCCO_3		Y10			
3	VCCO_3		Y9			
3	VCCO_3		W10			
3	VCCO_3		W9			
3	VCCO_3		V10			
3	VCCO_3		V9			
3	VCCO_3		U10			
3	VCCO_3		T10			
4	VCCO_4		AB13			
4	VCCO_4		AB12			
4	VCCO_4		AB11			
4	VCCO_4		AB10			
4	VCCO_4		AA15			
4	VCCO_4		AA14			
4	VCCO_4		AA13			
4	VCCO_4		AA12			

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L36N_3	AE4		
3	IO_L36P_3	AF4		
3	IO_L35N_3	AC10		
3	IO_L35P_3	AD10		
3	IO_L34N_3	AE1		
3	IO_L34P_3	AE2		
3	IO_L33N_3/VREF_3	AF6		
3	IO_L33P_3	AF7		
3	IO_L32N_3	AC8		
3	IO_L32P_3	AC9		
3	IO_L31N_3	AF2		
3	IO_L31P_3	AF3		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AG6		
3	IO_L29N_3	AD9		
3	IO_L29P_3	AE9		
3	IO_L28N_3	AG4		
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AG2		
3	IO_L27P_3	AG3		
3	IO_L26N_3	AD7		
3	IO_L26P_3	AE7		
3	IO_L25N_3	AH6		
3	IO_L25P_3	AH7		
3	IO_L24N_3	AH5		
3	IO_L24P_3	AJ5		
3	IO_L23N_3	AE8		
3	IO_L23P_3	AF8		
3	IO_L22N_3	AH1		
3	IO_L22P_3	AH2		
3	IO_L21N_3/VREF_3	AJ6		
3	IO_L21P_3	AK6		
3	IO_L20N_3	AG7		
3	IO_L20P_3	AG8		
3	IO_L19N_3	AJ3		
3	IO_L19P_3	AJ4		
3	IO_L18N_3	AJ1		
3	IO_L18P_3	AJ2		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
4	IO_L47N_4	AE15		
4	IO_L47P_4	AD15		
4	IO_L48N_4	AM14		
4	IO_L48P_4	AL14		
4	IO_L49N_4	AP14		
4	IO_L49P_4	AN14		
4	IO_L50_4/No_Pair	AH15		
4	IO_L53_4/No_Pair	AG16		
4	IO_L54N_4	AK15		
4	IO_L54P_4	AJ15		
4	IO_L55N_4	AM15		
4	IO_L55P_4	AL16		
4	IO_L56N_4	AE16		
4	IO_L56P_4	AD16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AN15		
4	IO_L66N_4	AJ16	NC	
4	IO_L66P_4/VREF_4	AH16	NC	
4	IO_L67N_4	AN16		
4	IO_L67P_4	AM16		
4	IO_L68N_4	AG17		
4	IO_L68P_4	AF17		
4	IO_L69N_4	AJ17		
4	IO_L69P_4/VREF_4	AH17		
4	IO_L73N_4	AL17		
4	IO_L73P_4	AK17		
4	IO_L74N_4/GCLK3S	AE17		
4	IO_L74P_4/GCLK2P	AD17		
4	IO_L75N_4/GCLK1S	AN17		
4	IO_L75P_4/GCLK0P	AM17		
5	IO_L75N_5/GCLK7S	AM18		
5	IO_L75P_5/GCLK6P	AN18		
5	IO_L74N_5/GCLK5S	AD18		
5	IO_L74P_5/GCLK4P	AE18		
5	IO_L73N_5	AK18		
5	IO_L73P_5	AL18		
5	IO_L69N_5/VREF_5	AH18		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L43N_7	R37		
7	IO_L42P_7	R34		
7	IO_L42N_7	R35		
7	IO_L41P_7	U28		
7	IO_L41N_7	T28		
7	IO_L40P_7	R32		
7	IO_L40N_7/VREF_7	R33		
7	IO_L39P_7	P38		
7	IO_L39N_7	P39		
7	IO_L38P_7	T29		
7	IO_L38N_7	T30		
7	IO_L37P_7	N37		
7	IO_L37N_7	P37		
7	IO_L36P_7	P35		
7	IO_L36N_7	P36		
7	IO_L35P_7	T27		
7	IO_L35N_7	R27		
7	IO_L34P_7	P33		
7	IO_L34N_7/VREF_7	P34		
7	IO_L33P_7	N38		
7	IO_L33N_7	N39		
7	IO_L32P_7	R28		
7	IO_L32N_7	R29		
7	IO_L31P_7	N35		
7	IO_L31N_7	M36		
7	IO_L30P_7	N33		
7	IO_L30N_7	N34		
7	IO_L29P_7	R30		
7	IO_L29N_7	R31		
7	IO_L28P_7	M37		
7	IO_L28N_7/VREF_7	M38		
7	IO_L27P_7	M33		
7	IO_L27N_7	M34		
7	IO_L26P_7	P28		
7	IO_L26N_7	P29		
7	IO_L25P_7	L38		
7	IO_L25N_7	L39		
7	IO_L24P_7	L36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	TXNPAD11	A7		
N/A	TXPPAD11	A6		
N/A	GNDA11	C6		
N/A	RXPPAD11	A5		
N/A	RXNPAD11	A4		
N/A	VTRXPAD11	B5		
N/A	AVCCAUXRX11	B4		
N/A	AVCCAUXRX14	AV4		
N/A	VTRXPAD14	AV5		
N/A	RXNPAD14	AW4		
N/A	RXPPAD14	AW5		
N/A	GNDA14	AU6		
N/A	TXPPAD14	AW6		
N/A	TXNPAD14	AW7		
N/A	VTTXPAD14	AV7		
N/A	AVCCAUXTX14	AV6		
N/A	AVCCAUXRX16	AV8		
N/A	VTRXPAD16	AV9		
N/A	RXNPAD16	AW8		
N/A	RXPPAD16	AW9		
N/A	GNDA16	AU9		
N/A	TXPPAD16	AW10		
N/A	TXNPAD16	AW11		
N/A	VTTXPAD16	AV11		
N/A	AVCCAUXTX16	AV10		
N/A	AVCCAUXRX17	AV12		
N/A	VTRXPAD17	AV13		
N/A	RXNPAD17	AW12		
N/A	RXPPAD17	AW13		
N/A	GNDA17	AU13		
N/A	TXPPAD17	AW14		
N/A	TXNPAD17	AW15		
N/A	VTTXPAD17	AV15		
N/A	AVCCAUXTX17	AV14		
N/A	AVCCAUXRX18	AV16		
N/A	VTRXPAD18	AV17		
N/A	RXNPAD18	AW16		
N/A	RXPPAD18	AW17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L75N_1/GCLK3P		G21		
1	IO_L75P_1/GCLK2S		F21		
1	IO_L74N_1/GCLK1P		J21		
1	IO_L74P_1/GCLK0S		K21		
1	IO_L73N_1		D20		
1	IO_L73P_1		C20		
1	IO_L69N_1/VREF_1		F20		
1	IO_L69P_1		E20		
1	IO_L68N_1		H20		
1	IO_L68P_1		J20		
1	IO_L67N_1		L20		
1	IO_L67P_1		K20		
1	IO_L66N_1/VREF_1		M20		
1	IO_L66P_1		M21		
1	IO_L65N_1		C19		
1	IO_L65P_1		D19		
1	IO_L64N_1		F19		
1	IO_L64P_1		E19		
1	IO_L60N_1		H19		
1	IO_L60P_1		G19		
1	IO_L59N_1		K19		
1	IO_L59P_1		J19		
1	IO_L58N_1		M19		
1	IO_L58P_1		L19		
1	IO_L57N_1/VREF_1		C17		
1	IO_L57P_1		C18		
1	IO_L56N_1		E18		
1	IO_L56P_1		E17		
1	IO_L55N_1		H18		
1	IO_L55P_1		G18		
1	IO_L54N_1		L18		
1	IO_L54P_1		K18		
1	IO_L53_1/No_Pair		D17		
1	IO_L50_1/No_Pair		D16		
1	IO_L49N_1		G17		
1	IO_L49P_1		F17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L53N_3		AE10		
3	IO_L53P_3		AE11		
3	IO_L52N_3		AE1		
3	IO_L52P_3		AE2		
3	IO_L51N_3/VREF_3		AE4		
3	IO_L51P_3		AE5		
3	IO_L50N_3		AF11		
3	IO_L50P_3		AE12		
3	IO_L49N_3		AE7		
3	IO_L49P_3		AE8		
3	IO_L48N_3		AF1		
3	IO_L48P_3		AF2		
3	IO_L47N_3		AG12		
3	IO_L47P_3		AF12		
3	IO_L46N_3		AF3		
3	IO_L46P_3		AF4		
3	IO_L45N_3/VREF_3		AF5		
3	IO_L45P_3		AF6		
3	IO_L44N_3		AF7		
3	IO_L44P_3		AF8		
3	IO_L43N_3		AF9		
3	IO_L43P_3		AF10		
3	IO_L42N_3		AG2		
3	IO_L42P_3		AG3		
3	IO_L41N_3		AG10		
3	IO_L41P_3		AG11		
3	IO_L40N_3		AG4		
3	IO_L40P_3		AG5		
3	IO_L39N_3/VREF_3		AG6		
3	IO_L39P_3		AG7		
3	IO_L38N_3		AG8		
3	IO_L38P_3		AH8		
3	IO_L37N_3		AH1		
3	IO_L37P_3		AH2		
3	IO_L36N_3		AH3		
3	IO_L36P_3		AJ3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L87P_7	AA37	
7	IO_L87N_7	AA38	
7	IO_L86P_7	AA33	
7	IO_L86N_7	AA34	
7	IO_L85P_7	Y40	
7	IO_L85N_7	Y41	
7	IO_L60P_7	W41	
7	IO_L60N_7	W42	
7	IO_L59P_7	AA31	
7	IO_L59N_7	AA32	
7	IO_L58P_7	V40	
7	IO_L58N_7/VREF_7	W40	
7	IO_L57P_7	W37	
7	IO_L57N_7	W38	
7	IO_L56P_7	Y36	
7	IO_L56N_7	Y37	
7	IO_L55P_7	V41	
7	IO_L55N_7	V42	
7	IO_L54P_7	V38	
7	IO_L54N_7	V39	
7	IO_L53P_7	Y31	
7	IO_L53N_7	Y32	
7	IO_L52P_7	U40	
7	IO_L52N_7/VREF_7	U41	
7	IO_L51P_7	T40	
7	IO_L51N_7	U39	
7	IO_L50P_7	Y35	
7	IO_L50N_7	W36	
7	IO_L49P_7	T37	
7	IO_L49N_7	U37	
7	IO_L48P_7	T41	
7	IO_L48N_7	T42	
7	IO_L47P_7	Y33	
7	IO_L47N_7	W34	
7	IO_L46P_7	T38	
7	IO_L46N_7/VREF_7	T39	
7	IO_L45P_7	R36	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	