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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	996
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-5ff1704c

- HyperTransport (LDT) I/O with current driver buffers
- Built-in DDR input and output registers
- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13 µm Nine-Layer Copper Process with 90 nm High-Speed Transistors
- 1.5V (V_{CCINT}) core power supply, dedicated 2.5V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Standard 1.00 mm Pitch.
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- Each Device 100% Factory Tested

General Description

The Virtex-II Pro and Virtex-II Pro X families contain platform FPGAs for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU blocks in Virtex-II Pro Series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13 µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gate arrays.

Architecture

Array Overview

Virtex-II Pro and Virtex-II Pro X devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high-density and high-performance system designs. Virtex-II Pro devices implement the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel (RocketIO) or 6.25 Gb/s (RocketIO X).
- Embedded IBM PowerPC 405 RISC processor blocks provide performance up to 400 MHz.
- SelectIO-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM+ memory modules provide large 18 Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and supports high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Features

This section briefly describes Virtex-II Pro / Virtex-II Pro X features. For more details, refer to Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description.

RocketIO / RocketIO X MGT Cores

The RocketIO and RocketIO X Multi-Gigabit Transceivers are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 100 Gb/s (RocketIO) or 170 Gb/s (RocketIO X) of full-duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s (RocketIO) or 6.25 Gb/s (RocketIO X).

Each RocketIO or RocketIO X core implements the following technology:

- Serializer and deserializer (SERDES)
- Monolithic clock synthesis and clock recovery (CDR)
- 10 Gigabit Attachment Unit Interface (XAUI) Fibre Channel (3.1875 Gb/s XAUI), Infiniband, PCI Express, Aurora, SXI-5 (SFI-5,/SPI-5), and OC-48 compatibility(1)
- 8/16/32-bit (RocketIO) or 8/16/32/64-bit (RocketIO X) selectable FPGA interface
- 8B/10B (RocketIO) or 8B/10B and 64B/66B (RocketIO X) encoder and decoder with bypassing option on each channel
- Channel bonding support (two to twenty channels)
  - Elastic buffers for inter-chip deskewing and channel-to-channel alignment
- Receiver clock recovery tolerance of up to 75 non-transitioning bits
- 50Ω (RocketIO X) or 50Ω /75Ω selectable (RocketIO) on-chip transmit and receive terminations
- Programmable comma detection and word alignment
- Rate matching via insertion/deletion characters
- Automatic lock-to-reference function
- Programmable pre-emphasis support
- Per-channel serial and parallel transmitter-to-receiver internal loopback modes
- Optional transmit and receive data inversion
- Cyclic Redundancy Check support (RocketIO only)

PowerPC 405 Processor Block

The PPC405 RISC CPU can execute instructions at a sustained rate of one instruction per cycle. On-chip instruction and data cache reduce design complexity and improve system throughput.

The PPC405 features include:

- PowerPC RISC CPU
  - Implements the PowerPC User Instruction Set Architecture (UISA) and extensions for embedded applications
  - Thirty-two 32-bit general purpose registers (GPRs)
  - Static branch prediction
  - Five-stage pipeline with single-cycle execution of most instructions, including loads/stores
  - Unaligned and aligned load/store support to cache, main memory, and on-chip memory
  - Hardware multiply/divide for faster integer arithmetic (4-cycle multiply, 35-cycle divide)
  - Enhanced string and multiple-word handling
  - Big/little endian operation support
- Storage Control
  - Separate instruction and data cache units, both two-way set-associative and non-blocking
  - Eight words (32 bytes) per cache line
  - 16 KB array Instruction Cache Unit (ICU), 16 KB array Data Cache Unit (DCU)
  - Operand forwarding during instruction cache line fill
  - Copy-back or write-through DCU strategy
  - Doubleword instruction fetch from cache improves branch latency
- Virtual mode memory management unit (MMU)
  - Translation of the 4 GB logical address space into physical addresses
  - Software control of page replacement strategy
  - Supports multiple simultaneous page sizes ranging from 1 KB to 16 MB
- OCM controllers provide dedicated interfaces between Block SelectRAM+ memory and processor block instruction and data paths for high-speed access
- PowerPC timer facilities
  - 64-bit time base
  - Programmable interval timer (PIT)
  - Fixed interval timer (FIT)
  - Watchdog timer (WDT)
- Debug Support
  - Internal debug mode
  - External debug mode
  - Debug Wait mode
  - Real Time Trace debug mode
  - Enhanced debug support with logical operators
  - Instruction trace and trace-back support
  - Forward or backward trace
- Two hardware interrupt levels support
- Advanced power management support

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register and an optional 3-state buffer to be driven directly or through an SDR or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V,(2) 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V(3)
- PCI compliant (66 MHz and 33 MHz) at 3.3V(3)
- GTL and GTLP

1. Refer to Table 4, Module 2 for detailed information about RocketIO and RocketIO X transceiver compatible protocols.
2. Refer to XAPP659 for more information.
3. Refer to XAPP653 for more information.

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

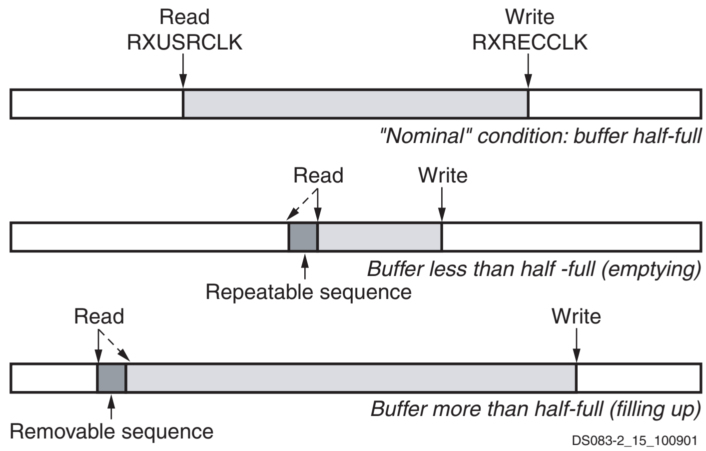


Figure 12: **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

Table 9: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LDT_25	2.5	N/R	N/R	0.500 – 0.740
LVDS_25	2.5	N/R	N/R	0.247 – 0.454
LVDSEXT_25	2.5	N/R	N/R	0.440 – 0.820
BLVDS_25	2.5	N/R	N/R	0.250 – 0.450
ULVDS_25	2.5	N/R	N/R	0.500 – 0.740
LVPECL_25	2.5	N/R	N/R	0.345 – 1.185
LDT_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740
LVDS_25_DT(1)	2.5	2.5	N/R	0.247 – 0.454
LVDSEXT_25_DT(1)	2.5	2.5	N/R	0.330 – 0.700
ULVDS_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740

Notes:
1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

Table 10: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R	Series
LVDCI_25	2.5	2.5	N/R	Series
LVDCI_DV2_25	2.5	2.5	N/R	Series
LVDCI_18	1.8	1.8	N/R	Series
LVDCI_DV2_18	1.8	1.8	N/R	Series
LVDCI_15	1.5	1.5	N/R	Series
LVDCI_DV2_15	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL18_I_DCI(3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split

Table 10: **Supported DCI I/O Standards *(Continued)***

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

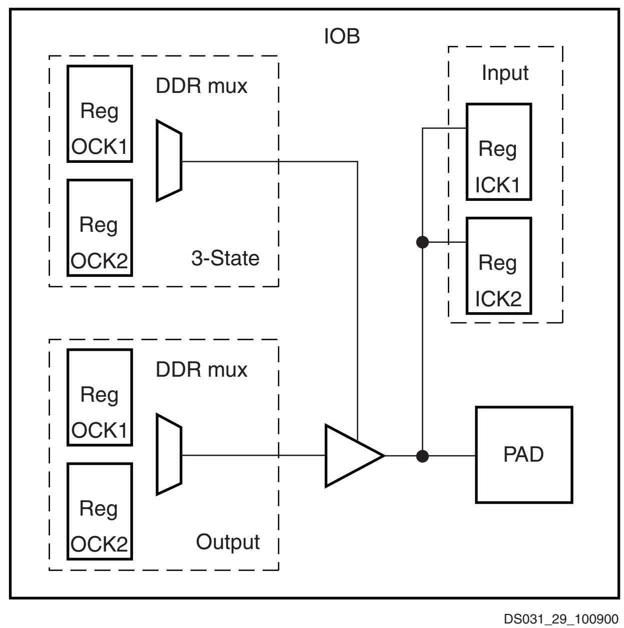


Figure 19: **Virtex-II Pro IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

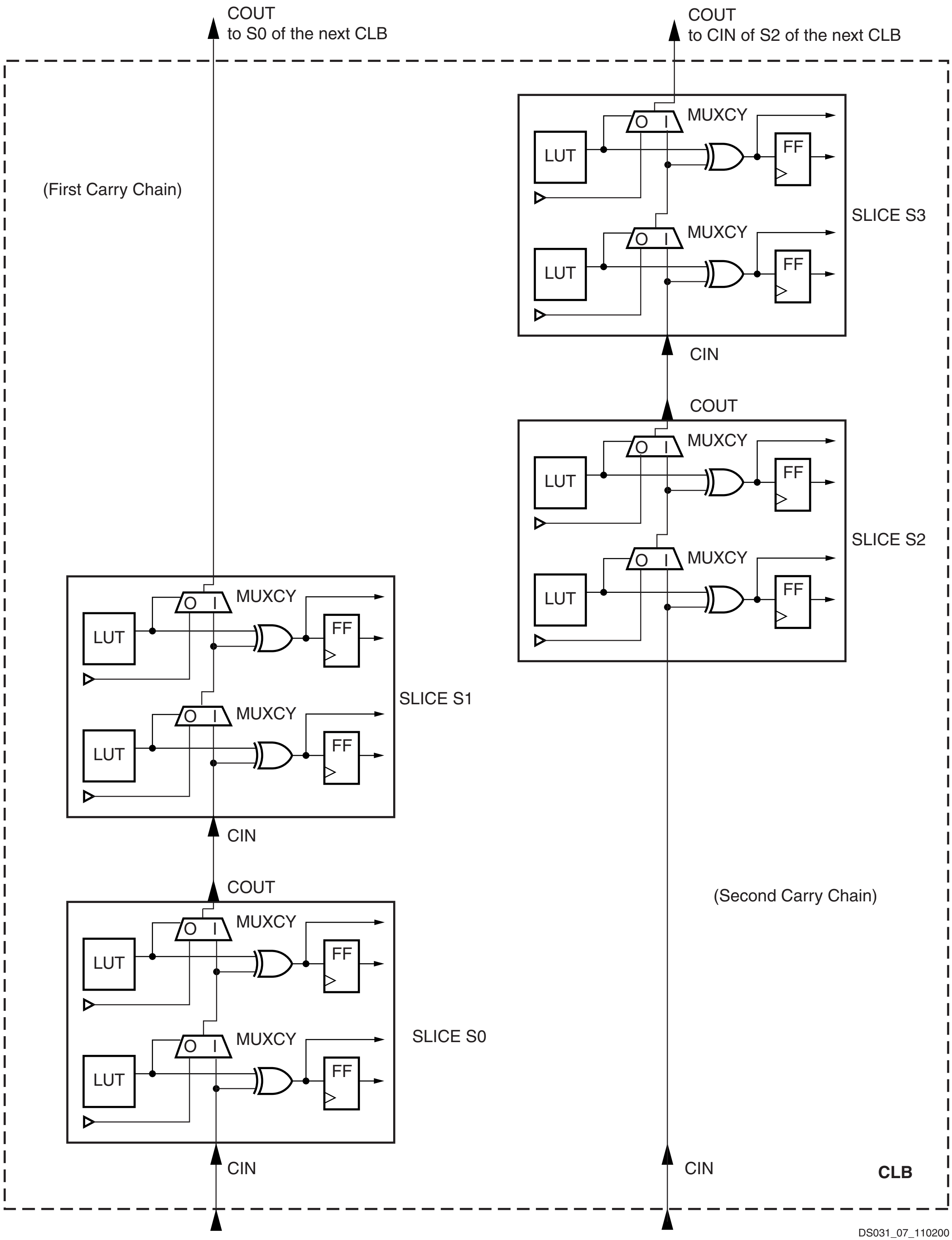


Figure 42: **Fast Carry Logic Path**

nally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II Pro block SelectRAM+ memory to advantage.

Each block SelectRAM+ cell is a fully synchronous memory as illustrated in Figure 47. Input data bus and output data bus widths are identical.

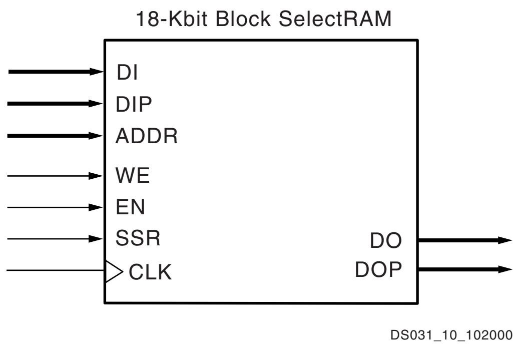


Figure 47: **18 Kb Block SelectRAM+ Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM+ has access to a common 18 Kb memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 22 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kb block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kb memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbs.

Table 22: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

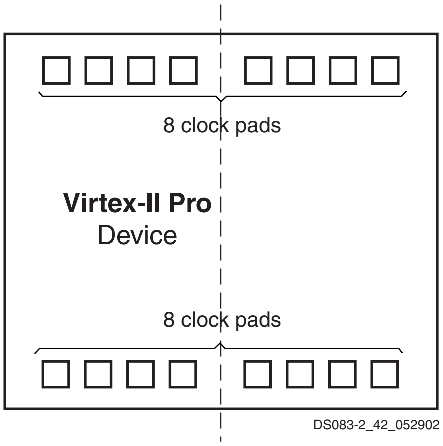


Figure 55: **Virtex-II Pro Clock Pads**

Each global clock multiplexer buffer can be driven either by the clock pad to distribute a clock directly to the device, or by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 51. Each global clock multiplexer buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock multiplexer buffer inputs, as shown in Figure 56.

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM+ blocks.

Eight global clocks can be used in each quadrant of the Virtex-II Pro device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning. (See the *Virtex-II Pro Platform FPGA User Guide*.)

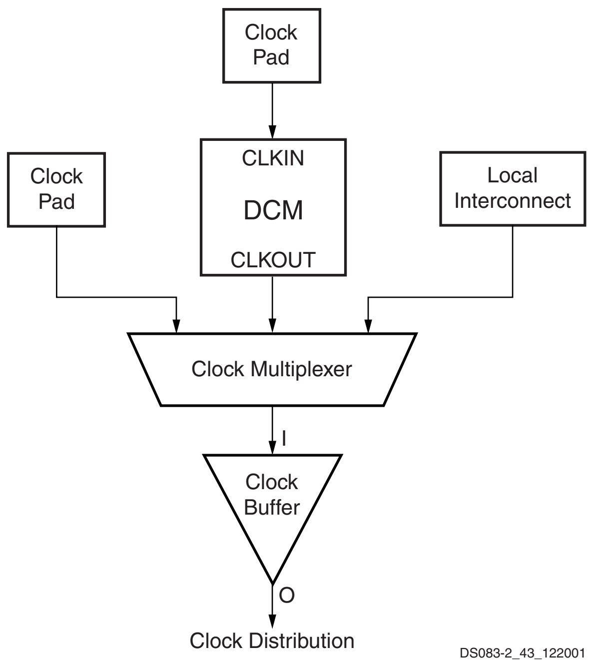


Figure 56: **Virtex-II Pro Clock Multiplexer Buffer Configuration**

Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as Virtex-II Pro Switching Characteristics (speed files).

Table 13 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 13: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin Performance (with I/O Delays)	Units
Basic Functions:			
16-bit Address Decoder	XC2VP20FF1152-6	7.20	ns
32-bit Address Decoder	XC2VP20FF1152-6	8.08	ns
64-bit Address Decoder	XC2VP20FF1152-6	8.15	ns
4:1 MUX	XC2VP20FF1152-6	3.85	ns
8:1 MUX	XC2VP20FF1152-6	7.24	ns
16:1 MUX	XC2VP20FF1152-6	7.30	ns
32:1 MUX	XC2VP20FF1152-6	7.64	ns
Combinatorial (pad to LUT to pad)	XC2VP20FF1152-6	3.26	ns
Memory:			
Block RAM			
Pad to setup	XC2VP20FF1152-6	1.72	ns
Clock to Pad	XC2VP20FF1152-6	6.63	ns
Distributed RAM			
Pad to setup	XC2VP20FF1152-6	1.78	ns
Clock to Pad	XC2VP20FF1152-6	4.12	ns

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
1	IO_L02N_1	C13
1	IO_L02P_1	B14
1	IO_L01N_1/VRP_1	C14
1	IO_L01P_1/VRN_1	C15
2	IO_L01N_2/VRP_2	E14
2	IO_L01P_2/VRN_2	E15
2	IO_L02N_2	E13
2	IO_L02P_2	F12
2	IO_L03N_2	F13
2	IO_L03P_2	F14
2	IO_L04N_2/VREF_2	F15
2	IO_L04P_2	F16
2	IO_L06N_2	G13
2	IO_L06P_2	G14
2	IO_L85N_2	G15
2	IO_L85P_2	G16
2	IO_L86N_2	G12
2	IO_L86P_2	H13
2	IO_L88N_2/VREF_2	H14
2	IO_L88P_2	H15
2	IO_L90N_2	H16
2	IO_L90P_2	J16
3	IO_L90N_3	J15
3	IO_L90P_3	J14
3	IO_L89N_3	J13
3	IO_L89P_3	K12
3	IO_L87N_3/VREF_3	K16
3	IO_L87P_3	K15
3	IO_L85N_3	K14
3	IO_L85P_3	K13
3	IO_L06N_3	L16
3	IO_L06P_3	L15
3	IO_L05N_3	L14

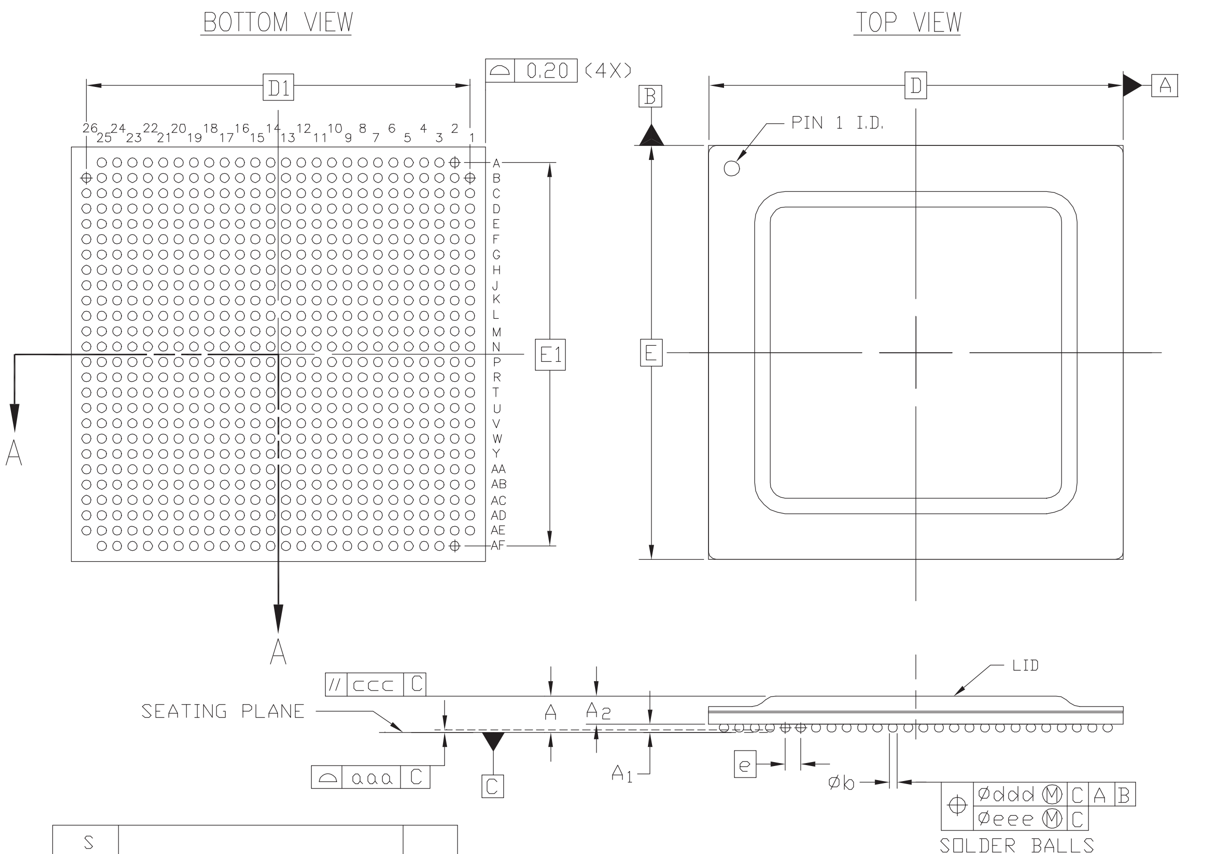
Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			

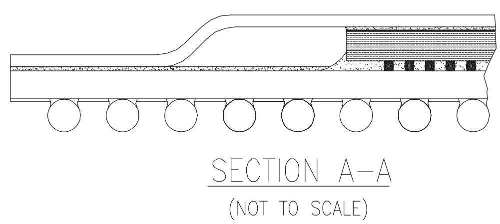
Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			

FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	–	2.45	2.65	
A_1	0.40	0.50	0.60	
A_2	–	–	2.15	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	–	–	0.20	
ccc	–	–	0.35	
ddd	–	–	0.30	
eee	–	–	0.10	
M	26			2



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

Figure 4: **FF672 Flip-Chip Fine-Pitch BGA Package Specifications**

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 9, XC2VP7, XC2VP20, and XC2VP30 Virtex-II Pro devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		N17			
N/A	GND		N16			
N/A	GND		N15			
N/A	GND		N14			
N/A	GND		N13			
N/A	GND		N12			
N/A	GND		M19			
N/A	GND		M18			
N/A	GND		M17			
N/A	GND		M16			
N/A	GND		M15			
N/A	GND		M14			
N/A	GND		M13			
N/A	GND		M12			
N/A	GND		L28			
N/A	GND		L25			
N/A	GND		L20			
N/A	GND		L11			
N/A	GND		L6			
N/A	GND		L3			
N/A	GND		H30			
N/A	GND		H1			
N/A	GND		F25			
N/A	GND		F18			
N/A	GND		F13			
N/A	GND		F6			
N/A	GND		E26			
N/A	GND		E5			
N/A	GND		D27			
N/A	GND		D22			
N/A	GND		D19			
N/A	GND		D12			
N/A	GND		D9			
N/A	GND		D4			
N/A	GND		C28			
N/A	GND		C17			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L57N_2	R4				
2	IO_L57P_2	R3				
2	IO_L58N_2/VREF_2	R2				
2	IO_L58P_2	T2				
2	IO_L59N_2	T8				
2	IO_L59P_2	T7				
2	IO_L60N_2	T6				
2	IO_L60P_2	T5				
2	IO_L85N_2	T4				
2	IO_L85P_2	T3				
2	IO_L86N_2	U10				
2	IO_L86P_2	U9				
2	IO_L87N_2	U6				
2	IO_L87P_2	U5				
2	IO_L88N_2/VREF_2	U2				
2	IO_L88P_2	V2				
2	IO_L89N_2	U8				
2	IO_L89P_2	U7				
2	IO_L90N_2	U4				
2	IO_L90P_2	U3				
3	IO_L90N_3	V3				
3	IO_L90P_3	V4				
3	IO_L89N_3	V7				
3	IO_L89P_3	V8				
3	IO_L88N_3	V5				
3	IO_L88P_3	V6				
3	IO_L87N_3/VREF_3	W2				
3	IO_L87P_3	Y2				
3	IO_L86N_3	V9				
3	IO_L86P_3	V10				
3	IO_L85N_3	W3				
3	IO_L85P_3	W4				
3	IO_L60N_3	Y1				
3	IO_L60P_3	AA1				
3	IO_L59N_3	V11				
3	IO_L59P_3	W11				
3	IO_L58N_3	W5				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L73P_4	AG17				
4	IO_L74N_4/GCLK3S	AH17				
4	IO_L74P_4/GCLK2P	AJ17				
4	IO_L75N_4/GCLK1S	AK17				
4	IO_L75P_4/GCLK0P	AL17				
5	IO_L75N_5/GCLK7S	AL18				
5	IO_L75P_5/GCLK6P	AK18				
5	IO_L74N_5/GCLK5S	AJ18				
5	IO_L74P_5/GCLK4P	AH18				
5	IO_L73N_5	AG18				
5	IO_L73P_5	AF18				
5	IO_L69N_5/VREF_5	AL19				
5	IO_L69P_5	AK19				
5	IO_L68N_5	AJ19				
5	IO_L68P_5	AH19				
5	IO_L67N_5	AE18				
5	IO_L67P_5	AD18				
5	IO_L57N_5/VREF_5	AL20				
5	IO_L57P_5	AL21				
5	IO_L56N_5	AJ20				
5	IO_L56P_5	AH20				
5	IO_L55N_5	AG19				
5	IO_L55P_5	AF19				
5	IO_L54N_5	AM22				
5	IO_L54P_5	AM21				
5	IO_L53_5/No_Pair	AK21				
5	IO_L50_5/No_Pair	AJ21				
5	IO_L49N_5	AE19				
5	IO_L49P_5	AD19				
5	IO_L48N_5	AL23				
5	IO_L48P_5	AL22				
5	IO_L47N_5	AH21				
5	IO_L47P_5	AG21				
5	IO_L46N_5	AF20				
5	IO_L46P_5	AE20				
5	IO_L45N_5/VREF_5	AM24				
5	IO_L45P_5	AL24				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L53P_6	W25				
6	IO_L53N_6	W26				
6	IO_L54P_6	AB33				
6	IO_L54N_6	AA33				
6	IO_L55P_6	Y28				
6	IO_L55N_6	Y29				
6	IO_L56P_6	W27				
6	IO_L56N_6	W28				
6	IO_L57P_6	Y31				
6	IO_L57N_6/VREF_6	Y32				
6	IO_L58P_6	W29				
6	IO_L58N_6	W30				
6	IO_L59P_6	W24				
6	IO_L59N_6	V24				
6	IO_L60P_6	AA34				
6	IO_L60N_6	Y34				
6	IO_L85P_6	W31				
6	IO_L85N_6	W32				
6	IO_L86P_6	V25				
6	IO_L86N_6	V26				
6	IO_L87P_6	Y33				
6	IO_L87N_6/VREF_6	W33				
6	IO_L88P_6	V29				
6	IO_L88N_6	V30				
6	IO_L89P_6	V27				
6	IO_L89N_6	V28				
6	IO_L90P_6	V31				
6	IO_L90N_6	V32				
7	IO_L90P_7	U32				
7	IO_L90N_7	U31				
7	IO_L89P_7	U28				
7	IO_L89N_7	U27				
7	IO_L88P_7	V33				
7	IO_L88N_7/VREF_7	U33				
7	IO_L87P_7	U30				
7	IO_L87N_7	U29				
7	IO_L86P_7	U26				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	VCCO_1	H15		
1	VCCO_1	D15		
1	VCCO_1	M14		
1	VCCO_1	M13		
1	VCCO_1	L12		
1	VCCO_1	H11		
1	VCCO_1	D11		
0	VCCO_0	H24		
0	VCCO_0	D24		
0	VCCO_0	L23		
0	VCCO_0	M22		
0	VCCO_0	M21		
0	VCCO_0	M20		
0	VCCO_0	H20		
0	VCCO_0	D20		
0	VCCO_0	M19		
0	VCCO_0	M18		
N/A	CCLK	AG9		
N/A	PROG_B	G26		
N/A	DONE	AF10		
N/A	M0	AG25		
N/A	M1	AG26		
N/A	M2	AF25		
N/A	TCK	G9		
N/A	TDI	F26		
N/A	TDO	F9		
N/A	TMS	H10		
N/A	PWRDWN_B	AG10		
N/A	HSWAP_EN	H25		
N/A	RSVD	H9		
N/A	VBATT	J10		
N/A	DXP	J25		
N/A	DXN	H26		
N/A	VCCINT	AD24		
N/A	VCCINT	L24		
N/A	VCCINT	AC23		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L64N_5		AU24		
5	IO_L64P_5		AV24		
5	IO_L60N_5		AR24		
5	IO_L60P_5		AT24		
5	IO_L59N_5		AN24		
5	IO_L59P_5		AP24		
5	IO_L58N_5		AL24		
5	IO_L58P_5		AM24		
5	IO_L57N_5/VREF_5		AY26		
5	IO_L57P_5		AY25		
5	IO_L56N_5		AV25		
5	IO_L56P_5		AV26		
5	IO_L55N_5		AR25		
5	IO_L55P_5		AT25		
5	IO_L54N_5		AM25		
5	IO_L54P_5		AN25		
5	IO_L53_5/No_Pair		AW26		
5	IO_L50_5/No_Pair		AW27		
5	IO_L49N_5		AT26		
5	IO_L49P_5		AU26		
5	IO_L48N_5		AP26		
5	IO_L48P_5		AR26		
5	IO_L47N_5		AN26		
5	IO_L47P_5		AM26		
5	IO_L46N_5		AL26		
5	IO_L46P_5		AL25		
5	IO_L45N_5/VREF_5		AU27		
5	IO_L45P_5		AV27		
5	IO_L44N_5		AT27		
5	IO_L44P_5		AR27		
5	IO_L43N_5		AN27		
5	IO_L43P_5		AP27		
5	IO_L39N_5		AL27		
5	IO_L39P_5		AM27		
5	IO_L38N_5		AY28		
5	IO_L38P_5		AY29		

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
08/14/02	2.0	Added package and pinout information for new devices.
08/27/02	2.1	• Updated SelectIO-Ultra information in Table 4. (Table deleted in v2.3.) • Corrected direction for RXNPAD and TXPPAD in Table 4 (formerly Table 5).
09/27/02	2.2	Corrected Table 2 and Table 3 entries for XC2VP30, FF1152 package, maximum I/Os from 692 to 644.
11/20/02	2.3	Added Number of Differential Pairs data to Table 3. Removed former Table 4.
12/03/02	2.4	Corrections in Table 4: • Reclassified GCLKx (S/P) pins as Input/Output, since these pins can be used as normal I/Os if not used as clocks. • Added cautionary note to PWRDWN_B pin, indicating that this function is not supported.
01/20/03	2.5	Added and removed package/pinout information for existing devices: • In Table 1, added FG676 package information. • In Table 3, added FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • In Table 12, removed FF1517 package option for XC2VP40. • Added FG676 package pinouts (Table 7) for XC2VP20, XC2VP30, and XC2VP40. • Added package diagram (Figure 3) for FG676 package.
05/19/03	2.5.1	• Added section **BREFCLK Pin Definitions**, page 5. • Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	2.5.3	• Added notation of "open-drain" to TDO pin in Table 4. • The final GND pin in each of six pinout tables was inadvertently deleted in v2.5.1. This revision restores the deleted GND pins as follows: - Pin A1, Table 6, page 16 (FG456) - Pin AF26, Table 7, page 30 (FG676) - Pin AN34, Table 10, page 98 (FF1152) - Pin E1, Table 11, page 130 (FF1148) - Pin C38, Table 12, page 162 (FF1517) - Pin E1, Table 14, page 253 (FF1696)
08/25/03	2.5.5	• Table 4: Deleted Note 2, obsolete. There is only one GNDA pin per MGT. • Table 4: Deleted pins ALT_VRP and ALT_VRN. Not used in Virtex-II Pro FPGAs.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 4, signal descriptions column: - For signals TDI, TMS, and TCK, added: Pins are 3.3V-compatible. - For signals M2, M1, M0, added: Tie to 3.3V only with 100Ω series resistor. No toggling during or after configuration. - For signal TDO, added: No internal pull-up. External pull-up to 3.3V OK with resistor greater than 200Ω.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-4 (Module 4 of Virtex-II Pro X data sheet). Added data on available Pb-free packages and updated package diagrams for affected devices.