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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	996
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-5ff1704i

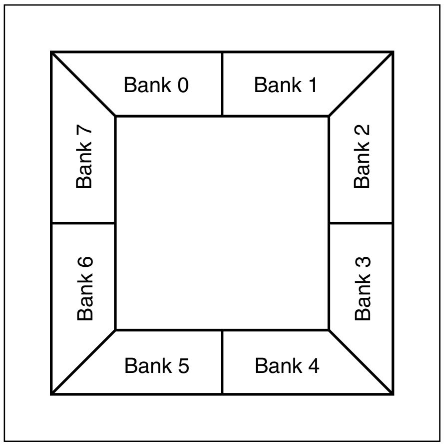

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Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

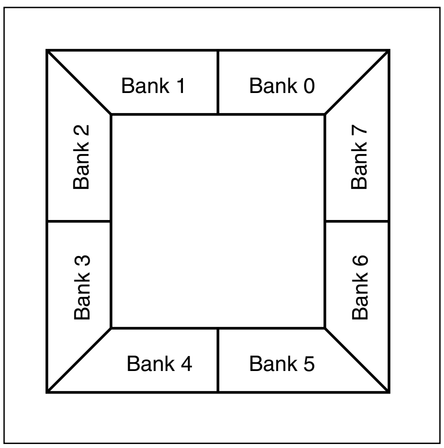

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Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

Sum of Products

Each Virtex-II Pro slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 43.

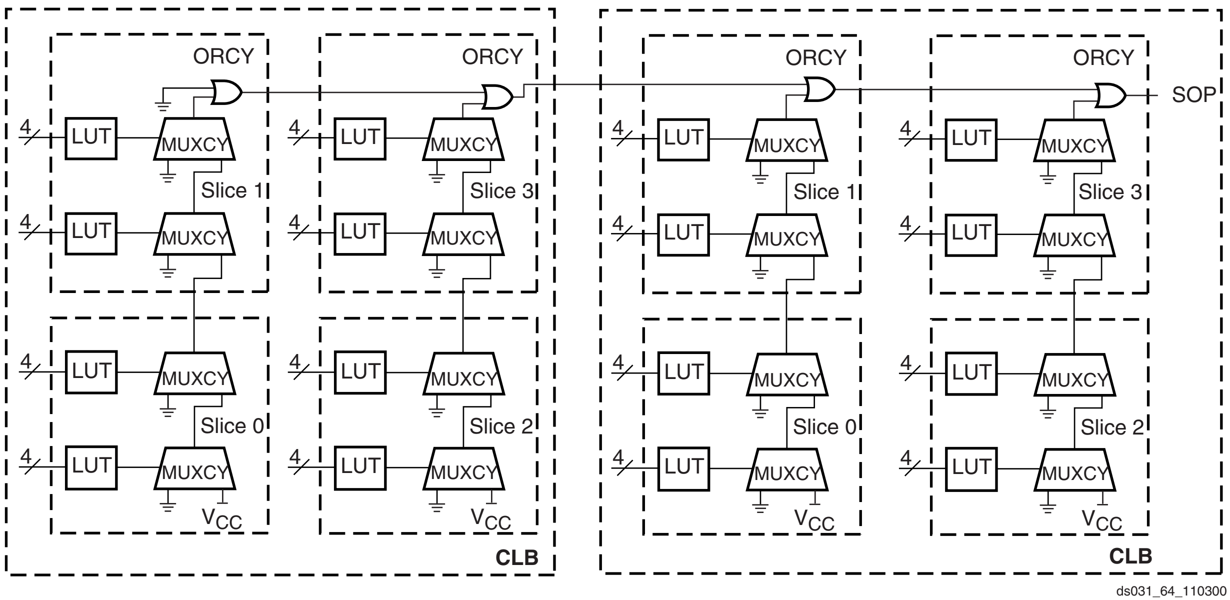

Figure 43: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 44 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

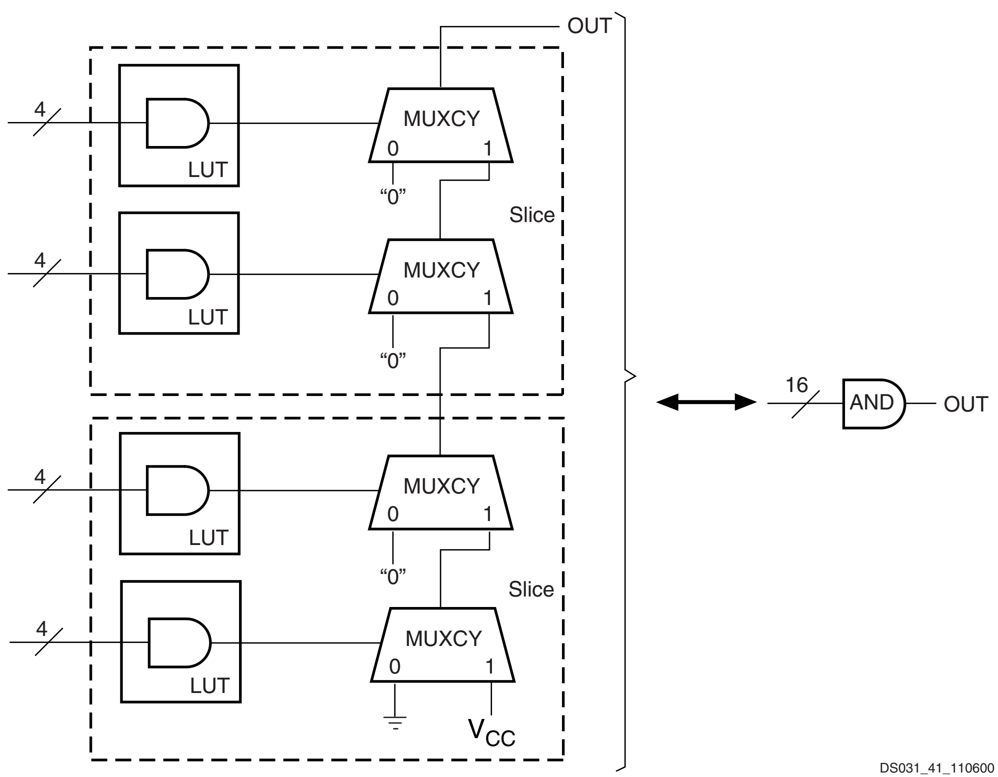

Figure 44: **Wide-Input AND Gate (16 Inputs)**

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 27.

Table 27: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, connect the CLKFB input to CLK0. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$\mathrm{FREQ}_{\mathrm{CLKFX}} = (M/D) \bullet \mathrm{FREQ}_{\mathrm{CLKIN}}$$

where M and D are two integers. Specifications for M and D are provided under **DCM Timing Parameters** in Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics. By default, $M = 4$ and $D = 1$, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles, with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode. See Table 28 for more details.

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Table 28: **CLKDV Duty Cycle for Non-integer Divides**

CLKDV_DIVIDE	Duty Cycle
1.5	1/3
2.5	2/5
3.5	3/7
4.5	4/9
5.5	5/11
6.5	6/13
7.5	7/15

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 63 illustrates the effects of fine-phase shifting. For more information on DCM features, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 29 lists fine-phase shifting control pins, when used in variable mode.

Table 29: **Fine Phase Shifting Control Pins**

Control Pin	Direction	Function
PSINCDEC	In	Increment or decrement
PSEN	In	Enable ± phase shift
PSCLK	In	Clock for phase shift
PSDONE	Out	Active when completed

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP).

Virtex-II Pro device configuration using Boundary-Scan is compatible with with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 32: **Virtex-II Pro Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 33 lists the default total number of bits required to configure each device.

Table 33: **Virtex-II Pro Default Bitstream Lengths**

Device	Number of Configuration Bits
XC2VP2	1,305,376
XC2VP4	3,006,496
XC2VP7	4,485,408
XC2VP20	8,214,560
XC2VPX20	8,214,560
XC2VP30	11,589,920
XC2VP40	15,868,192
XC2VP50	19,021,344
XC2VP70	26,098,976
XC2VPX70	26,098,976
XC2VP100	34,292,768

Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Virtex-II Pro X			Virtex-II Pro			Units
		Min	Typ	Max	Min	Typ	Max	
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	1.25			1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			2.0			V
I_{REF}	V_{REF} current per pin			10			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10			10	µA
C_{IN}	Input capacitance (sample-tested)			10			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)			150			150	µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample-tested)			150			150	µA
I_{BATT}(1)	Battery supply current	Note (2)			Note (2)			nA
$I_{CCAUXTX}$	Operating AVCCAUXTX supply current		115			60	105	mA
$I_{CCAUXRX}$	Operating AVCCAUXRX supply current		85			35	75	mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC-coupled		55			30		mA
	Operating I_{TTX} supply current when transmitter is DC-coupled	N/A	N/A	N/A		15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC-coupled		15			0		mA
	Operating I_{TRX} supply current when receiver is DC-coupled	N/A	N/A	N/A		15		
P_{CPU}	Power dissipation of PowerPC™ 405 processor block		0.9			0.9		mW/ MHz
P_{RXTX}(3)	Power dissipation of MGT @ 1.25 Gb/s per channel	N/A	N/A	N/A		230		mW
	Power dissipation of MGT @ 2.5 Gb/s per channel		290			310		mW
	Power dissipation of MGT @ 3.125 Gb/s per channel		310			350		mW
	Power dissipation of MGT @ 4.25 Gb/s per channel		450		N/A	N/A	N/A	mW
	Power dissipation of MGT @ 6.25 Gb/s per channel		525		N/A	N/A	N/A	mW

Notes:

1. Characterized, not tested.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

3. Total dissipation of fully operational PMA and PCS combined. This power is the average power supply dissipation per MGT. The averaging was done by simultaneously turning on all eight transceivers and dividing the total power supply dissipation by eight.

Table 27: **RocketIO Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	1.0		3.125(1)	Gb/s
		Wirebond packages	1.0		2.5(1)	Gb/s
Serial data rate, half-speed clock(3) (2X oversampling)		Flipchip packages	0.600		1.0	Gb/s
		Wirebond packages	0.600		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}	2.126 Gb/s – 3.125 Gb/s			0.17	UI(2)
		1.0626 Gb/s – 2.125 Gb/s			0.08	UI
		1.0 Gb/s – 1.0625 Gb/s			0.05	UI
		600 Mb/s – 999 Mb/s			0.08(4)	UI
Serial data output random jitter	T_{RJ}	2.126 Gb/s – 3.125 Gb/s			0.18	UI
		1.0626 Gb/s – 2.125 Gb/s			0.19	UI
		1.0 Gb/s – 1.0625 Gb/s			0.18	UI
		600 Mb/s – 999 Mb/s			0.18(4)	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(5)	T_{TXLAT}	Including CRC		14	17	TXUSRCLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

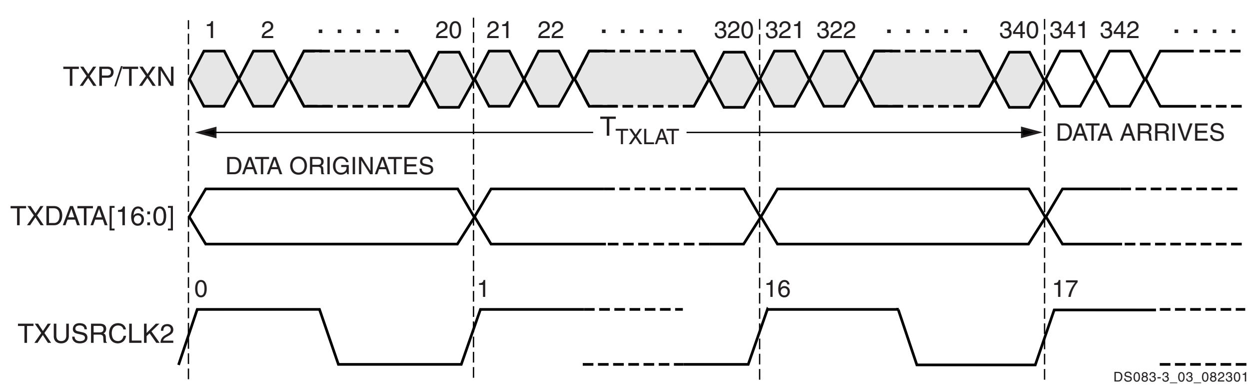

Figure 5: **RocketIO Transmit Latency (Maximum, Including CRC)**

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 56: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade -7	Speed Grade -6	Speed Grade -5	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2	1.80/–0.44	1.85/–0.41	1.96/–0.43	ns
		XC2VP4	1.82/–0.53	1.83/–0.31	1.90/–0.29	ns
		XC2VP7	1.80/–0.34	1.81/–0.24	1.88/–0.19	ns
		XC2VP20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VPX20	1.76/–0.24	1.83/–0.17	1.92/–0.15	ns
		XC2VP30	1.75/–0.22	1.92/–0.26	1.99/–0.23	ns
		XC2VP40	2.25/–0.54	2.40/–0.56	2.49/–0.54	ns
		XC2VP50	2.93/–1.02	2.98/–0.93	3.00/–0.83	ns
		XC2VP70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VPX70	2.79/–0.72	2.79/–0.55	2.78/–0.41	ns
		XC2VP100	N/A	5.58/–2.35	5.60/–2.35	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Date	Version	Revision
09/15/05	4.4	• Table 2: Added Footnote (7) to AVCCAUXRX for RocketIO X (1.8V for all non-8B/10B-encoded data). • Table 3: - Power dissipation for 10.3125 Gb/s deleted. - Max $I_{CCAUXTX}$ and $I_{CCAUXRX}$ specifications added for Virtex-II Pro. • Table 11: Added specification for minimum p-p differential input voltage. • Table 22: - F_{GCLK}: Changed high end of range to 425 MHz. - T_{GJTT}: Changed measurement units to picoseconds and added maximum specifications for two bit rate ranges. - T_{LOCK}: Changed measurement units to microseconds and adderd typical specification. - T_{PHASE}: Changed measurement units to microseconds and adderd typical and maximum specifications. • Table 24: - All parameters: Deleted specifications for 10.3125 Gb/s. - T_{RJTOL}: Added typical specifications. - T_{JTOL}, T_{SJTOL}, and T_{DDJTOL}: Added typical and maximum specifications. • Table 26: Restructured table. Total Jitter parameter added. All jitter parameters respecified. • Table 28: Restructured table and added new specifications.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Table 15: Removed -7 designations for XC2VPX20 and XC2VPX70 devices.
03/05/07	4.6	*No changes in Module 3 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Changed I_{TRX} typical value in Table 3.

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Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	K15			
N/A	GND	K17			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M10			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M17			
N/A	GND	N10			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	N17			
N/A	GND	P10			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	P17			
N/A	GND	R10			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L53_0/No_Pair		A21	NC		
0	IO_L54N_0		H18	NC		
0	IO_L54P_0		G18	NC		
0	IO_L56N_0		C21	NC		
0	IO_L56P_0		C20	NC		
0	IO_L57N_0		J17	NC		
0	IO_L57P_0/VREF_0		H17	NC		
0	IO_L67N_0		E17			
0	IO_L67P_0		D17			
0	IO_L68N_0		D18			
0	IO_L68P_0		C18			
0	IO_L69N_0		J16			
0	IO_L69P_0/VREF_0		H16			
0	IO_L73N_0		E16			
0	IO_L73P_0		D16			
0	IO_L74N_0/GCLK7P		C16			
0	IO_L74P_0/GCLK6S		B16			
0	IO_L75N_0/GCLK5P	BREFCLKN	G16			
0	IO_L75P_0/GCLK4S	BREFCLKP	F16			
1	IO_L75N_1/GCLK3P		F15			
1	IO_L75P_1/GCLK2S		G15			
1	IO_L74N_1/GCLK1P		B15			
1	IO_L74P_1/GCLK0S		C15			
1	IO_L73N_1		D15			
1	IO_L73P_1		E15			
1	IO_L69N_1/VREF_1		H15			
1	IO_L69P_1		J15			
1	IO_L68N_1		C13			
1	IO_L68P_1		D13			
1	IO_L67N_1		D14			
1	IO_L67P_1		E14			
1	IO_L57N_1/VREF_1		H14	NC		
1	IO_L57P_1		J14	NC		
1	IO_L56N_1		C11	NC		
1	IO_L56P_1		C10	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	TXPPAD9	A8				
N/A	GNDA9	C8				
N/A	RXPPAD9	A7				
N/A	RXNPAD9	A6				
N/A	VTRXPAD9	B7				
N/A	AVCCAUXRX9	B6				
N/A	AVCCAUXTX11	B4	NC	NC		
N/A	VTTXPAD11	B5	NC	NC		
N/A	TXNPAD11	A5	NC	NC		
N/A	TXPPAD11	A4	NC	NC		
N/A	GNDA11	C5	NC	NC		
N/A	RXPPAD11	A3	NC	NC		
N/A	RXNPAD11	A2	NC	NC		
N/A	VTRXPAD11	B3	NC	NC		
N/A	AVCCAUXRX11	B2	NC	NC		
N/A	AVCCAUXRX14	AN2	NC	NC		
N/A	VTRXPAD14	AN3	NC	NC		
N/A	RXNPAD14	AP2	NC	NC		
N/A	RXPPAD14	AP3	NC	NC		
N/A	GNDA14	AM5	NC	NC		
N/A	TXPPAD14	AP4	NC	NC		
N/A	TXNPAD14	AP5	NC	NC		
N/A	VTTXPAD14	AN5	NC	NC		
N/A	AVCCAUXTX14	AN4	NC	NC		
N/A	AVCCAUXRX16	AN6				
N/A	VTRXPAD16	AN7				
N/A	RXNPAD16	AP6				
N/A	RXPPAD16	AP7				
N/A	GNDA16	AM8				
N/A	TXPPAD16	AP8				
N/A	TXNPAD16	AP9				
N/A	VTTXPAD16	AN9				
N/A	AVCCAUXTX16	AN8				
N/A	AVCCAUXRX17	AN10	NC	NC	NC	
N/A	VTRXPAD17	AN11	NC	NC	NC	
N/A	RXNPAD17	AP10	NC	NC	NC	
N/A	RXPPAD17	AP11	NC	NC	NC	
N/A	GNDA17	AM12	NC	NC	NC	

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	Y34		
N/A	GND	AU32		
N/A	GND	AN32		
N/A	GND	G32		
N/A	GND	C32		
N/A	GND	AH31		
N/A	GND	AD31		
N/A	GND	T31		
N/A	GND	M31		
N/A	GND	Y30		
N/A	GND	AU28		
N/A	GND	AN28		
N/A	GND	G28		
N/A	GND	C28		
N/A	GND	AT24		
N/A	GND	AN24		
N/A	GND	AJ24		
N/A	GND	AC24		
N/A	GND	AB24		
N/A	GND	AA24		
N/A	GND	Y24		
N/A	GND	W24		
N/A	GND	V24		
N/A	GND	U24		
N/A	GND	L24		
N/A	GND	G24		
N/A	GND	D24		
N/A	GND	AD23		
N/A	GND	AC23		
N/A	GND	AB23		
N/A	GND	AA23		
N/A	GND	Y23		
N/A	GND	W23		
N/A	GND	V23		
N/A	GND	U23		
N/A	GND	T23		
N/A	GND	AD22		
N/A	GND	AU39		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L49P_0		G26		
0	IO_L50_0/No_Pair		D27		
0	IO_L53_0/No_Pair		D26		
0	IO_L54N_0		K25		
0	IO_L54P_0		L25		
0	IO_L55N_0		G25		
0	IO_L55P_0		H25		
0	IO_L56N_0		E26		
0	IO_L56P_0		E25		
0	IO_L57N_0		C25		
0	IO_L57P_0/VREF_0		C26		
0	IO_L58N_0		L24		
0	IO_L58P_0		M24		
0	IO_L59N_0		J24		
0	IO_L59P_0		K24		
0	IO_L60N_0		G24		
0	IO_L60P_0		H24		
0	IO_L64N_0		E24		
0	IO_L64P_0		F24		
0	IO_L65N_0		D24		
0	IO_L65P_0		C24		
0	IO_L66N_0		M22		
0	IO_L66P_0/VREF_0		M23		
0	IO_L67N_0		K23		
0	IO_L67P_0		L23		
0	IO_L68N_0		J23		
0	IO_L68P_0		H23		
0	IO_L69N_0		E23		
0	IO_L69P_0/VREF_0		F23		
0	IO_L73N_0		C23		
0	IO_L73P_0		D23		
0	IO_L74N_0/GCLK7P		K22		
0	IO_L74P_0/GCLK6S		J22		
0	IO_L75N_0/GCLK5P	BREFCLKN	F22		
0	IO_L75P_0/GCLK4S	BREFCLKP	G22		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L30P_1		G13		
1	IO_L29N_1		K13		
1	IO_L29P_1		J13		
1	IO_L28N_1		M13		
1	IO_L28P_1		L13		
1	IO_L27N_1/VREF_1		E12		
1	IO_L27P_1		D12		
1	IO_L26N_1		F12		
1	IO_L26P_1		G12		
1	IO_L25N_1		J12		
1	IO_L25P_1		H12		
1	IO_L21N_1		L12		
1	IO_L21P_1		K12		
1	IO_L20N_1		C11		
1	IO_L20P_1		C10		
1	IO_L19N_1		F11		
1	IO_L19P_1		E11		
1	IO_L09N_1/VREF_1		J11		
1	IO_L09P_1		H11		
1	IO_L08N_1		D10		
1	IO_L08P_1		E10		
1	IO_L07N_1		G10		
1	IO_L07P_1		F10		
1	IO_L06N_1		J10		
1	IO_L06P_1		H10		
1	IO_L05_1/No_Pair		K11		
1	IO_L03N_1/VREF_1		D9		
1	IO_L03P_1		C9		
1	IO_L02N_1		E9		
1	IO_L02P_1		F9		
1	IO_L01N_1/VRP_1		H9		
1	IO_L01P_1/VRN_1		G9		
2	IO_L01N_2/VRP_2		C5		
2	IO_L01P_2/VRN_2		C6		
2	IO_L02N_2		E7		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L87P_7		AA33		
7	IO_L87N_7		AA34		
7	IO_L86P_7		Y31		
7	IO_L86N_7		Y32		
7	IO_L85P_7		Y39		
7	IO_L85N_7		Y40		
7	IO_L60P_7		Y36		
7	IO_L60N_7		Y37		
7	IO_L59P_7		Y33		
7	IO_L59N_7		Y34		
7	IO_L58P_7		W41		
7	IO_L58N_7/VREF_7		W42		
7	IO_L57P_7		W39		
7	IO_L57N_7		W40		
7	IO_L56P_7		W31		
7	IO_L56N_7		W32		
7	IO_L55P_7		W37		
7	IO_L55N_7		W38		
7	IO_L54P_7		W35		
7	IO_L54N_7		W36		
7	IO_L53P_7		W33		
7	IO_L53N_7		W34		
7	IO_L52P_7		V41		
7	IO_L52N_7/VREF_7		V42		
7	IO_L51P_7		V38		
7	IO_L51N_7		V39		
7	IO_L50P_7		V31		
7	IO_L50N_7		U32		
7	IO_L49P_7		V35		
7	IO_L49N_7		V36		
7	IO_L48P_7		V32		
7	IO_L48N_7		V33		
7	IO_L47P_7		U31		
7	IO_L47N_7		T31		
7	IO_L46P_7		U41		
7	IO_L46N_7/VREF_7		U42		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L26P_4	AU12	
4	IO_L27N_4	AR12	
4	IO_L27P_4/VREF_4	AP12	
4	IO_L28N_4	AW13	
4	IO_L28P_4	AW12	
4	IO_L29N_4	BA12	
4	IO_L29P_4	AY12	
4	IO_L30N_4	AN13	
4	IO_L30P_4	AM13	
4	IO_L34N_4	AU13	
4	IO_L34P_4	AT13	
4	IO_L35N_4	BA13	
4	IO_L35P_4	AY13	
4	IO_L36N_4	AM14	
4	IO_L36P_4/VREF_4	AL14	
4	IO_L76N_4	AR15	
4	IO_L76P_4	AT14	
4	IO_L77N_4	AV14	
4	IO_L77P_4	AU14	
4	IO_L78N_4	AP14	
4	IO_L78P_4	AN14	
4	IO_L79N_4	AW15	
4	IO_L79P_4	AY14	
4	IO_L80_4/No_Pair	BB14	
4	IO_L83_4/No_Pair	BA14	
4	IO_L84N_4	AM15	
4	IO_L84P_4	AL15	
4	IO_L85N_4	AT16	
4	IO_L85P_4	AT15	
4	IO_L86N_4	AV15	
4	IO_L86P_4	AU15	
4	IO_L87N_4	AP15	
4	IO_L87P_4/VREF_4	AN15	
4	IO_L37N_4	AY16	
4	IO_L37P_4	AY15	
4	IO_L38N_4	BB15	
4	IO_L38P_4	BA15	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L10N_5	AW27	NC
5	IO_L10P_5	AW26	NC
5	IO_L45N_5/VREF_5	AN27	
5	IO_L45P_5	AP27	
5	IO_L44N_5	AU27	
5	IO_L44P_5	AV27	
5	IO_L43N_5	AR27	
5	IO_L43P_5	AR26	
5	IO_L39N_5	AL27	
5	IO_L39P_5	AM27	
5	IO_L38N_5	BA28	
5	IO_L38P_5	BB28	
5	IO_L37N_5	AY28	
5	IO_L37P_5	AY27	
5	IO_L87N_5/VREF_5	AN28	
5	IO_L87P_5	AP28	
5	IO_L86N_5	AU28	
5	IO_L86P_5	AV28	
5	IO_L85N_5	AT28	
5	IO_L85P_5	AT27	
5	IO_L84N_5	AL28	
5	IO_L84P_5	AM28	
5	IO_L83_5/No_Pair	BA29	
5	IO_L80_5/No_Pair	BB29	
5	IO_L79N_5	AY29	
5	IO_L79P_5	AW28	
5	IO_L78N_5	AN29	
5	IO_L78P_5	AP29	
5	IO_L77N_5	AU29	
5	IO_L77P_5	AV29	
5	IO_L76N_5	AT29	
5	IO_L76P_5	AR28	
5	IO_L36N_5/VREF_5	AL29	
5	IO_L36P_5	AM29	
5	IO_L35N_5	AY30	
5	IO_L35P_5	BA30	
5	IO_L34N_5	AT30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	