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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-5ffg1517c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Functional Description: RocketIO Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO multi-gigabit transceiver. For an in-depth discussion of the RocketIO MGT, including digital and analog design considerations, refer to the ***RocketIO Transceiver User Guide***.

RocketIO Overview

Up to twenty RocketIO MGTs are available. The MGT is designed to operate at any baud rate in the range of 622 Mb/s to 3.125 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 4.

The RocketIO MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 3.125 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The PCS contains the bypassable 8B/10B encoder/ decoder, elastic buffers, and Cyclic Redundancy Check (CRC) units. The encoder and decoder handle the 8B/10B coding scheme. The elastic buffers support the clock correction (rate matching) and channel bonding features. The CRC units perform CRC generation and checking.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 10, page 11 shows a high-level block diagram of the RocketIO transceiver and its FPGA interface signals.

Table 4: **Protocols Supported by RocketIO Transceiver**

Mode	Channels (Lanes)(1)	I/O Bit Rate (Gb/s)
Fibre Channel	1	1.06
		2.12
		3.1875 (2)
Gigabit Ethernet	1	1.25
10Gbit Ethernet	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4, ...	0.622 – 3.125
Custom Protocol	1, 2, 3, 4, ...	up to 3.125

Notes:
1. One channel is considered to be one transceiver.
2. Virtex-II Pro MGT can support the 10G Fibre Channel data rates of 3.1875 Gb/s across 6" of standard FR-4 PCB and one connector (Molex 74441 or equivalent) with a bit error rate of 10^{-12} or better.

PMA

Transmitter Output

The RocketIO transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 8. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω (or, optionally, 75Ω) source resistors. The signal swing is created by switching the current in a common-source differential pair.

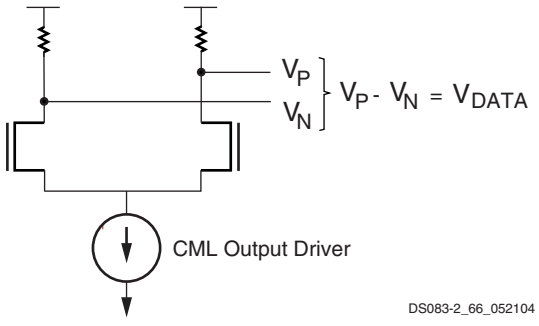

Figure 8: **CML Output Configuration**

Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by V_{TTX}. This configuration uses a CML approach with selectable 50Ω or 75Ω termination to TXP and TXN as shown in Figure 9.

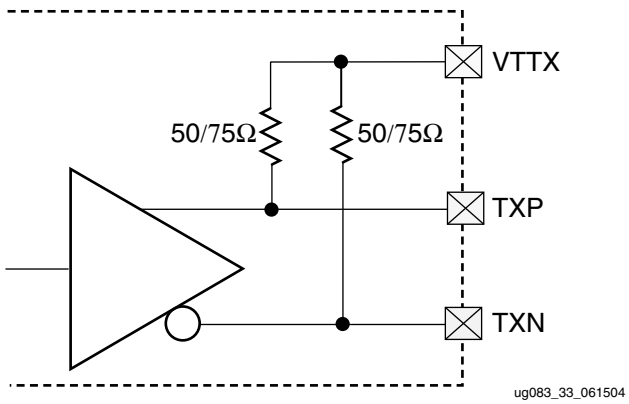

Figure 9: **RocketIO Transmit Termination**

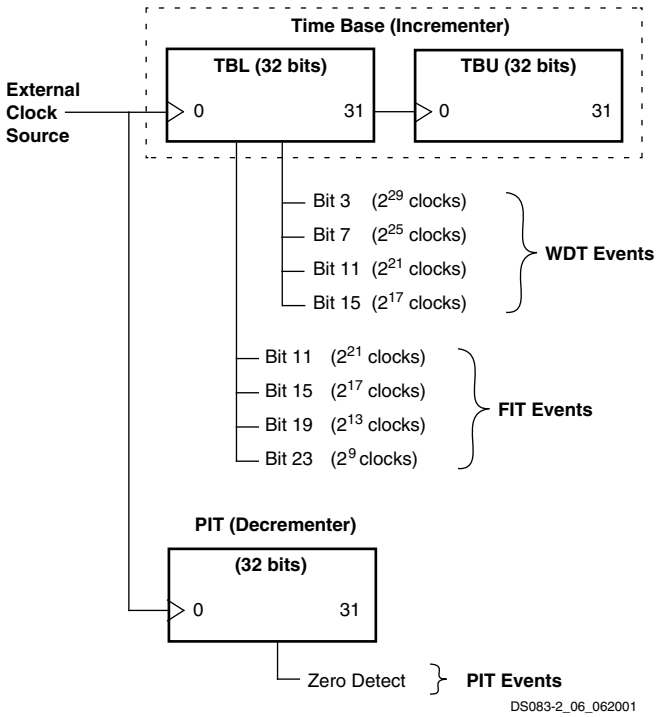

Figure 17: **Relationship of Timer Facilities to Base Clock**

Interrupts

The PPC405 provides an interface to an interrupt controller that is logically outside the PPC405 core. This controller combines the asynchronous interrupt inputs and presents them to the embedded core as a single interrupt signal. The sources of asynchronous interrupts are external signals, the JTAG/debug unit, and any implemented peripherals.

Debug Logic

All architected resources on the embedded PPC405 core can be accessed through the debug logic. Upon a debug event, the PPC405 core provides debug information to an external debug tool. Three different types of tools are supported depending on the debug mode: ROM monitors, JTAG debuggers, and instruction trace tools.

In internal debug mode, a debug event enables exception-handling software at a dedicated interrupt vector to take over the CPU core and communicate with a debug tool. The debug tool has read-write access to all registers and can set hardware or software breakpoints. ROM monitors typically use the internal debug mode.

In external debug mode, the CPU core enters stop state (stops instruction execution) when a debug event occurs. This mode offers a debug tool read-write access to all registers in the PPC405 core. Once the CPU core is in stop state, the debug tool can start the CPU core, step an instruction, freeze the timers, or set hardware or software break points. In addition to CPU core control, the debug logic is capable of writing instructions into the instruction cache, eliminating the need for external memory during initial board bring-up. Communication to a debug tool using external debug mode is through the JTAG port.

Debug wait mode offers the same functionality as external debug mode with one exception. In debug wait mode, the CPU core goes into wait state instead of stop state after a debug event. Wait state is identical to stop state until an interrupt occurs. In wait state, the PPC405 core can vector to an exception handler, service an interrupt and return to wait state. This mode is particularly useful when debugging real time control systems.

Real-time trace debug mode is always enabled. The debug logic continuously broadcasts instruction trace information to the trace port. When a debug event occurs, the debug logic signals an external debug tool to save instruction trace information before and after the event. The number of instructions traced depends on the trace tool.

Debug events signal the debug logic to stop the CPU core, put the CPU core in debug wait state, cause a debug exception or save instruction trace information.

Big Endian and Little Endian Support

The embedded PPC405 core supports big endian or little endian byte ordering for instructions stored in external memory. Since the PowerPC architecture is big endian internally, the ICU rearranges the instructions stored as little endian into the big endian format. Therefore, the instruction cache always contains instructions in big endian format so that the byte ordering is correct for the execution unit. This feature allows the 405 core to be used in systems designed to function in a little endian environment.

- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant. (See Global Clock Multiplexer Buffers, page 48.)
- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row. (See 3-State Buffers, page 43.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice. (See CLB/Slice Configurations, page 44.)
- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See Sum of Products, page 42.)
- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See Shift Registers, page 39.)

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments.

Table 35: **IOB Input Switching Characteristics**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.84	0.87	0.91	ns, max
Pad to I output, with delay	T_{IOPID}	XC2VP2	1.84	1.94	2.06	ns, max
		XC2VP4	1.84	1.94	2.06	ns, max
		XC2VP7	1.84	1.94	2.06	ns, max
		XC2VP20	2.14	2.23	2.37	ns, max
		XC2VPX20	2.14	2.23	2.37	ns, max
		XC2VP30	2.14	2.26	2.46	ns, max
		XC2VP40	2.54	2.67	2.81	ns, max
		XC2VP50	2.54	2.68	2.87	ns, max
		XC2VP70	2.54	2.72	2.91	ns, max
		XC2VPX70	2.54	2.72	2.91	ns, max
		XC2VP100	N/A	4.71	4.80	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.86	0.89	0.93	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2VP2	2.30	2.62	2.97	ns, max
		XC2VP4	2.57	2.89	3.23	ns, max
		XC2VP7	2.50	2.84	3.17	ns, max
		XC2VP20	2.65	3.04	3.42	ns, max
		XC2VPX20	2.65	3.04	3.42	ns, max
		XC2VP30	2.69	3.12	3.51	ns, max
		XC2VP40	3.30	3.63	4.03	ns, max
		XC2VP50	3.86	4.10	4.45	ns, max
		XC2VP70	4.00	4.25	4.57	ns, max
		XC2VPX70	4.00	4.25	4.57	ns, max
		XC2VP100	N/A	6.50	7.06	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.60	0.60	0.67	ns, max

Table 36: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.59	0.68	0.75	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.59	0.68	0.75	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.59	0.68	0.75	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.49	0.57	0.62	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.27	0.31	0.35	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.27	0.31	0.35	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.17	0.20	0.22	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.17	0.20	0.22	ns
LVDS, 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.33	0.37	0.41	ns
LVDS, 2.5V, with Differential Termination (DT)	LVDS_25_DT	$T_{ILVDS\_25\_DT}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DT	LVDSEXT_25_DT	$T_{ILVDSEXT\_25\_DT}$	0.33	0.37	0.41	ns
ULVDS, 2.5V, with DT	ULVDS_25_DT	$T_{IULVDS\_25\_DT}$	0.31	0.36	0.40	ns
LDT, 2.5V, with DT	LDT_25_DT	$T_{ILDT\_25\_DT}$	0.31	0.36	0.40	ns

Multiplier Switching Characteristics

Table 45: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T_{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T_{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T_{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T_{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T_{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T_{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T_{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T_{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T_{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T_{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T_{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T_{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T_{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T_{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T_{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T_{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T_{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T_{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T_{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T_{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T_{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T_{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T_{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T_{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T_{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T_{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T_{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T_{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T_{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T_{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T_{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T_{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T_{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T_{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T_{MULT_P0}	1.13	1.27	1.43	ns, max

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Date	Version	Revision
12/05/03 (cont'd)	3.0 (cont'd)	• Non-speedsfile parameter values added or updated: • Table 3: I_{BATT}. • Table 4: For XC2VP100, I_{CCINTQ}, I_{CCOQ}, and I_{CCAUXQ}. • Table 5: For XC2VP100, $I_{CCINTMIN}$. • Table 17: T_{CPWL} and T_{CPWH}. • Table 25: Added explanatory footnote to T_{RXLAT} (MGT receiver latency) max value. • Table 57: Added Footnote (3) regarding use of CLKIN_DIVIDE_BY_2 attribute.
02/19/04	3.1	• Updated time and frequency parameters as per speedsfile **v1.85**. • Table 2, Recommended Operating Conditions: Revised Footnotes (4) and (6). • Table 4, Quiescent Supply Current: Added Footnote (1) and updated Typical parameters. • Table 10, LVPECL DC Specifications: Added parameter values for Maximum Differential Input Voltage (LVPECL). • Table 14, Register-to-Register Performance: Removed reference to a number of designs for which test data is no longer provided. • Table 16, Processor Clocks Absolute AC Characteristics: Added Footnote (1) referring to XAPP755. • Added Table 41, Clock Distribution Switching Characteristics. • Revised section Configuration Timing, page 39 through page 41, and JTAG Test Access Port Switching Characteristics, page 42, with improved timing diagrams, parameter tables, and organization. • Table 50, Master/Slave Serial Mode Timing Characteristics, and Table 51, SelectMAP Mode Write Timing Characteristics: Added parameter $F_{CC\_STARTUP}$. • Table 51, SelectMAP Mode Write Timing Characteristics: Broke out T_{SMDCC}/T_{SMCCD}, DATA[0:7] setup/hold time, by device, and added new parameter specifications for XC2VP70 and XC2VP100 devices. • Table 57, Operating Frequency Ranges: Added callouts for existing Footnote (3) to the four CLKIN parameters. Added new Footnote (4) to the four CLKIN parameters. Added new Footnote (5) to CLK2X, CLK2X180. Added new Footnote (6) to CLK2X, CLK2X180; CLK0, CLK180; and CLKIN (using DLL outputs).
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Table 2, Recommended Operating Conditions: Corrected VTTX/VTRX lower voltage limit from 1.8V to 1.6V. • Table 5, Power-On Current for Virtex-II Pro Devices: Added Footnote (2) stating that listed I_{CCOMIN} values apply to the entire device (all banks). • Table 40, Output Delay Measurement Methodology: Corrected V_{MEAS} for LVTTL from 1.4V to 1.65V. • Table 57, Operating Frequency Ranges: Corrected CLKOUT_FREQ_1X_LF_MAX and CLKIN_FREQ_DLL_LF_MAX for -7 devices from 210 MHz to 270 MHz. • Table 65, Package Skew: Removed XC2VP40FF1517.
06/30/04	4.0	Merged in DS110-3 (Module 3 of Virtex-II Pro X data sheet). This merge added numerous previously unpublished RocketIO X MGT parameters. Specifications in this revision are from speedsfile **v1.86**.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	IO_L85N_7	G2
7	IO_L06P_7	G3
7	IO_L06N_7	G4
7	IO_L04P_7	F1
7	IO_L04N_7/VREF_7	F2
7	IO_L03P_7	F3
7	IO_L03N_7	F4
7	IO_L02P_7	F5
7	IO_L02N_7	E4
7	IO_L01P_7/VRN_7	E2
7	IO_L01N_7/VRP_7	E3
0	VCCO_0	F8
0	VCCO_0	F7
0	VCCO_0	E8
1	VCCO_1	F9
1	VCCO_1	F10
1	VCCO_1	E9
2	VCCO_2	H12
2	VCCO_2	H11
2	VCCO_2	G11
3	VCCO_3	K11
3	VCCO_3	J12
3	VCCO_3	J11
4	VCCO_4	M9
4	VCCO_4	L9
4	VCCO_4	L10
5	VCCO_5	M8
5	VCCO_5	L8
5	VCCO_5	L7
6	VCCO_6	K6
6	VCCO_6	J6
6	VCCO_6	J5
7	VCCO_7	H6
7	VCCO_7	H5

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
2	IO_L58N_2/VREF_2	M21			
2	IO_L58P_2	N21			
2	IO_L60N_2	M22			
2	IO_L60P_2	M23			
2	IO_L85N_2	M25			
2	IO_L85P_2	M26			
2	IO_L86N_2	N18			
2	IO_L86P_2	N19			
2	IO_L88N_2/VREF_2	N22			
2	IO_L88P_2	N23			
2	IO_L90N_2	N24			
2	IO_L90P_2	N25			
3	IO_L90N_3	P25			
3	IO_L90P_3	P24			
3	IO_L89N_3	P23			
3	IO_L89P_3	P22			
3	IO_L87N_3/VREF_3	P19			
3	IO_L87P_3	P18			
3	IO_L85N_3	R26			
3	IO_L85P_3	R25			
3	IO_L60N_3	R23			
3	IO_L60P_3	R22			
3	IO_L59N_3	P21			
3	IO_L59P_3	R21			
3	IO_L57N_3/VREF_3	R19			
3	IO_L57P_3	R18			
3	IO_L55N_3	T26			
3	IO_L55P_3	T25			
3	IO_L54N_3	T22			
3	IO_L54P_3	T21			
3	IO_L53N_3	R20			
3	IO_L53P_3	T20			
3	IO_L51N_3/VREF_3	U26			
3	IO_L51P_3	U25			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
1	IO_L06N_1	E9			
1	IO_L06P_1	E8			
1	IO_L05_1/No_Pair	F8			
1	IO_L03N_1/VREF_1	D7			
1	IO_L03P_1	E7			
1	IO_L02N_1	C6			
1	IO_L02P_1	D6			
1	IO_L01N_1/VRP_1	A3			
1	IO_L01P_1/VRN_1	B3			
2	IO_L01N_2/VRP_2	C4			
2	IO_L01P_2/VRN_2	D3			
2	IO_L02N_2	A2			
2	IO_L02P_2	B1			
2	IO_L03N_2	C2			
2	IO_L03P_2	C1			
2	IO_L04N_2/VREF_2	D2			
2	IO_L04P_2	D1			
2	IO_L05N_2	E4			
2	IO_L05P_2	E3			
2	IO_L06N_2	E2			
2	IO_L06P_2	E1			
2	IO_L40N_2/VREF_2	F5	NC	NC	NC
2	IO_L40P_2	F4	NC	NC	NC
2	IO_L42N_2	F3	NC	NC	NC
2	IO_L42P_2	F2	NC	NC	NC
2	IO_L43N_2	G6	NC		
2	IO_L43P_2	G5	NC		
2	IO_L44N_2	G4	NC		
2	IO_L44P_2	G3	NC		
2	IO_L45N_2	F1	NC		
2	IO_L45P_2	G1	NC		
2	IO_L46N_2/VREF_2	H6	NC		
2	IO_L46P_2	H5	NC		
2	IO_L47N_2	H4	NC		
2	IO_L47P_2	H3	NC		
2	IO_L48N_2	H2	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L59N_2		P8			
2	IO_L59P_2		P7			
2	IO_L60N_2		N4			
2	IO_L60P_2		N3			
2	IO_L85N_2		P3			
2	IO_L85P_2		P2			
2	IO_L86N_2		R8			
2	IO_L86P_2		R7			
2	IO_L87N_2		P5			
2	IO_L87P_2		P4			
2	IO_L88N_2/VREF_2		R2			
2	IO_L88P_2		T2			
2	IO_L89N_2		R6			
2	IO_L89P_2		R5			
2	IO_L90N_2		R4			
2	IO_L90P_2		R3			
3	IO_L90N_3		U1			
3	IO_L90P_3		V1			
3	IO_L89N_3		T5			
3	IO_L89P_3		T6			
3	IO_L88N_3		T3			
3	IO_L88P_3		T4			
3	IO_L87N_3/VREF_3		U2			
3	IO_L87P_3		U3			
3	IO_L86N_3		T7			
3	IO_L86P_3		T8			
3	IO_L85N_3		U4			
3	IO_L85P_3		U5			
3	IO_L60N_3		V2			
3	IO_L60P_3		W2			
3	IO_L59N_3		T9			
3	IO_L59P_3		U9			
3	IO_L58N_3		V3			
3	IO_L58P_3		V4			
3	IO_L57N_3/VREF_3		W1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
5	IO_L48N_5		AH20	NC		
5	IO_L48P_5		AH21	NC		
5	IO_L47N_5		AE19	NC		
5	IO_L47P_5		AE20	NC		
5	IO_L46N_5		AD18	NC		
5	IO_L46P_5		AC18	NC		
5	IO_L45N_5/VREF_5		AJ22			
5	IO_L45P_5		AH22			
5	IO_L44N_5		AE21			
5	IO_L44P_5		AE22			
5	IO_L43N_5		AD19			
5	IO_L43P_5		AC19			
5	IO_L39N_5		AG21			
5	IO_L39P_5		AF21			
5	IO_L38N_5		AF22			
5	IO_L38P_5		AF23			
5	IO_L37N_5		AD20			
5	IO_L37P_5		AC20			
5	IO_L09N_5/VREF_5		AK23			
5	IO_L09P_5		AJ23			
5	IO_L08N_5		AE23			
5	IO_L08P_5		AE24			
5	IO_L07N_5/VREF_5		AD21			
5	IO_L07P_5		AC21			
5	IO_L06N_5/VRP_5		AH23			
5	IO_L06P_5/VRN_5		AG23			
5	IO_L05_5/No_Pair		AD23			
5	IO_L03N_5/D4		AH24			
5	IO_L03P_5/D5		AG24			
5	IO_L02N_5/D6		AD22			
5	IO_L02P_5/D7		AC22			
5	IO_L01N_5/RDWR_B		AF24			
5	IO_L01P_5/CS_B		AG25			
6	IO_L01P_6/VRN_6		AK28			
6	IO_L01N_6/VRP_6		AJ28			

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M23		
N/A	VCCINT	AB22		
N/A	VCCINT	AA22		
N/A	VCCINT	Y22		
N/A	VCCINT	W22		
N/A	VCCINT	V22		
N/A	VCCINT	U22		
N/A	VCCINT	T22		
N/A	VCCINT	R22		
N/A	VCCINT	P22		
N/A	VCCINT	N22		
N/A	VCCINT	AB21		
N/A	VCCINT	N21		
N/A	VCCINT	AB20		
N/A	VCCINT	N20		
N/A	VCCINT	AB19		
N/A	VCCINT	N19		
N/A	VCCINT	AB18		
N/A	VCCINT	N18		
N/A	VCCINT	AB17		
N/A	VCCINT	N17		
N/A	VCCINT	AB16		
N/A	VCCINT	N16		
N/A	VCCINT	AB15		
N/A	VCCINT	N15		
N/A	VCCINT	AB14		
N/A	VCCINT	N14		
N/A	VCCINT	AB13		
N/A	VCCINT	AA13		
N/A	VCCINT	Y13		
N/A	VCCINT	W13		
N/A	VCCINT	V13		
N/A	VCCINT	U13		
N/A	VCCINT	T13		
N/A	VCCINT	R13		
N/A	VCCINT	P13		
N/A	VCCINT	N13		
N/A	VCCINT	AC12		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	VCCO_2	F8		
2	VCCO_2	U7		
2	VCCO_2	Y5		
2	VCCO_2	N4		
2	VCCO_2	J4		
2	VCCO_2	E4		
2	VCCO_2	U3		
2	VCCO_2	E1		
1	VCCO_1	N14		
1	VCCO_1	K13		
1	VCCO_1	F13		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	K17		
1	VCCO_1	F17		
1	VCCO_1	P16		
1	VCCO_1	N16		
1	VCCO_1	P15		
1	VCCO_1	N15		
0	VCCO_0	K27		
0	VCCO_0	F27		
0	VCCO_0	N26		
0	VCCO_0	P25		
0	VCCO_0	N25		
0	VCCO_0	P24		
0	VCCO_0	N24		
0	VCCO_0	P23		
0	VCCO_0	K23		
0	VCCO_0	F23		
0	VCCO_0	P22		
0	VCCO_0	P21		
N/A	CCLK	AJ10		
N/A	PROG_B	D32		
N/A	DONE	AJ11		
N/A	M0	AP31		
N/A	M1	AJ30		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	AU3		
N/A	GND	AT3		
N/A	GND	D3		
N/A	GND	C3		
N/A	GND	B3		
N/A	GND	AN12		
N/A	GND	G12		
N/A	GND	C12		
N/A	GND	Y10		
N/A	GND	AH9		
N/A	GND	AD9		
N/A	GND	T9		
N/A	GND	M9		
N/A	GND	AU8		
N/A	GND	AN8		
N/A	GND	G8		
N/A	GND	C8		
N/A	GND	Y6		
N/A	GND	AM5		
N/A	GND	AH5		
N/A	GND	T17		
N/A	GND	AT16		
N/A	GND	AN16		
N/A	GND	AJ16		
N/A	GND	AC16		
N/A	GND	AB16		
N/A	GND	AA16		
N/A	GND	Y16		
N/A	GND	W16		
N/A	GND	V16		
N/A	GND	U16		
N/A	GND	L16		
N/A	GND	G16		
N/A	GND	D16		
N/A	GND	AU12		
N/A	GND	AB18		
N/A	GND	AA18		
N/A	GND	Y18		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCAUX		AM11		
N/A	VCCAUX		AN33		
N/A	VCCAUX		AN10		
N/A	VCCAUX		AV39		
N/A	VCCAUX		AV4		
N/A	VCCAUX		AW38		
N/A	VCCAUX		AW22		
N/A	VCCAUX		AW21		
N/A	VCCAUX		AW5		
N/A	VCCAUX		AA42		
N/A	VCCAUX		AA41		
N/A	VCCAUX		AA2		
N/A	VCCAUX		AA1		
N/A	VCCAUX		Y42		
N/A	VCCAUX		Y1		
N/A	VCCAUX		L32		
N/A	VCCAUX		L11		
N/A	VCCAUX		K33		
N/A	VCCAUX		K10		
N/A	VCCAUX		E39		
N/A	VCCAUX		E4		
N/A	VCCAUX		D38		
N/A	VCCAUX		D22		
N/A	VCCAUX		D21		
N/A	VCCAUX		D5		
N/A	GND		AB38		
N/A	GND		AB35		
N/A	GND		AB32		
N/A	GND		AB26		
N/A	GND		AB25		
N/A	GND		AB24		
N/A	GND		AB23		
N/A	GND		AB22		
N/A	GND		AB21		
N/A	GND		AB20		
N/A	GND		AB19		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	